A Customized On-die Oscilloscope for Monitoring of Noise Waveforms inside IC Due to ESD

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Abstract - **An on-die oscilloscope circuit is proposed to monitor the power noise waveforms inside IC due to the electrostatic discharge (ESD) events for a more complete analysis of the effects of the ESD on the electronic systems. When an ESD event occurs, the induced noise voltage waveform in the power supply is sampled and converted to digital data in real time. A holding signal created by the ESD detector circuit is used to hold the digital data. The stored digital data are read and converted back to the analog noise waveform based on the sampling process. The operation of each circuit block in the monitoring IC is analyzed and validated by measurement results. The delay between eight clock signals from the DLL is about 200ps for 620MHz input clock as expected. The power noise waveforms due to the ESD events are measured with a digital oscilloscope instrument using cables and directly sampled by the on-die oscilloscope with a sampling rate of 5GHz and 1.6GHz. These sampled noises are converted and reconstructed into analog noise waveforms, and then compared to the noises measured by the digital oscilloscope.**

Keywords—**Analog-to-Digital Converter(ADC), Binary counter, Delay Locked Loop(DLL), Electrostatic Discharge (ESD), ESD detector, Linear regulator, Monitoring IC, On-die oscilloscope, Reconstruction, Sampling, Shift register, Transmission line pulse (TLP)**

I. INTRODUCTION

ESD events can be easily generated by human activities [1] and cause various failures in an electronic system. For the safety of the product and customers, ESD issues should be considered early in the design phase of the product. Therefore, the ESD immunity test according to international standards [2] has to be implemented on every electronic product. In [3], the effect of ESD noises on the mobile phones was analyzed by checking the immunity of these devices to ESD events, and the ESD immunity was improved by using RC low pass filters. The electromagnetic susceptibility (EMS) problems due to ESD in IC were studied in [4]. In [5], the soft failures in the operation of wearable devices due to the ESD events were studied by

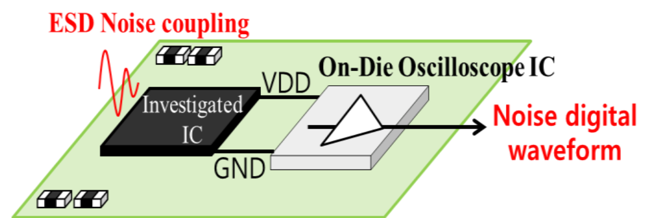

Fig. 1. The on-die oscilloscope for monitoring of power supply noises inside IC in an electronic system.

modeling system-level ESD noises in the wearable devices using the ESD discharging currents.

In all of these proposed papers, the ESD noises inside electronic products were studied in the same way by measuring the ESD noise voltage waveforms with an oscilloscope using cables. However, this measurement method has some limitations and issues. First, soldering the measurement cables to the interested nets could be sometimes infeasible in a smaller and denser product. Second, the measured differential-mode voltages can be affected by the common-mode noises due to the strong radiation from the ESD generator. Third, when measuring the ESD noise waveform, it can be different from the actual ESD noise waveform inside IC because the radiated field can affect the measurement cables, wire bonding, and oscilloscope. Fourth, parasitic resistance, inductance, and capacitance of PCBs and cables can affect measured waveforms, and the longer the path from the event origin to the measuring device, the greater the problems.

Several studies have been proposed to solve these mentioned measurement limitations. In [6], the ESD detection circuit is proposed to approximate the levels of noises due to ESD events. The melted fuse is used to sense the ESD noises, which have levels above the threshold level, by the ESD detector. In [7], the on-chip detector circuit uses inside capacitors to sense ESD noises which are coupled to on-die capacitors. In [8], an RC circuit is used inside the on-chip detector to sense the ESD noises. These all on-die detector circuits can provide only limited information, such as peak voltages or current levels of ESD noises, without any precise information about the actual ESD noise waveforms. In [9], the IC is proposed to monitor ESD noise waveforms. However, this circuit design failed to monitor ESD noise waveforms as expected in a real experiment. In this paper, an on-die oscilloscope circuit is proposed to overcome

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limitations due to the measurement methods using cables and digital oscilloscope by directly capturing the ESD noise waveforms inside IC in a convenient way within a considerable short path for a more complete investigation of the effects of the ESD events on the electronic products, as shown in Fig. 1.

Section II discusses the block diagram of the proposed on-die oscilloscope and explains the operations of circuit blocks when monitoring ESD noises. In section III, the operations of circuit blocks inside the on-die oscilloscope are tested in the experiment. Moreover, the ESD noise waveforms are measured by the oscilloscope using cables and directly sampled by the on-die oscilloscope, and these measured waveforms by the oscilloscope and reconstructed analog noise waveforms by the monitoring IC are compared with each other.

II. ANALYSIS OF OPERATION OF EACH CIRCUIT BLOCK IN THE ON-DIE OSCILLOSCOPE

The overall block diagram of the proposed on-die oscilloscope is shown in Fig. 2. The main building blocks of the system are the linear regulator, the delay locked loop (DLL), 8 flash type analog-to-digital converter (ADC), shift register, binary counter, and ESD detector. An ESD event applied to the power supply net VDD is shown as a "spark" at VDD. For the correct operation of circuit blocks inside the on-die oscilloscope, the linear regulator is used to create a new stable internal power supply VDDA, which must be robust against the ESD noises in the external power supply VDD. For matching the power noise waveforms in the VDD to the sampling range of the ADCs resistive voltage division is used to attenuate the DC parts of the noise waveforms at the (3.3:0.8) ratio and capacitive voltage division is used to attenuate the AC parts of the noise waveforms at the (2.5:1) ratio. The high speed for sampling the high frequency components of the noise waveforms is achieved by combining eight ADCs so that the effective sampling rate is increased by 8 times, and by using the DLL which can provide eight multi-phase high frequency clock signals to eight ADCs for sampling. Each ADC samples and converts the attenuated noise waveform into 5-bit digital data. This proposed on-die oscilloscope requires a high-speed sampling rate of at least 5 GHz to accurately sample high-frequency power noise, such as ESD noise. Flash ADCs with higher sampling rates are preferred over other types of ADCs with higher bit resolution but slower speeds, as its main study is on high- frequency power noise. Flash ADC resolution was only 5 bits, but it was sufficient to capture power noise accurately. The sampled digital data from ADCs are shifted into the shift register, which consists of 128 5-bit D flip-flops (DFFs) storing binary bits. In the shift register, sampled data from each ADC are continuously shifted and lost in the last 5-bit DFFs. A Hold signal is used to stop the data shift inside the shift register. Hold signal is sent to the register from the ESD detector circuit when it senses the occurrence of ESD noises. After the data shift is stopped, the binary counter is used for reading the data from the first 5-bit DFF to the 128th 5-bit DFF per every reference clock pulse supplied from outside. The digital data read from the shift register are converted back to an analog noise waveform through post-processing which is based on the sampling process and the attenuation ratio.

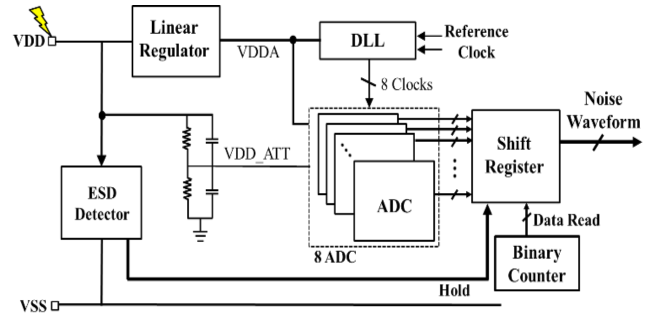


Fig. 2. Block diagram of the proposed on-die oscilloscope.

III. RESULTS AND DISCUSSIONS

A. Designed IC and PCB Structures

The designed monitoring IC was fabricated in a 180nm CMOS process, and its total size is $5{,}000\mu m \times 3{,}916\mu m$. The location of each circuit block in the designed monitoring IC is shown in Fig. 3.

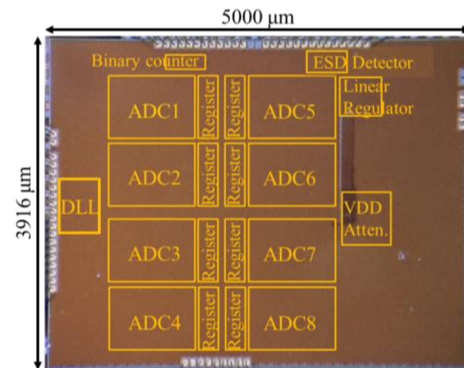
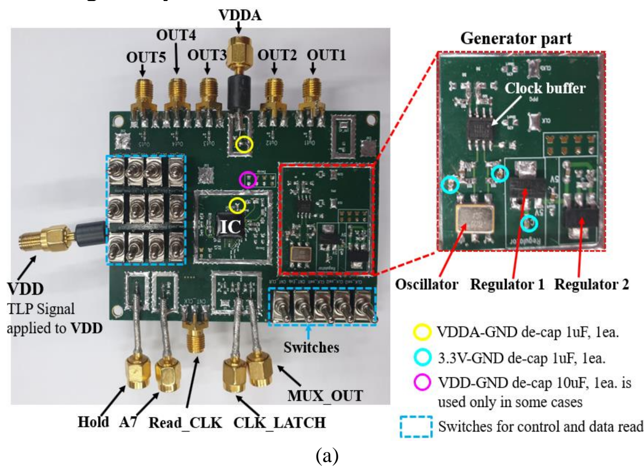


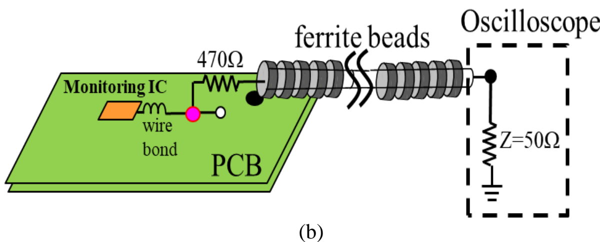
Fig. 3. Designed monitoring IC and locations of each circuit block.

In Fig. 4(a), the designed monitoring IC is mounted on a 6-layer PCB with dimensions of $91mm \times 68mm$ by chip-on-board (COB) assembly. The first layer is used for mounting the designed monitoring IC and electrical components, the second and sixth layers are for the ground planes, and the fifth layer is used for the 3.8V DC VDD power plane to supply the monitoring IC. The fourth layer is divided into two planes, the first is the ground plane, and the second is the 3.3V power plane, which is used to generate the reference clock signals for the DLL by supplying an oscillator and a clock buffer on the PCB. The important signal traces for the input or output signals of the monitoring IC are routed in the third layer with a characteristic impedance of 50 Ω. Two commercial regulators are mounted on the PCB to generate a 3.8V DC VDD power supply and a 3.3V DC power supply from 5.4V DC voltage supplied from outside. The input signal Read_CLK is for providing a reference clock signal to the binary counter of the monitoring IC. Two output signals of the IC (MUX_OUT and CLK_LATCH) are measured by the digital oscilloscope to study the performance of the DLL and are terminated to

ground through 50 Ω resistors on the PCB for impedance matching. For triggering the oscilloscope to start measuring the output data from the registers the output signal A7, the LSB of the 7-bit binary counter is measured. The output Hold signal is measured to study the ESD detector when ESD events occur. For checking the stability of the internal VDDA power supply inside the monitoring IC the output VDDA net is measured on the PCB. The 5-bit data stored in each of the 128 5-bit DFFs in the shift register are read in the proper sequence from the 5 output nets (OUT1 to OUT5) on the PCB when the binary counter starts to operate. Because these output signals are generated by the large size inverter buffers which have low output impedances, they are measured using the semi-rigid cables that are connected to these output nets in series with 470 Ω to create a 520 Ω high impedance probe, as shown in Fig. 4(b). These output signals are measured with a digital oscilloscope and compensated for the 520 Ω high impedance probe gain by multiplying these signals by 10.4.



(a)



(b)

Fig. 4. (a) Designed PCB, measurement cables, and components on the PCB. (b) Setup for measuring important signals and powers.

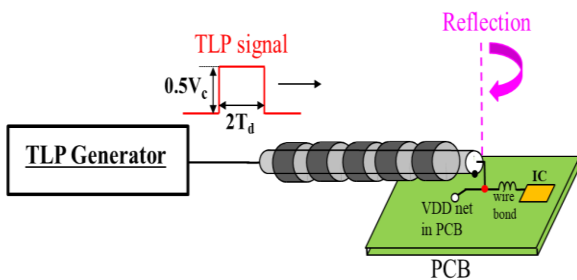


Fig. 5. Test setup for applying TLP signals.

B. Experiment of ESD Detector

In this section, the performance of the ESD detector circuit block is analyzed when a noise occurs in the VDD by applying transmission line pulse (TLP) toward the VDD net on the PCB, as shown in Fig. 5. Most of the applied TLP signal is reflected because the input impedance of the power supply VDD net on the PCB is very small compared to 50 Ω. It is possible to control the amplitude and width of the TLP signal by adjusting the charging voltage (Vc) and the pulse width (Td) from the TLP generator.

When the ESD detector circuit senses noise in the VDD, it changes the initial low state of the Hold signal to a high state to stop the data shift in the register. When the TLP signal with the 5ns pulse widths and charging voltage (Vc) of 140V is applied, the noise with 0.890V amplitude is created in the VDD, as shown in Fig.6. A charging voltage (Vc) of at least 140 V is required for the ESD detector to sense the noise in the VDD and make the high Hold signal. If a charging voltage is below 140V, the noise created in the VDD is not sensible by the ESD detector. From the measurement result, it is shown that the ESD detector circuit can sense all noises in the VDD which have amplitudes higher than 0.890V.

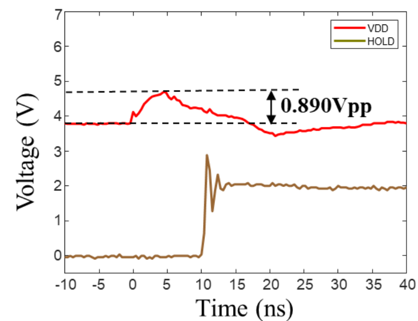


Fig. 6. Measured voltage waveforms of VDD and Hold signals when the TLP signal with the 5ns pulse width and charging voltage of 140V (Vc) is applied.

C. Experimental Validation of Stability of Internal Power

The stability of the internal supply voltage VDDA in the presence of external noise in the VDD is required for the correct operation of the monitoring IC. The power supply rejection ratio (PSRR) of the linear regulator inside IC is shown in Fig. 7. It was confirmed that the linear regulator can block higher frequency noises more effectively. The stability of the VDDA is validated by measuring both the internal supply voltage VDDA and the external supply voltage VDD on the PCB when TLP signals are applied. When a TLP signal with 10ns width is applied the measurement results of the VDD and VDDA voltage waveforms are shown in Fig. 8. Although there is a high 1.111V peak-to-peak noise voltage in the VDD, the noise amplitude in the VDDA is lower than 130 mV peak-to-peak. When two 1μF de-caps are installed between VDDA-GND nets, as shown in Fig. 4(a), to make the VDDA supply net more stable, the noise in the VDDA almost disappears. When the monitoring IC is used for sampling ESD noises, de-caps are installed between VDDA-GND nets to make the stable VDDA net for the correct operation of the monitoring IC.

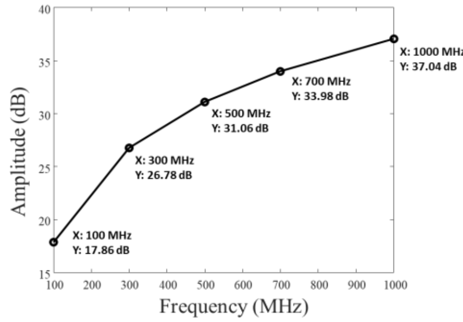


Fig. 7. Simulated PSRR of the linear regulator

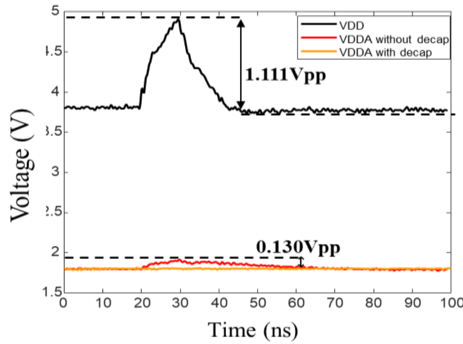


Fig. 8. Measured voltage waveforms of VDD and VDDA signals when the applied TLP signal has 10ns pulse width.

D. Experimental Validation of DLL and ADC Operation.

When the monitoring IC is sampling ESD noises in the power supply VDD it uses 620MHz clock signals to sample. The oscillator and clock buffer on the PCB generate a 620MHz clock signal, which is transferred as a reference clock for the DLL inside the monitoring IC, and the DLL makes eight multi-phase 620MHz clock signals by using this reference clock. These eight multi-phase 620MHz clock signals can be measured in the output CLKLATCH net on the PCB, in which the clock signal is selected from the eight clocks (CLKLATCH1 to CLKLATCH8) by controlling a 3-bit switch on the PCB. The input clock of the first ADC is also measured in the MUX_OUT net on the PCB as a reference clock to extract the delay between the eight clock signals from the DLL by measuring the delay of each clock signal from the same reference clock.

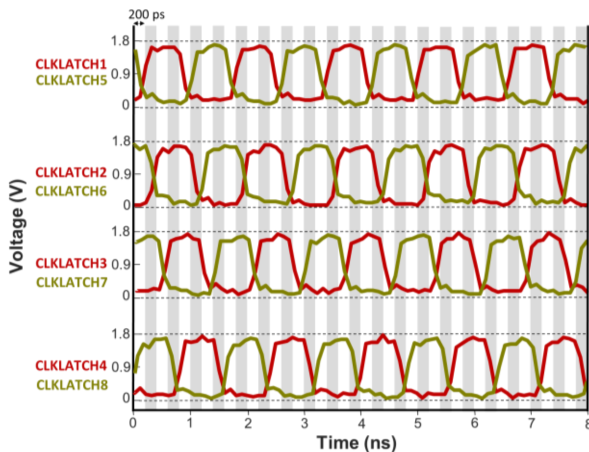


Fig. 9. The measured results of eight 620 MHz multi-phase clock signals generated by the DLL.

Fig. 9 shows the measurement results of all eight clock signals (CLKLATCH1 to CLKLATCH8) from the DLL with respect to the same reference clock. The delay of each clock signal from the previous clock signal is same with the expected 200ps (one eighth of the 620MHz clock signal period). Moreover, the measured rising time of the eight clock signals is short as expected, about 100ps. The total effective sampling rate of the monitoring IC is about 5GHz because eight ADCs with 620MHz input clocks are implemented to sample the ESD noise waveforms.

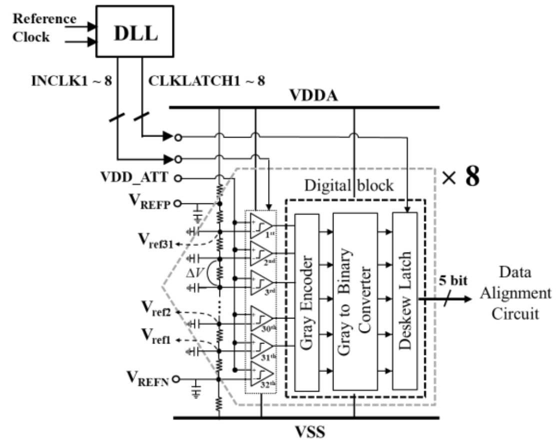


Fig. 10. Block diagram of 5-bit flash ADC

The block diagram of flash ADC is shown in Fig. 10. The ADC is composed of a reference voltage ladder, comparators, and a digital block including a gray encoder, gray to the binary converter, and the latch circuit. The 32-reference voltages are created between VDDA and GND for each comparator. The minimum reference voltage V_REFN and the maximum reference voltage V_REFP are designed as 0.3V and 1.3V, respectively. Therefore, the ADC can capture signals in the sampling range of 0.3V to 1.3V, voltage gap is calculated as 31.3mV. The latch circuit is for adjusting skew that comes from the encoding and converting process. Each ADC consumes about 60mA current in root mean square value.

E ESD Experimental Test Setup

In the ESD immunity test of the electronic products, the effect of ESD is studied by injecting ESD discharge currents with the ESD gun, which generates strong electromagnetic radiation. Therefore, the test setup for conducting the ESD test is considered to reduce the influence of the ESD gun′s radiation on the operation of the monitoring IC. In the ESD experimental test setup, the ESD gun was placed inside a metal gate and important components on the PCB such as the monitoring IC, generator part, and measurement signals are shielded with copper tape as shown in Fig. 11(a). The ESD gun injects an ESD discharge current through the hole in the metal cage into the copper stick that connects to the VDD pad on the PCB. This ESD current creates the noise waveform in the VDD, which is then sampled by the monitoring IC. The same ESD noise waveform is also measured with oscilloscope by soldering the semi-rigid coaxial cable with ferrite beads to the VDD net on the PCB

next to the monitoring IC, as shown in Fig. 11(b). The ground strap of the ESD gun, metal cage, and PCB ground plane were connected to a reference ground plane (GRP) on the floor in this ESD experimental test setup.

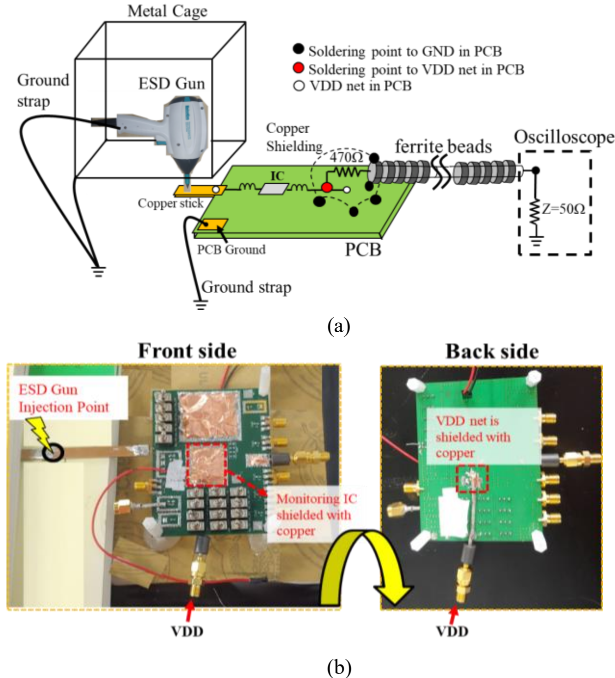


Fig. 11. (a) Test setup for the ESD experiment. (b) Photographs of the front and rear sides of the PCB in the ESD experiment.

F.ESD Experimental Results

The ESD noise waveform in the VDD is sampled by ADCs and stored in registers. After the Hold signal from the ESD detector stops the shifting of data, a 10MHz read clock is applied through the input Read_CLK net to the binary counter inside the monitoring IC for reading the stored data in the shift register. The LSB of the 7-bit binary counter (A7) triggers the oscilloscope to start measuring the 5 output nets (OUT1 ~ 5). In every 10 MHz read clock cycle, digital data from one 5-bit DFFs in the shift register is read through 5 output nets and in total, it takes 128 clock cycles (12.8μs) to read all data from the 128 5-bit DFFs. A set of the measured 128 5-bit binary data is converted to an analog voltage through post-processing and arranged along the corresponding sampling time step of 200ps at the 5GHz sampling rate to reconstruct the noise signal duration of 26 ns. The DC and AC parts of this analog waveform result are then multiplied by the (3.3:0.8), and (2.5:1) ratio to compensate the attenuation in the R-C attenuation circuit in Fig. 2.

In fig. 12(a), the ESD noise voltage in the VDD measured by the digital oscilloscope shows sufficient agreement with the reconstructed analog waveform by the on-die oscilloscope IC after all post-processing. To reconstruct a longer ESD noise duration with the same 128 points, another 200MHz reference clock is supplied to the DLL from the generator part. In this time, the duration of 80ns of the same ESD noise waveform is reconstructed by the on-die oscilloscope due to the low sampling rate of 1.6GHz (8×200MHz). The measured ESD noise voltage in the VDD agrees well with the reconstructed analog waveform by the on-die oscilloscope IC when the 1.6GHz sampling rate is used, as shown in Fig. 12(b). According to the attenuation ratio of DC and AC parts, when applied DC voltage is 3.8V as this ESD experiments, the peak VDD voltage that can be captured by the proposed on-die oscilloscope is 4.8V. This peak value on VDD occurs under 450V ESD events. VDDA which supplies power to DLL, ADC, and the inner part is protected by the linear regulator with de-caps, remained stable. Therefore, the peak ESD voltage value that can be captured by the proposed on-die oscilloscope depends on the sampling range rather than VDDA consideration.

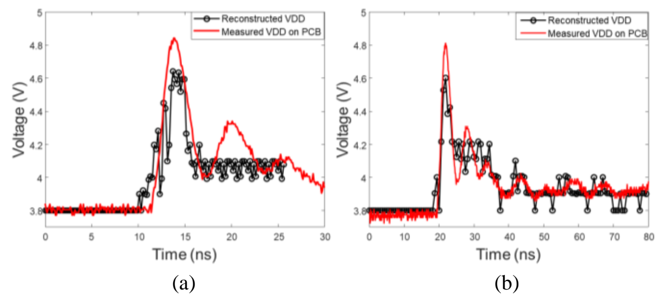


Fig. 12. Measured ESD noise voltages on the PCB and the reconstructed waveforms by the on-die oscilloscope IC with (a) 5GHz sampling rate and (b) with 1.6GHz sampling rate.

TABLE I. Comparison with Previous Research

Ref.	Contribution	Resolution/ Sampling rate	Measurement Validation
[8]	ESD event sensing in power supply voltage using RC based circuit	Not applicable	Yes
[9]	Circuit design for noise waveform capturing	5bit/6.4G	No
This work	Reconstruction of the power noise waveforms inside IC	5bit/5G	Yes

IV. CONCLUSION

This paper proposed the on-die oscilloscope to analyze the effect of ESD on electronic products by monitoring the ESD noise waveforms in a convenient way. The function of each circuit block in the on-die oscilloscope was discussed. The internal design of the manufactured monitoring IC and PCB, and a setup for measuring important signals were explained. The measurement showed that internal power noises in the VDDA can be removed totally by installing de-caps. The operation of the DLL was checked by observing the measurement results of eight multi-phase clock signals generated by the DLL. The performance of the ESD detector circuit was analyzed by observing the noise in the VDD and Hold signal. A sufficient agreement between the ESD noise waveforms measured by the digital oscilloscope using cables and the reconstructed ESD noise waveforms by the designed on-die oscilloscope proved that the on-die oscilloscope can be applied to conduct ESD immunity tests in complex integrated systems by installing this on-die oscilloscope IC next to the real electronic product.

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