

# A Widely Tunable K-band Voltage-Controlled Oscillator

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**Abstract** - A wideband LC voltage-controlled oscillator (VCO) using a 3-bit switched-capacitor bank is proposed for improving the frequency bandwidth in K-band applications. The capacitor bank is composed of metal-oxide-metal (MOM) capacitors to obtain a high-quality factor of the LC tank. The size of the unit capacitor in the capacitor bank is optimized to achieve a wide tuning range. The fabricated chip area is  $400 \mu\text{m} \times 610 \mu\text{m}$  by using the TSMC 65-nm RF CMOS process. The overall tuning range of the proposed VCO is from 18.82 to 23.28 GHz in measurement, and it consumes 46.4 mW, including a buffer stage at a 1 V supply voltage. The measured phase noise is  $-105.8 \text{ dBc/Hz}$  at a 1-MHz offset frequency. A figure-of-merit (FOM) and FOM incorporating the tuning range (FOM<sub>T</sub>) are  $-179 \text{ dBc/Hz}$  and  $-185.2 \text{ dBc/Hz}$  at a 1-MHz offset from the center frequency, respectively.

**Keywords**—Capacitor bank, Local oscillator, Phase noise, Voltage-controlled oscillator

## I. INTRODUCTION

An oscillator that can oscillate at a wide bandwidth is a necessary device for a wideband transmitter at K-band [1]. But, as the oscillation frequency increases, the bandwidth is limited due to the low-quality factor of the tuning components [2]. The transmitter structure based on the multiplier chain can be designed for wideband designs because of the low oscillation frequency of the oscillator, but it has high power consumption and a large chip area.

Several techniques have been introduced to improve the tuning range performance of the VCO. The switchable inductor-based VCO is reported in [3]. In this structure, an inductive tuning method is utilized to achieve a wide tuning range in which the effective inductance of the tank is controlled by the switch located between the differential port. However, multiple inductors require a larger chip area, thus making it difficult to design a compact layout. Moreover, operation at a high frequency is unstable due to the oscillation frequency being near the self-resonance frequency (SRF), and the absence of fine-tuning causes a dead-zone. In [4], a switchable multi-core VCO using switch transistor or transformer is designed to realize multiple frequency bands. However, the parasitic capacitance of the

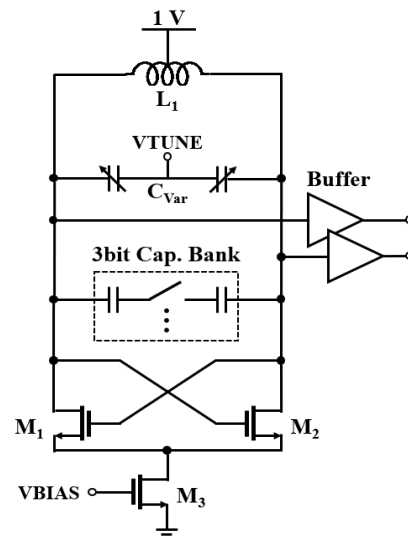


Fig. 1. Schematic diagram of the proposed voltage-controlled oscillator

switch transistor shifts the tuning range down, and the transformer has a much lower  $Q$  than a standalone inductor. Also, the multi-core VCO requires a high-power dissipation which results in a degraded figure-of-merit (FOM).

In this paper, a wideband LC VCO using a high  $Q$ -factor 3-bit capacitor bank is proposed for improving the tuning range [5]. The wide tuning range can be improved by switching the unit capacitor of the capacitor bank, fabricating a smaller chip area than switchable inductor-based VCO. The LC tank for resonance consists of an inductor, varactors, and a 3-bit capacitor bank to increase the tuning range. A cross-coupled transistor pair compensating for the loss of the LC tank, a tied tail current source comprising the VCO core, and a buffer for impedance matching has been designed. The target tuning range is 18.82 - 23.28 GHz, which is a portion of the K-band, and it is slightly raised in consideration of the parasitic capacitance of the switch transistor, which is an issue in [4].

## II. ANALYSIS OF VOLTAGE-CONTROLLED OSCILLATOR

### A. LC Tank Design

The proposed VCO consists of a cross-coupled NMOS transistor, an LC tank, and a buffer amplifier as shown in Fig. 1. The LC tank for resonance at the operation frequency consists of an inductor, varactor, and a 3-bit capacitor bank to increase the tuning range. An LC tank including the inductor, the 3-bit capacitor, and the varactor requires a high

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quality( $Q$ )-factor for wide bandwidth. The inductor  $L_1$  is designed as an octagonal spiral shape to increase the  $Q$ -factor and the size of the inductor is set to have the highest quality factor. Fig. 2 shows the simulation results for the oscillation frequency and output power depending on the inductor provided in the process design kit. The inductance and the  $Q$ -factor of the designed inductor are 100 pH and 20 at 23.3 GHz, respectively. The 3-bit switched capacitor bank provides a capacitance ratio of 1:2:4, and the unit capacitance  $C_{unit}$  is 60 fF as it is shown in Fig. 3. When off state, only  $L_1$  resonates with the intrinsic capacitor  $C_{int}$  which has a capacitance of 120 fF. The capacitors of the capacitor bank were implemented on a metal-oxide-metal (MOM) capacitor instead of a metal-insulator-metal (MIM) capacitor because of the  $Q$ -factor. Fig. 4 shows the comparison of the  $Q$ -factor of MIM and MOM capacitors when having the same capacitance of 170 fF. Physical dimensions of capacitors used in the simulation are  $13.4 \mu\text{m} \times 12.1 \mu\text{m}$  of MOM capacitor and  $17.5 \mu\text{m} \times 12.5 \mu\text{m}$  of MIM capacitor, respectively. The MOM capacitor has a  $Q$ -factor of twice as much to the MIM capacitor over the tuning range because of

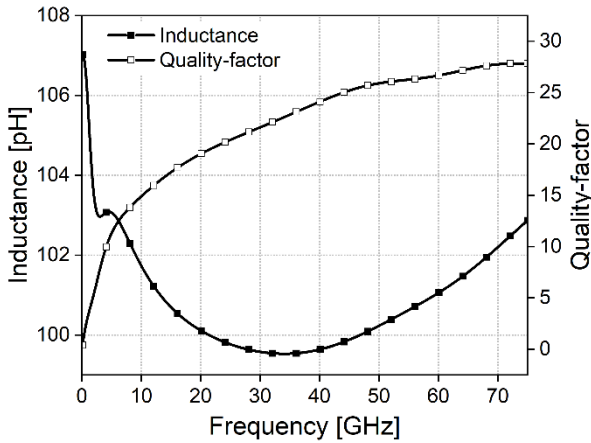


Fig. 2. Simulated output characteristics of the proposed VCO depending on the inductance

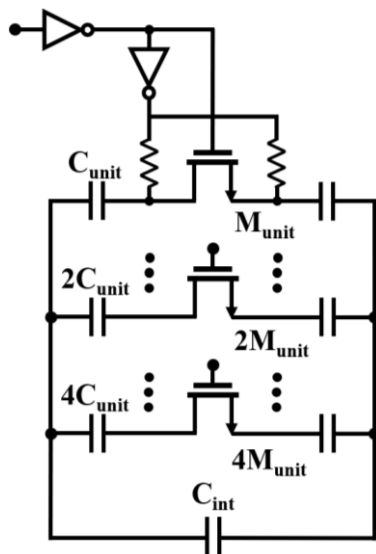


Fig. 3. Schematic diagram of a 3-bit switched capacitor bank

the parasitic resistor, thereby a MOM capacitor was used in this design.

A MOS varactor which is a voltage-dependent capacitor is utilized for fine-tuning. By adjusting the control voltage, the varactor has a capacitance of 110.1-183.1 fF and operates in accumulation mode as shown in Fig. 5 [6]. The adjustable capacitance ranges from 462.6-709.1 fF including the capacitor bank and the varactors, with the increased capacitance of 100 fF due to the layout effect and the parasitic capacitance of the switch. A coarse-tuning is performed by a bit control that makes a total of 8 ( $2^3$ ) gaps with 3-bit input, and a fine-tuning is performed by capacitance variation of the varactor, for ensuring approximately 50% overlap in each bit and preventing a dead-zone. As a result of the electromagnetic simulation, the

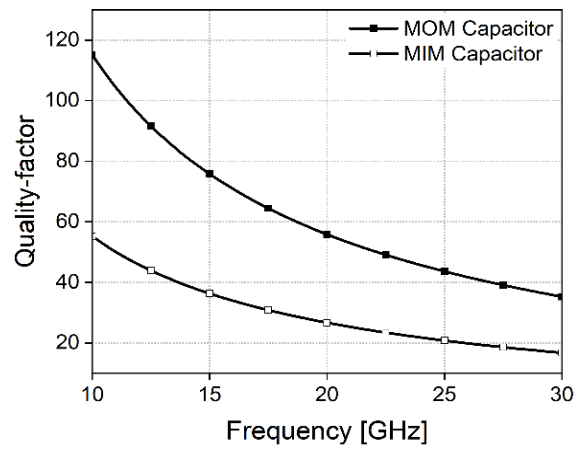


Fig. 4. Simulated quality-factor of MOM and MIM capacitors LC tank achieved a wide tuning range of 19.01–23.08 GHz

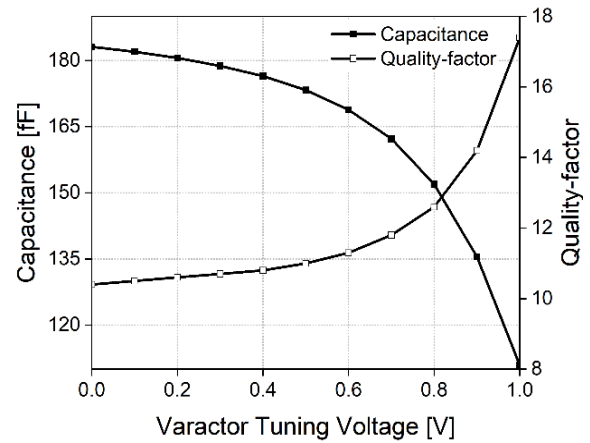


Fig. 5. The capacitance and quality-factor of the MOS varactor operating in the accumulation mode

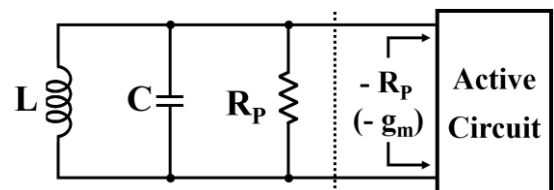


Fig. 6. Equivalent circuit of the VCO

**B. Differential Transistor Pair Design**

The NMOS transistors  $M_1$  and  $M_2$  which have faster mobility than the PMOS transistor is used to compensate for the loss of the LC tank as shown in Fig. 6. The common-source stage is used to design the amplifier having a voltage gain larger than unity. The transistor pairs are cross-coupled connected to comprise the feedback system, providing the  $360^\circ$  shift. These two conditions, called ‘Barkhasuen criteria’, must be satisfied to oscillate. The total width of the cross-coupled pairs  $M_1$  and  $M_2$  is  $32\ \mu\text{m}$  with the minimum gate length of  $60\ \text{nm}$ . The transistor  $M_3$  is used as a current source to solve the overcurrent of the cross-coupled pair.

**C. Class-A Buffer Amplifier Design**

A class-A buffer amplifier is designed to be insensitive to the load variations. The common-source topology is used, and a  $50\ \Omega$  matching is performed by an L-type matching network. The gate bias is set to have the smallest power level in the second harmonic for improving the fundamental output power. Fig. 7 shows the simulation results of the return loss of the buffer amplifier, and a reflection coefficient of  $-10\ \text{dB}$  or less is achieved in the tuning range.

III. RESULTS AND DISCUSSIONS

Fig. 8 shows the photograph of the VCO with the chip area of  $400\ \mu\text{m} \times 610\ \mu\text{m}$  including pads, and the VCO is fabricated using TSMC 65nm 1P9M CMOS process. The output performances, excluding phase noise, were measured by probing with ground-signal (GS) and signal-ground (SG) probe tips. The mounted FR4 printed circuit board (PCB) with an RF SMA connector was used to measure the phase noise by using a signal analyzer. In the case of measuring the phase noise, the supply and bias voltages were applied to the chip using a low drop-out regulator module to minimize the noise from the external equipment. The shielded chamber was used in the phase noise measurement to block externally induced noise. The measurement was performed in one port between differential ports with terminating the other port with the reference impedance of  $50\ \Omega$ .

Fig. 9 shows the tuning range measured by switching on and off the 3-bit capacitor bank and the varactor, from  $18.82$  to  $23.28\ \text{GHz}$ ,  $21.2\%$ . The output power was measured after de-embedding the loss of cable and probe tips for comparison with the simulation results as shown in Fig. 10. From a  $1\text{-V}$  supply, a current of  $24\ \text{mA}$  flows through the VCO core at the frequency in which the performance of phase noise is the best, hence it consumes  $24\ \text{mW}$  at this frequency as shown in Fig. 11. At the oscillation frequency of  $21.45\ \text{GHz}$ , corresponding to bit ‘110’ and the varactor off, the VCO has the lowest phase noise,  $-105.8\ \text{dBc/Hz}$  at  $1\ \text{MHz}$  offset as shown in Fig. 12. Since the spectrum analyzer used for the measurement cannot read the noise power at the  $10\text{-MHz}$  offset from the carrier frequency power, it shows a nonlinearity after  $1\text{-MHz}$ . As one of the main performances of the VCO, the  $FOM$  showing the phase noise compared to power consumption is  $-179\ \text{dBc/Hz}$  and the  $FOM$  incorporating the tuning range ( $FOM_T$ ) is

$-185.2\ \text{dBc/Hz}$ . As shown in Table I, the proposed VCO has both a wide tuning range and low phase noise, thus a decent  $FOM_T$ .

Compared with the previous works, the measured phase noise of the proposed VCO indicates sufficient performance. However, the power consumption is up to  $31\ \text{mW}$ , as can be seen from the  $FOM$ , which shows inefficient operation. The low oscillation efficiency is caused by the low inductance of the implemented LC tank, which requires an increase in the total capacitance to generate the desired oscillation frequency range. The increased varactor to ensure a  $50\%$

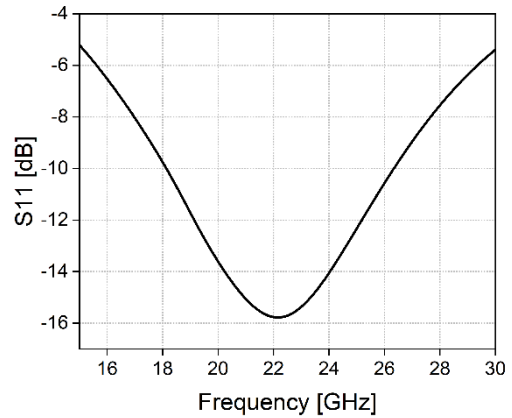


Fig. 7. Measured reflection coefficient at the minimum and maximum frequencies

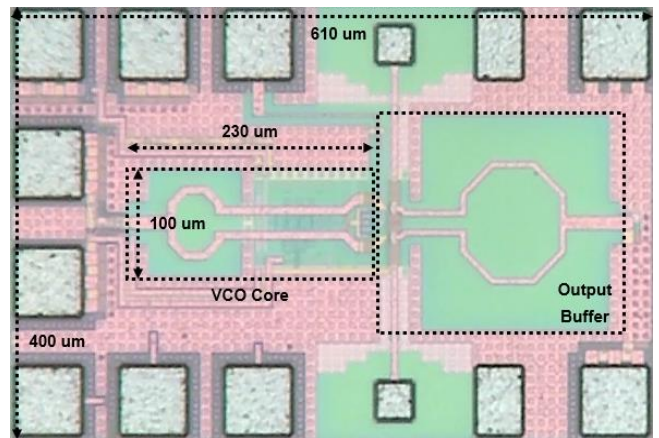


Fig. 8. Die photograph of the proposed VCO

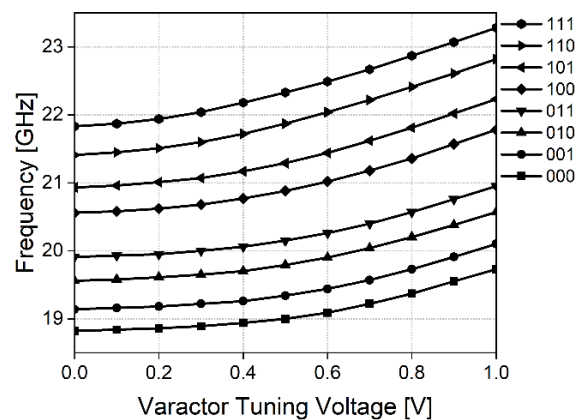


Fig. 9. Measured tuning range of the proposed VCO

overlap within the total given capacitance degrades the overall  $Q$  of the LC tank. Accordingly, the transconductance required to compensate for the tank loss increases, inevitably having larger size for the cross-coupled transistor and the current source which increases power consumption. Therefore, it is necessary to reduce the proportion of total capacitance so that the high  $Q$  of the designed inductor is meaningful.

IV. CONCLUSION

A tunable LC VCO using the 3-bit switched capacitor is proposed for wideband performances. By using the MOM capacitor instead of the MIM capacitor, the  $Q$ -factor of the LC tank is improved. A 3-bit switched-capacitor is used to control the resonance frequency without the dead-zone. A tuning range of 21.2% is achieved at the K-band. The VCO operates from 18.82 to 23.28 GHz, and the measured phase

noise is  $-105.8$  dBc/Hz at a 1MHz offset with an output power of  $-1.35$  dBm. The current consumption of the proposed VCO is 24 mA at a supply voltage of 1 V.

TABLE I. Comparison of the proposed VCO specification and other works

|                             | This Work | [7]                 | [8]    | [9]    |
|-----------------------------|-----------|---------------------|--------|--------|
| Technology (nm)             | 65        | 65                  | 65     | 250    |
| Tuning Range (%)            | 21.2      | 20.1                | 9.5    | 25     |
| Frequency (GHz)             | 21.45     | 26.3                | 24.25  | 19.4   |
| Phase Noise @ 1MHz (dBc/Hz) | -105.8    | -121 <sup>†</sup>   | -100.8 | -101.2 |
| FOM (dBc/Hz)                | -179      | -185.8 <sup>†</sup> | -179.3 | -177   |
| FOM <sub>T</sub> (dBc/Hz)   | -185.2    | -191.8 <sup>†</sup> | -179   | -185.3 |

$$FOM = PN - 20 \log_{10}(f_0/\Delta f) + 10 \log_{10}(P_{DC}/1mW) \text{ [7], [10], [11]}$$

$$FOM_T = FOM - 20 \log_{10}(FTR/10\%) \text{ [7], [10], [11]}$$

<sup>†</sup>Average value over the entire frequency tuning range

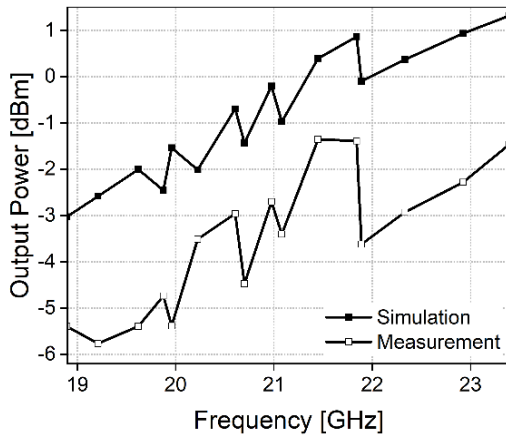


Fig. 10. Output power of the proposed VCO

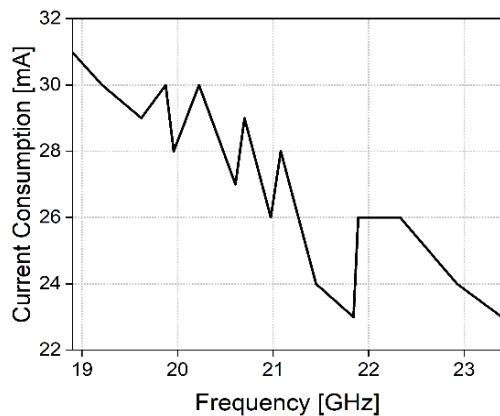


Fig. 11. Current consumption of the VCO core

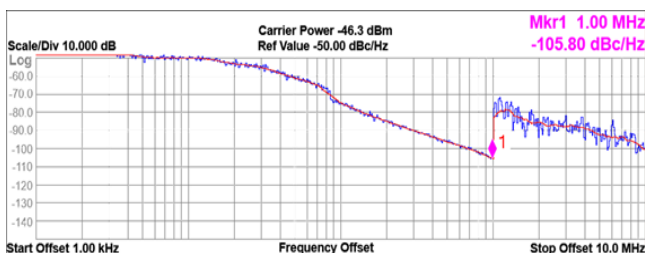


Fig. 12. Measured phase noise at the 1 MHz offset

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. 2021R1A2C2004356). Chip fabrication and EDA tools were partially supported by the IDEC, Korea. The authors thank Joon-hyuk Yoon for checking English corrections.

REFERENCES

- [1] P. Agarwal *et al.*, "Switched substrate-shield-based low-loss CMOS inductors for wide tuning range VCOs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 8, pp. 2964–2976, Aug. 2017.
- [2] X. Liu, Y. Chao and H. C. Luong, "A 59-to-276-GHz CMOS signal generator using varactor-less VCO and dual-mode ILFD," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2324–2334, Aug. 2021.
- [3] J. Zhang, N. Sharma and K. K. O, "21.5-to-33.4 GHz Voltage-controlled oscillator using NMOS switched inductors in CMOS", *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 7, pp. 478–480, Jul. 2014.
- [4] A. Basaligheh, P. Saffari, W. Winkler and K. Moez, "A wide tuning range, low phase noise, and area efficient dual-band millimeter-wave CMOS VCO based on switching cores", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2888–2897, Aug. 2019.
- [5] A. Kral, F. Behbahani and A. A. Abidi, "RF-CMOS oscillators with switched tuning", *Proceedings of the IEEE 1998 Custom Integrated Circuits Conference*, Santa Clara, CA, USA, pp. 555–558, May 1998.

- [6] N. H. W. Fong *et al.*, "A 1-V 3.8 - 5.7-GHz wide-band VCO with differentially tuned accumulation MOS varactors for common-mode noise rejection in CMOS SOI technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 8, pp. 1952–1959, Aug. 2003.
- [7] M. H. Kashani, R. Molavi and S. Mirabbasi, "A 2.3-mW 26.3-GHz Gmboosted differential colpitts VCO with 20% tuning range in 65-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 4, pp. 1556–1565, Apr. 2019.
- [8] W. Tan, T. Wu, Z. Xing, Y. Peng, H. Liu and K. Kang, "A 21.95-24.25 GHz Class-C VCO for 24 GHz FMCW radar applications," *IEEE MTT-S International Wireless Symposium*, Guangzhou, China, pp. 1–3, May 2019.
- [9] B. Jung and R. Harjani, "A 20GHz VCO with 5GHz tuning range in 0.25  $\mu\text{m}$  SiGe BiCMOS," *2004 IEEE International Solid-State Circuits Conference*, San Francisco, CA, USA, pp. 178–521, Sep. 2004.
- [10] S. Lightbody, A. H. M. Shirazi, H. Djahanshahi, R. Zavari, S. Mirabbasi and S. Shekhar, "A  $-195$  dBc/Hz FoMT 20.8-to-28-GHz LC VCO with transformer-enhanced 30% tuning range in 65-nm CMOS," *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 200–203, Jun. 2018.
- [11] Y. Fu, L. Li, D. Wang and X. Wang, "A  $-193.6$  dBc/Hz FoMT 28.6-to-36.2 GHz dual-core CMOS VCO for 5G applications," *IEEE Access*, vol. 8, pp. 62191–62196, 2020.



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His research interests include Millimeter-wave/terahertz circuits Transmitter IC.



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