128-Channel Recording, 32-Channel Stimulation, Digitally Interfaced Optogenetic Neuromodulation System-on-Chip

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***Abstract* - This paper presents a digitally interfaced a 128-channel recording, 32-channel stimulation optogenetic neuromodulation system on chip (SoC) that has been developed for long-term optogenetics neuroscience research. The low-power 128-channel neural recording frontend offers low-noise multichannel recording, on-chip 16-bit data digitization, and electrode impedance measurement. The 32-channel optogenetic stimulator provides high-resolution, accurate optical stimulation. The chip communicates through two control signal shared SPI interfaces for simultaneous recording and stimulation with independent on-the-fly control command and data transfer, resulting in only 6 external wires. The developed system constitutes a fully digital, bidirectional 128/32-channel SoC suitable for *in-vivo* neuromodulation.**

***Keywords*—Application-specific integrated circuit (ASIC), Multichannel neural recording and stimulation, Neuromodulation, Optogenetics**

I. INTRODUCTION

Since the first introduction of optogenetic research in 2005 [1], it has been gaining its popularity in neuroscience community. This technique genetically modifies specific types of neurons to express light-sensitive ion channels, opsins, on their membranes. The light-sensitive channels thus, react to specific wavelength of light to excite or inhibit neural activities. Compared to traditional electrical current, voltage, or charge-based stimulation, the newly introduced optical stimulation is more cell-specific. It also makes simultaneous recording much easier, while the electrical method tends to saturate the recording amplifier or induces huge artifacts that cannot be easily compensated afterwards.

For a complete optogenetic system that enable recording and stimulation simultaneously, there are many design criteria need to be met. The interconnection between blocks, the heat dissipation, and the power and timing distribution are the first challenges to overcome [2], [3]. On top of that, as the application is focused on implantable devices, it becomes increasingly more complicated. Bio-compatible material for the implanted devices is the first necessity to be considered for the safety and long-term recordings with animal-under-test. Temperature change also needs to be closely tracked to maintain a safe environment for the brain cells of the animal- under-test. The system weight is also important. The total system weight, including everything on the system, should be no more than 10% of the animal weight. When the test object is a larger animal, like a rat or a genuine pig, around a 30-gram constraint is applied. However, for smaller rodents like mice, a strict 2-gram system is required [4].

Frontend integrated circuit architectures for multichannel neural recordings to achieve performance for neural recordings while maintaining low-power and small-area consumptions have been extensively researched, each with a specific set of pros and cons [5]–[8]. The ac-coupled architecture may be one of the most widely adopted architectures [9], [10]. It solves the issue of large electrode dc offset (EDO) and provides balanced performance between noise, power, gain uniformity, distortion, and so on. However, the ac-coupled architectures require relatively large physical area to implement EDO rejection. This large area consumption issue in the ac-coupled architectures has been solved by the dc-coupled frontend. It optimizes the circuit area by eliminating the large input capacitor and adopting mixed-signal feedback loops for the EDO suppression, however, with limitations to linearity and noise performance. The dc-coupled direct ADC has come out most recently [11]. The Δ-modulation [12], [13] and switched capacitor (SC)-based direct sampling [14], and the difference differential amplifier (DDA) input stage-based Δ-modulation can achieve a rail-to-rail input range, removing the EDO concern, but with the cost of a high oversampling rate (OSR), *i.e.*, high power consumption, and thereby limiting their applications to very low frequency neural signals, such as electroencephalogram (EEG), intracranial EEG (iEEG), electrocorticogram (ECoG), and field potentials.

It is also important to select an implantable neural stimulator suitable for the given environment. There are many different electrodes available for neural stimulations, resulting in a vast range of potential electrode impedances according to types (*e.g.*, surface or penetrating), geometry and size, and materials. Therefore, the desired stimulation strength can vary a lot, for instance, the electrical stimulation using dc current uses from a few μA for intracortical

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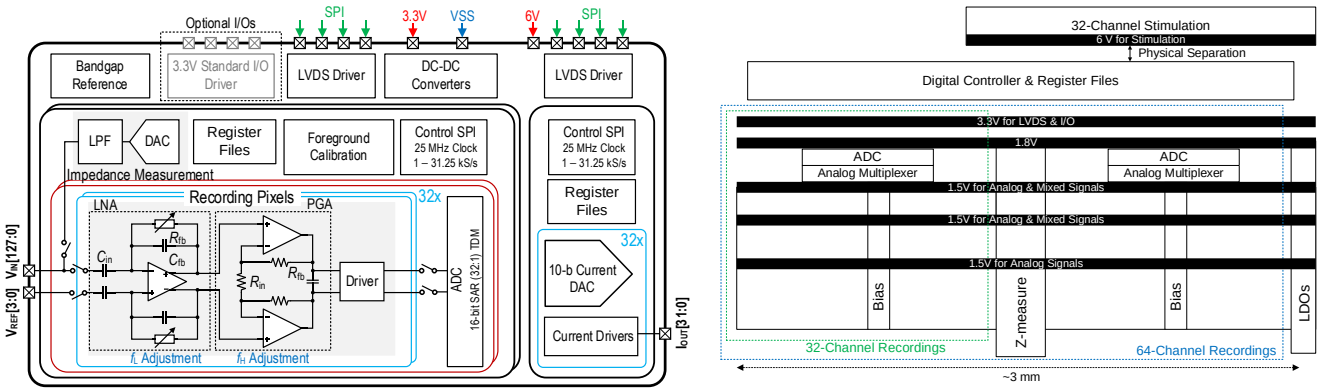


Fig. 1. Proposed 128/32-channel neuromodulation ASIC: (a) ASIC block diagram, (b) Simplified 64-channel floorplan for SoC implementation.

stimulation to a few mA for motor muscle and cortical stimulations, with variety of the requirement of precision, and waveform, and timing. In addition, not only for the electrical current stimulations, but also different stimulators have also been published, such as charge-controlled stimulation and voltage-controlled stimulation [15].

In this paper, a neuromodulation system on chip (SoC) with 128-channel recording and 32-channel optogenetic stimulation has been presented, which is designed for long-term optogenetics neuroscience research. This SoC provides a digitally interfaced, bidirectional, multi-parallel interface to neurons in the brain. This neuromodulation SoC relies on an external processing unit for the closed-loop operation. Even though it has inherently higher latency and power consumption for data transmission than the systems that have on-chip processing and control units, it has greater flexibility, as processing algorithms, such as feature extraction and classification can easily be reprogrammed and adjusted on-the-fly according to the testing environment. In addition, this external processing can relax power constraints on the classification hardware, allowing computationally extensive algorithm can be adopted for better accuracy.

The ASIC provides a 128-channel/32-channel interface to the brain for any processing entity capable of SPI command and data transfer and is therefore easy to employ. To cover many different application scenarios, the SoC is capable of low-noise neural recording in both local field potentials (LFPs) and action potentials (APs) frequency bands with bandwidth adjustments, as well as high-precision stimulation for μLEDs with ~50 dB of dynamic range (DR). A larger channel count can be easily accommodated by the modular, expandable design, which allows controlling several SoCs simultaneously.

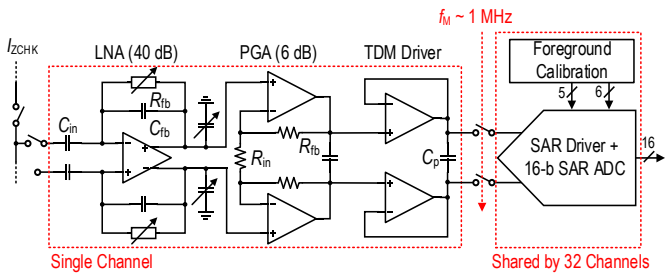


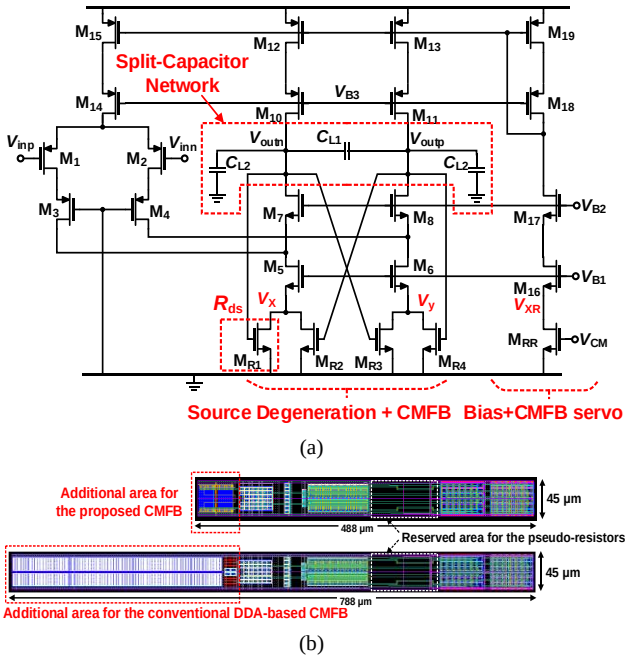
Fig. 2. Block diagram of proposed system integration, including chip and base station side respectively.

II. 128/32-CHANNEL NEUROMODULATION ASIC

Fig. 1(a) shows the proposed application specific integrated circuit (ASIC) architecture for 128-channel recording and 32-channel optogenetic stimulation SoC. The recording ASIC is 32-channel modular, consists of 4 modules to realize the total 128 channels. The stimulation ASIC is also 32-channel modular, only a single module has been implemented with the recording circuit. The SoC includes all necessary references, such as a bandgap reference (BGR), current references (β-multiplier), power rails (1.2, 1.5, and 1.8 V) from the internal low dropout regulators (LDOs), standard SPI I/O, and low voltage differential signaling (LVDS) drivers. Thus, only two supplies, 3.3 V and 6 V dedicated for recording and stimulation, respectively, are required. Fig 1 (b) shows the floor plan for the ASIC. Since the ASIC includes many different functionalities, the careful floorplan is necessary. The recording channel is assigned column-parallel, each occupies 40 μm pitch with 5 μm physical separation (thus, 45 μm pitch for each) and the staggered pads have been employed to accommodate the inputs with such a narrow pitch. As shown in Fig. 1 (b), the single module has its own bias block, 2 modules share a digital controller and a SPI, and 4 modules share the LDOs. For the stimulation ASIC, there is a dedicated SPI and LVDS driver but its control signals, such as CS_b and SCLK, can be shared with the recording circuit. The power rails have been also planned to minimize the inference coupling. As shown, the analog supplies, such 1.2, 1.5 V and the digital supply 1.8 V are separately generated in the bottom and top size, respectively. The stimulation circuits that consume relatively higher peak power than recording circuits has been placed on top of the controller with > 100 μm physical separation.

A. Analog Frontend Circuit for Neural Recording

In this work, the ac-coupled architecture has been implemented to inherit its advantages over the newly developed dc-coupled or direct-ADC architectures, such as excellent gain uniformity across the multiple channels, less design effort due to the well-developed design procedures, inherent passive offset cancellation, and relatively high input impedance, while compensating the high power and large area consumptions with the proposed novel circuit design



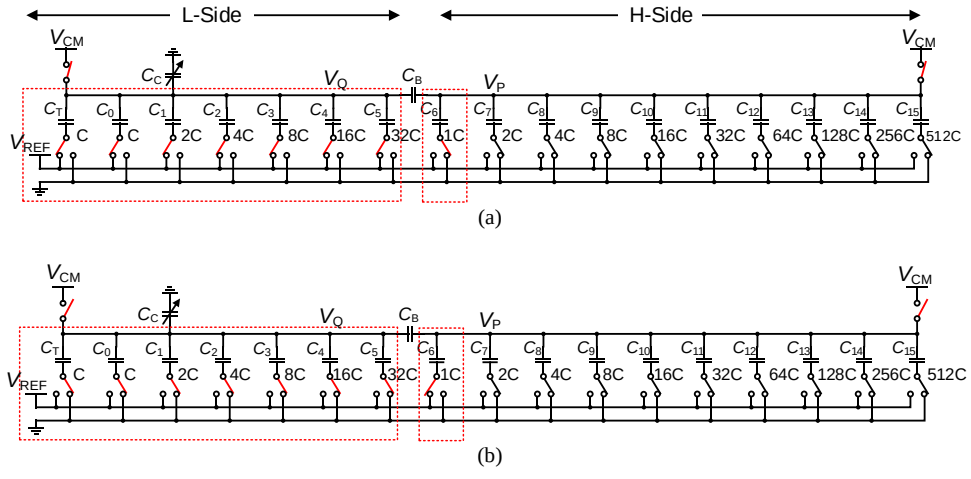
(a)

(b)

Fig. 3. (a) Implemented FC-OTA for the LNA where the source degeneration resistors have been replaced by the transistors and those transistors are re-used for the CMFB operation [16], and (b) the layout comparison with a conventional FC-OTA.

techniques. Fig. 2 shows the analog frontend circuit diagram for neural recordings. The frontend AC-coupled amplifier (LNA) provides a low noise and bandpass-shaped recording. The LNA can adjust the low cut-off frequency (f_L) from sub-Hz to a few Hz and the high cut-off frequency (f_H) from a few kHz with a fixed 40 dB mid-band gain. The f_L is adjusted via the pseudo resistor with a 2-b current digital to analog converter (DAC) and the f_H is changed through the output capacitance (C_L) adjustment. The following programmable amplifier (PGA) has been implemented with non-inverting resistive feedback structure, therefore the combination of the LNA and the PGA looks like a conventional instrument amplifier with 3 amplifiers. The PGA also provides additional f_H adjustment allowing the frontend circuit to be reconfigured to record low frequency neural signals. This can achieve 6 dB gain with high frequency cut-off adjustment from 1 kHz to 15.5 kHz. When considering the bandwidth, the recording channel has a capability to embrace LFPs and extracellular action potentials (APs) simultaneously, those are essential for the in-depth neuroscience research, and can be reconfigured to record ECoG while saving the power consumption. All recording channels have a time-division multiplexing (TDM) buffer to share the 16-b successive approximation register (SAR) ADC. The SAR ADC has been implemented using a split-capacitor array DAC, preamplifier, latched comparator, and control logics. The SAR ADC has two foreground calibration loops, each for the comparator offset and capacitor DAC calibrations.

The conventional circuit topologies have been adopted for the transistor-level implementations in non-critical circuit blocks. For instance, the class AB amplifiers were used for the PGA and driver implementation, and a conventional StrongArm latched comparator and split capacitor (6-10) DAC were employed for the SAR ADC. However, the most critical circuit block, LNA has been carefully realized with newly developed technique because it is one of the most power and area consuming blocks in the neural recording frontend. The implemented operational transconductance amplifier (OTA) for the LNA is shown in Fig. 3 (a), which is based on our previous implementation [16]. The backbone of the OTA is a folded-cascode OTA (FC OTA) that has been widely adopted for neural recording applications due to its favorable characteristics, such low-power and low-noise performance. However, the implementation of this OTA is bulky due to the resistor-based source degeneration and the necessary of the common mode feedback (CMFB) circuit for the fully differential operation. In the current implementation, the area-consuming resistors have been replaced the small transistors (M_{R1-4}), and they are reused for the CMFB sensor. The CMFB servo loop has been realized by the folded cascode branch (M_{5-8}), therefore the additional OTA for the CMFB has been completely removed. In addition, the output capacitor has been split as shown in Fig. 3 (a) to enhance the bandwidth of the common mode loop. Fig. 3 (b) shows the area comparison between the conventional FC-OTA and the implemented FC-OTA, indicating reduction of area and power ~37% and ~11%, respectively, while exhibiting the same noise performance.



(a)

(b)

Fig. 4. Implemented 16-b split capacitor (6 + 10-b) capacitor DAC (CDAC) describing CDAC calibration procedures ((a) and (b))

B. Circuit for 16-b SAR ADC with Foreground Calibration

This work includes two 16-b split capacitor (6 + 10-b) SAR ADCs, each has two separate foreground calibrations. Figs. 4 (a) and (b) shows the capacitor DAC (CDAC) calibration. In the beginning of the calibration, all L-side capacitors are connected to V_{REF} (1111111), and all H-side capacitors are grounded (000000000). Since the calibration capacitor, C_C is initially set to the lowest value in its tunable range, the total weight of the L-side is initially larger than that of the lowest bit in the H-side. Due to the charge conversation in the node V_P, V_P becomes smaller than V_{CM} after the all capacitors in the L-side are switched to the ground (0000000) and the lowest capacitor in the H-side is connected to V_{REF}. The comparator compares V_P and V_{CM} and delivers the results to increase C_C until V_P becomes larger than V_{CM}. Another calibration is for the comparator offset removal. Before the CDAC calibration, the top plates of the CDAC are set to V_{CM} and the body biases of the input pair of the preamplifier shown in Fig. 5 (a) are swept using the resistor DAC (RDAC) shown in Fig. 5 (b). The ratio of the transconductance of the input pair, $M_{1,2}$ (g_m) to the body transconductance (g_{mb}) is ~0.3^{-1}, thus ΔV_{BS} = 15 mV is required to cover the offset of ±5 mV. ΔV_{BS} can be realized by the 7-b RDAC, resulting a LSB of ~117 μV. The unit resistance (R_{unit}) of ~6 Ω has been employed with the reference resistor (R_{REF}) of ~ 77 kΩ. The large resistance distribution, such as 6 Ω to 77 kΩ has been laid out with a unit 60 Ω poly resistor with 10× parallel combinations and 10 segments of 128× series combination (10 × 7.7 kΩ). The static current consumption in the resistor string is ~19.3 μA. For the energy-efficient operation of the SAR ADC, V_{CM}-based switching scheme has been adopted [17]. To generate the necessary V_{CM} (= 1.5/2 V) without using amplifiers, the unit CDAC structure and the control circuit shown in Fig. 6 has been used [18]. To make the converter not to be limited by thermal noise, the total capacitance has been set as > 30 pF, ($2kT/C < 27.6 \times 10^{-9}$ V^2, i.e., 16.6 μV_{rms}) with the given 32.7 μV_{rms} of the least significant bit (LSB). The unit capacitance (C_U) has been set

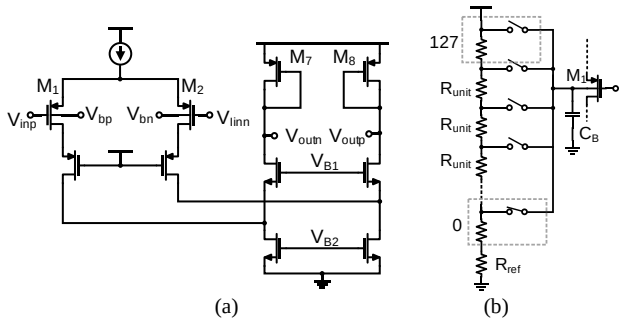


Fig. 5. (a) Preamplifier for the latched comparator, (b) 7-b RDAC for the offset calibration

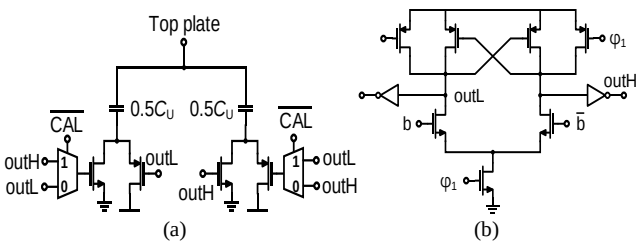


Fig. 6. Unit CDAC: (a), and the controller for the unit CDAC (b).

as 35.6 fF that thus, constitutes the total capacitance of 35.45 pF.

C. Circuit for Electrode Impedance Measurement

To improve system's functionality and safety, monitoring the electrode impedance is helpful. Tissue reactions over long-term recordings can significantly alter the electrode-tissue interface, resulting in changes in electrode impedance, which can affect the recording quality. In addition, the impedance measurement before and after assembly would increase the recording yields. Therefore, tracking of the impedance allows monitoring the electrode condition and enhance the recording quality over time. In this work, the dedicated impedance measurement circuit has been implemented with the recording frontend circuit as shown in Fig. 7. The 8-b DAC receives a sinewave and converts it into a voltage waveform with a full scale of 1.2 V. After filtering, this voltage waveform is converted into a current through the selectable capacitors (0.1, 1, and 10 pF), then applied to the electrode under test. The impedance measurement procedures are controlled in the software where the appropriate scaling capacitor to prevent the saturation in the recording channel is selected and all 64 channels are swept sequentially. The amplified sinewaves are analyzed and the impedance information at a specific frequency (applied through the 8-b DAC) is extracted in the software. To cover all 128 channels in the system, two impedance measurement circuits have been implemented.

D. Digital Control and LVDS drivers

This neuromodulation ASIC has three dedicated SPIs, two for the 128-channel recording and one for 32-channel stimulation. Fig. 8 (a) shows a timing diagram for the SPI commands and data dedicated for recording. The single SPI period is 840.4 ns where 16 SCLKs are toggled with 40.8 ns period. In the digital controller, 5 commands are coded for the foreground calibration, chip reset, data conversion, and register read and write. The 32 SPI periods and 3 auxiliary SPI periods becomes 1 SPI cycle (35 × 840.4 ns), thus > 30 kS/s sampling time is assigned for a single channel recording. The data conversion takes 3 SPI period to decode the conversion command (channel information), to covert the data, and to load the converted data into the SPI format. The 3 auxiliary SPI periods are also assigned for the register read and write, calibration, and chip reset. The single SPI dedicated for the recording basically operates for 32-channel, but it can cover 64 channels without increasing the clock rate by employing double data rate (DDR) technique as shown in

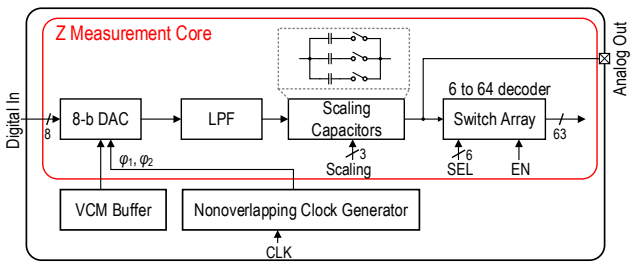


Fig. 7. Block diagram of proposed system integration, including chip and base station side respectively.

Fig. 8 (a). Fig. 8 (b) shows the core LVDS TX (left) and RX (right) drivers. For LVDS operation, a 3.3 V external supply is directly used. To filter out any glitches, a R-C low pass filter (LPF) has been implemented for the input of the TX driver. The threshold reference ($V_{TH,RX}$) for the RX driver has been implemented using 6 PMOS stacks as shown in the right of Fig. 8 (b).

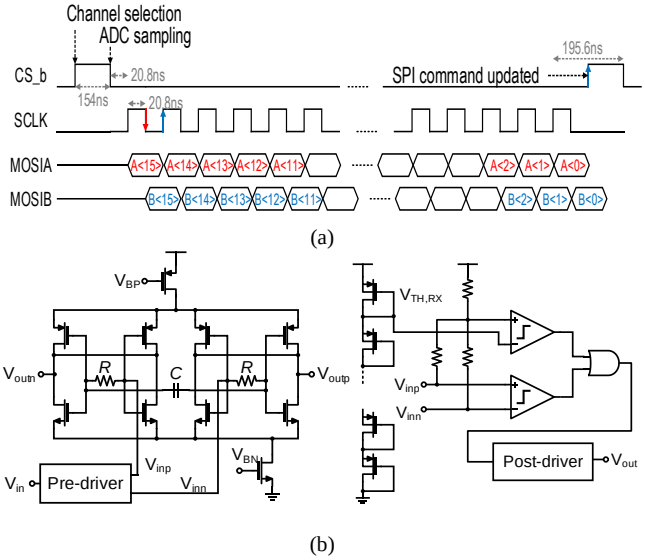


Fig. 8. Conceptual timing diagram for SPI operation (a), and core circuits for LVDS TX (left) and RX (right) drivers.

E. Optogenetic Stimulation

A previous version of the custom optogenetic stimulation ASIC to drive current to the μLEDs on the optoelectrode has been employed [19] with the resolution modification. The stimulation chip consists of 32 current DACs controlled by an SPI-based serial input. The DACs drive the μLEDs with up to 256 μA current with 8-b resolution. The 1 μA current steps provide fine control of emitted optical power while the large output range allows a high optical power option for neural activation in a large tissue volume. The output currents are simultaneously updated at the rate of 11.72 kHz by feeding 32 8-bit values into an input register which controls the output current level for each DAC channel.

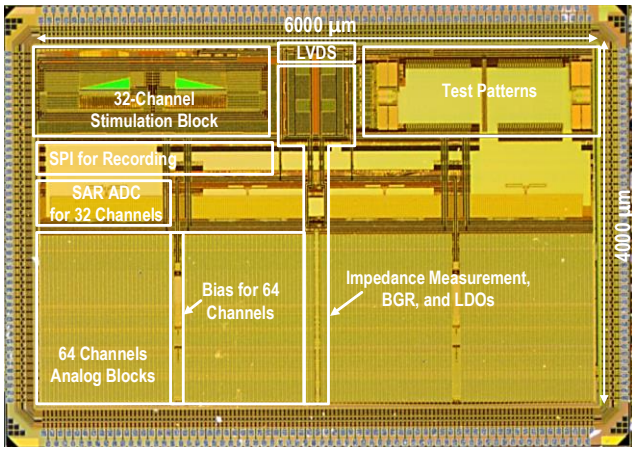


Fig. 9. Die microphotograph for the fabricated neuromodulation ASIC

III. MEASUREMENT

The presented neuromodulation SoC has been fabricated with 180 nm 1P6M CMOS process. The die micro-photograph is shown in Fig. 9 where the important circuit blocks are highlighted. The ASIC occupies 6000 × 4000 μm^2 including test patterns. To accommodate 128 separate inputs and 4 reference inputs toward the single side of the chip (bottom), staggered pads have been employed.

A. Benchtop Test

Fig. 10 shows the frequency response of the fabricated LNA using Agilent 35670A. The mid-band gain was ~39.5 dB. The measured bandwidth of the LNA spans from 0.0227 Hz to 14.642 kHz that can fully embrace LFPs and APs. As shown, f_L and f_H can be programmed from 22.7 to 87.3 mHz (2-b sets: 22.7, 39.8, 60, and 87.3 mHz) and from 12.541 to 14.642 kHz (1.5-b sets: 12.54, 13.55, and 14.64 kHz), respectively. Further f_H adjustment can be made when programming PGA (not shown) with 2-b; 8.0, 10.74, 12.16, 13.34 kHz. Fig. 11 (a) shows the input referred noise (IRN) spectrum of the LNA from 0.4 Hz to 50 kHz. The estimated $1/f$ noise corner was ~180 Hz and the power spectral thermal noise density was ~23 nV/√Hz. The calculated input referred noise (IRN) of the LNA was ~4.11 μV_{rms} from 0.4 to 10.5 kHz. Fig. 11 (b) depicts the transient output noise measurement of the same LNA using a Keysight MSO2004B for 10 seconds, that can cover down to 0.1 Hz. The calculated IRN from the transient measurement was ~4.24 μV_{rms}, which is well matched to the spectral measurement in Fig. 11 (a). The measured total harmonic distortions (THDs) with 105 Hz and 1 kHz sinewaves are also shown in Fig. 12. The calculated THD from the measurement were ~1% for 4.8 mV_{pp} inputs for both cases. Fig. 13 shows the measured signal to noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) up to the Nyquist rate (500 kS/s). The calculated effective number of bit (ENOB) was 12.31 bit at 499 kS/s. Fig. 14 shows the captured LVDS waveforms (MISO2) with a 100 Ω external resistor. The peak-to-peak amplitude was estimated as ~0.35 V with a 1.22 V common mode (CM) voltage while sending data to the host computer with 7m distance. The LVDS output can drive up 7 m of the flexible cable (RHD SPI cable, *Intan Technology*, USA) without bit errors. Fig. 15 shows the comparison between the pre-

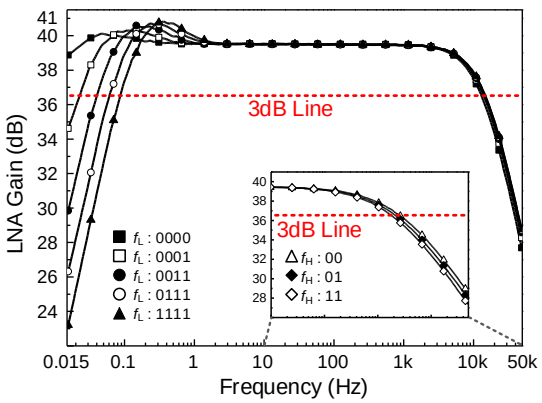
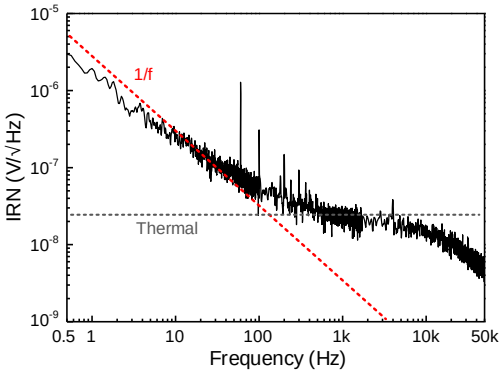
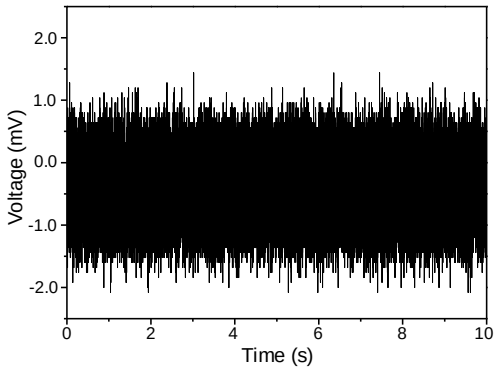


Fig. 10. Measured frequency response of LNA



(a)



(b)

Fig. 11. Measurement noise characteristics: (a) spectral density of input referred noise, (b) transient output noise

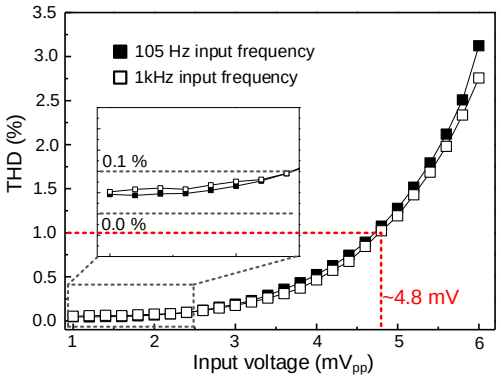


Fig.12. Total harmonic distortion (THD) measurements for 105 Hz and 1 kHz sinewaves.

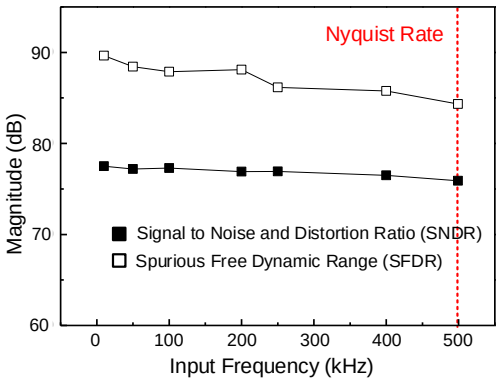


Fig. 13. SNDR and SFDR with various input frequencies.

recoded broadband neural signals (LFP + AP) and the output of the fabricated chip with the pre-recorded neural signals input. To fairly compare, the output has been referred to the input. Fig. 16 (a) and (b) show the dc-sweeping result of the optogenetic stimulator from code 0 to 255 and the calculated DNL (top) and INL (bottom), respectively. The max/min DNLs are 0.38/-0.2, thus there is no missing code. Table I summarizes the measurement results and compares with other state-of-the-art works. The presented work shows the highest level of integration by including all required circuit blocks on chip and has the largest number of parallel recording and stimulation.

TABLE I. Performance Comparison of Neural Interface

	[a][2]	[3]	**This work**
Tech. [nm]	180	180	180
Recording ASIC			
No. of Ch.	32	16	128
Area/Ch. [mm²]	0.46	0.1	0.1312
Power/Ch. [μW]	11.8 (LNA)	9 (LNA)	13.2 (LNA)
IRN [μVrms]	3.8/3.3 (LFP/AP)	4.57	4.1
ADC	I-ΔΣ	V-ADC	16-b SAR
Resolution (bit)	16	10	16
ENOB	12.1	9.1	12.3 (worst)
f_L (Hz)	0.2	0.3	0.02 – 250
f_H (kHz)	7.5	7	7.6 – 13.4
Sampling freq. (kS/s)	20	1000/250 (CC/CV)	31.25 (variable)
Supply Voltage (V)	1.8	5	3.3
Stimulation ASIC			
No. of Ch.	32	16	32
Area/Ch. [mm²]	-	0.013	0.09
Power/Ch. [μW]	-	-	975 @ 100 μA
Resolution (bit)	-	6	8
Min. Current [μA]	-	-	1
Supply Voltage	±9	5	6
Stimulation Type	Electrical	Electrical	Optical
Others			
[b]PMU	N	N	Y
Z-Measurement	N	Y	Y

[a] Recording and Stimulation ASIC were integrated in one channel
[b] Power management unit

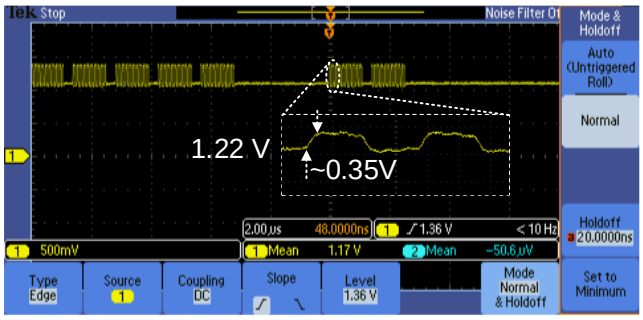


Fig. 14. Picture of the captured oscilloscope screen for LVDS measurement

B. In Vitro Test

Before *in vivo* testing, the recording quality of the fabricated ASIC has been characterized *in vitro* setup. A custom silicon neural probe connected with the ASIC has been dipped in phosphate buffered saline (PBS) with the reference and ground connections. A set of pre-recorded

neural signals (recorded from motor cortex in a rat) then has been applied through PBS solutions. The schematic of the *in-vitro* testing setup is shown in Fig. 17 (a). The ASIC has been configured with the highest bandwidth to simultaneously record both LFP and AP signals and the recorded data has been collected using a customized USB-based interface board (XEM6010, OpalKelly, USA) and transferred to the host computer for further processing. The recorded raw data is shown in the top Fig. 17 (b). For better visualization, the raw neural signals have been bandpass filtered (3rd-order Butterworth, f_P = 0.8 – 7 kHz, f_S < 0.6, > 8 kHz) using a commercial software (MATLAB, MathWorks, USA) and the resulting APs are shown in the bottom of Fig. 17 (b). An inset in Fig. 17 (b) depicts the enlarged ~80 ms of the LFP and AP.

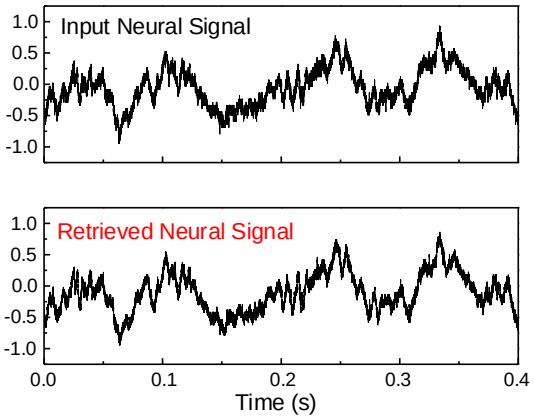


Fig. 15. Prerecorded broadband neural signal (top) and the retrieved neural signal by this neuromodulation ASIC (bottom).

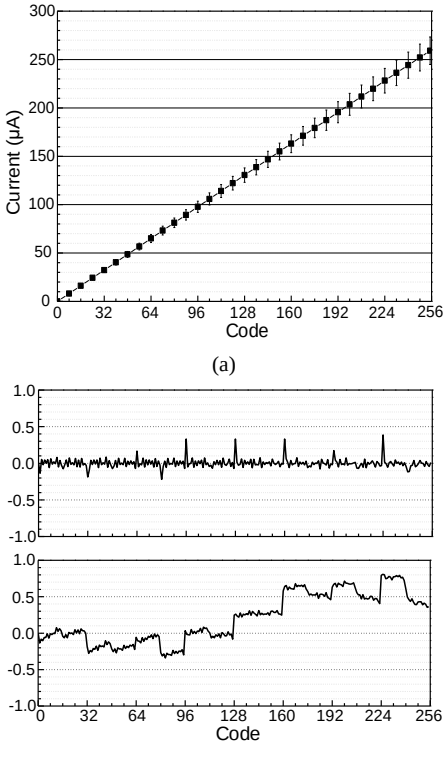


Fig. 16. DC-sweep from code 0 to 255 for the optogenetic stimulator (a), and DNL (top) and INL (bottom) (b).

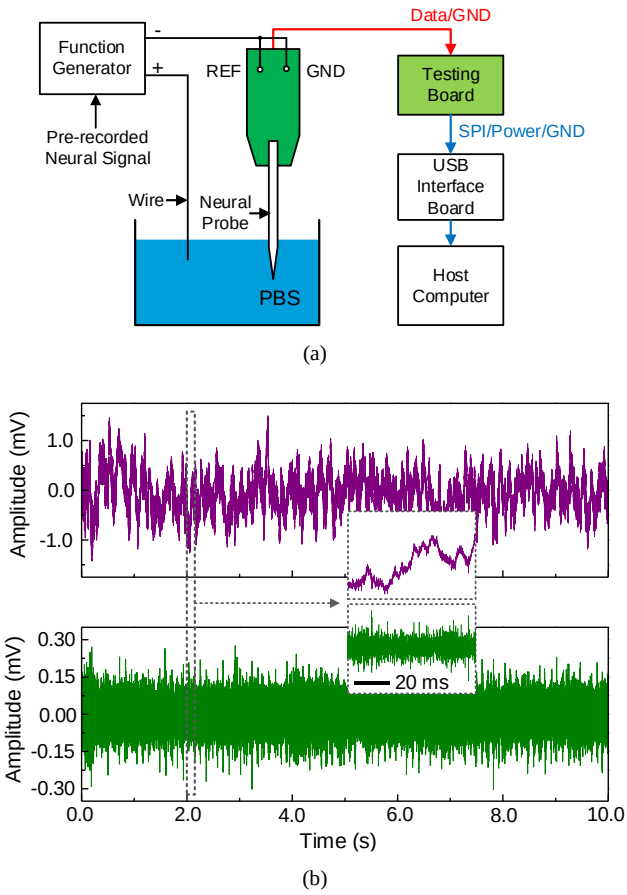


Fig. 17. Schematic of the *in vitro* setup: (a) and retrieved raw data (top) and (b) filtered APs (bottom).

IV. CONCLUSION

The on-chip integration of a 128/32-channel neuromodulation SoC for long-term optogenetic neuroscience research has been presented. The presented SoC consists of low-power, low-noise 128-channel neural recording frontends and high-precision 32-channel optogenetic μLED drivers. The recording frontends offer 128-channel simultaneous recording, on-chip data digitization with 16-b resolution, and on-the-fly electrode impedance measurement, and the optogenetic drivers provides 32-channel simultaneous 8-b driving current with 1 μA resolution. The neuromodulation SoC communicates with a host computer using two SPI interfaces for recording and stimulation. Since the control signals for the SPIs can be shared, only 6 pins are required for the operation.

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