A WR3.4 x12 Frequency Multiplier Chain Based on InP HBT Technology

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***Abstract* – In this work, a x12 frequency multiplier chain has been developed in a 250-nm InP HBT technology for operation in the WR3.4 frequency band. The multiplier chain is composed of three frequency multipliers: a V-band frequency tripler, a D-band frequency doubler, and a WR3.4 frequency doubler. The V-band cascode frequency tripler exhibited a maximum output power of 0.83 dBm with a bandwidth of 59 - 72 GHz, while the D-band bootstrapped Gilbert-cell frequency doubler showed a maximum output power of 6.13 dBm with a bandwidth of 140 - 164 GHz. With the WR3.4 push-push frequency doubler, a maximum output power of 0.5 dBm was obtained with a bandwidth of 278 - 325 GHz. The fully integrated multiplier chain exhibited a saturation output power of 1.6 dBm at 300 GHz and a peak conversion gain of -3.6 dB at 3.5-dBm input power. The circuit operated over a frequency range of 246 - 318 GHz with up to 4.3-dB in-band output power variation. The total DC power consumption was 131mW.**

***Keywords*—250-nm InP HBT, Frequency multiplier**

I. INTRODUCTION

Recently, the terahertz frequency band, roughly ranging from 100 GHz to 10 THz, has been attracting lots of interests in various applications for scientific and engineering fields such as imaging, spectroscopy, radio astronomy, radar applications, and communication systems. Especially, the THz frequency band can be used as the carrier frequency for the wireless communication, making it possible to achieve a data rate higher than 100 Gbit/s when a frequency band above 300 GHz is employed. However, the terahertz band shows a high atmospheric absorption (mainly due to water vapor and oxygen). Hence, when a long-distance wireless link is needed, frequency bands avoiding attenuation peaks such as the frequency band around 300 GHz need to be selected. As the practical aspects become more important in the application of THz frequency band, planar semiconductor-based THz systems are gaining increasing attention because of their advantages of small form factor, low power dissipation, low cost, and so on.

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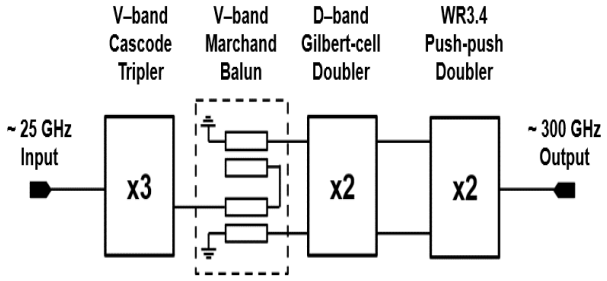

Fig. 1. Block diagram of the WR3.4 x12 frequency multiplier chain.

One of the essential elements for the THz wireless communication systems is the high performance THz signal sources. On-chip oscillators can be utilized for the generation of high-frequency signals. Although such an approach benefits from the fact that no separate external signal source is needed, it is still challenging to realize on-chip oscillators with low phase noise, low jitter, and high output power. On the other hand, frequency multipliers driven by a high-quality signal source that operates at a lower frequency can alleviate the drawbacks of the on-chip oscillators. Key performance matrices required for frequency multipliers operating at THz band are high output power and wide bandwidth. For this, increasing number of frequency multipliers have been recently reported based on various techniques in the THz frequency band [1-7].

It has been challenging to realize semiconductor-based circuits operating over 300 GHz because of the high frequency performance limitation of transistors. However, recent development of semiconductor technologies have made THz circuits possible. One example is the 250-nm InP HBT technology used in this work, which enable circuit performance well over WR3.4 frequency band with its f_t and f_{max} being 350 and 650 GHz, respectively. Also, the devices show high BV_{CEO} of over 4 V, which is advantageous for high-power performance. The process provides four metal layers including a 3-μm thick Metal 4 layer, which is important to achieve low-loss passive devices including transmission lines at high frequency operation. This technology also offers thin-film resistors of 50Ω/sq, metal-insulator-metal capacitors of 0.3fF/μm^2, and backside vias. Based on this technology, a WR3.4 x12 multiplier chain which consists of a V-band tripler, a D-band doubler, and a WR3.4 doubler is developed in this work, aiming at enhanced output power and bandwidth.

The developed x12 frequency multiplier chain converts single-ended input signals around 25 GHz to single-ended output signals in the vicinity of 300 GHz, a part of WR3.4 band (220 – 325 GHz). The frequency multiplier chain consists of three cascaded frequency multipliers based on different topologies: V-band cascode frequency tripler, D-band bootstrapped Gilbert-cell frequency doubler, and WR3.4 push-push frequency doubler. In addition, a V-band Marchand balun is inserted after the cascode tripler to convert single-ended signals to differential signals to drive the D-band doubler. The block diagram is shown in Fig. 1. The first step that needs to be determined in the multiplier design is the circuit topology. There have been various topologies available for high-frequency multipliers [1-2] [8], and a proper topology should be selected that best fits for the application in terms of the operation frequency and the harmonic order. Also, matching networks need to be selected, which play an important role for suppressing the unwanted harmonics and while maintaining the desired signal component.

The remaining part of this paper is composed of following sections. In Section II – Section IV, the circuit design and measurement for each of the unit frequency multipliers are described, while those for the integrated WR3.4 x12 frequency multiplier are presented in Section V. Lastly, the conclusion follows in Section VI.

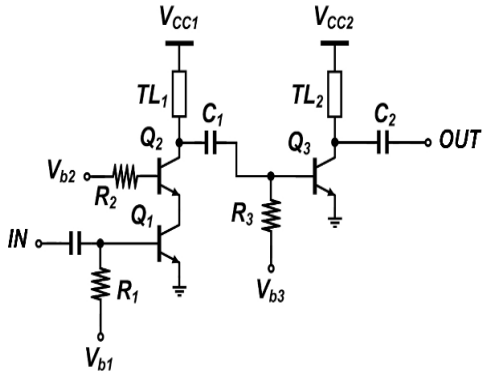

Fig. 2. Schematic of the V-band cascode frequency tripler.

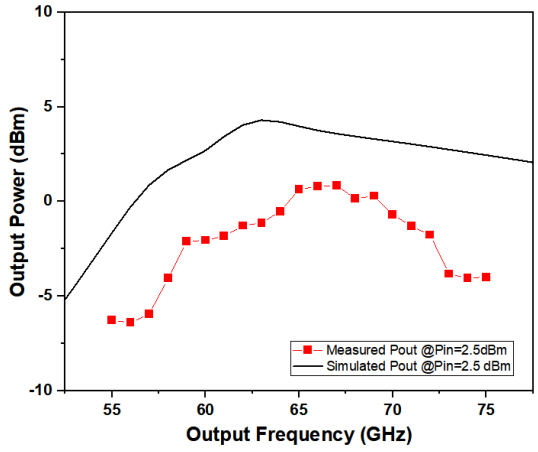

Fig. 3. Simulated and measured output power vs. output frequency of the V-band cascode frequency tripler at input power of 2.5 dBm.

II. V-BAND CASCODE TRIPLER

The V-band cascode frequency tripler converts single-ended signals around 25 GHz to single-ended signals in the V-band near 75 GHz. As shown in Fig. 2, the cascode tripler consists of a cascode stage for x3 multiplication followed by a common-emitter amplifying stage. In the front stage, both fundamental and third harmonic frequency signals are amplified by the cascode transistors. As the input power grows, the power of third harmonic frequency signal increases more rapidly than that of the fundamental frequency signal. However, since the cascode stage itself is an amplifying stage, there arises a strong leakage of the fundamental-mode signal to the stage output, which needs to be effectively suppressed. In this multiplier, the fundamental-mode and other unwanted harmonic signals are filtered by the interstage matching network comprising a short stub TL_1 and a series capacitance C_1 with a small value. The same method of impedance matching using short stub TL_2 and a capacitor C_2 is used at the output of the common-emitter amplifying stage for further suppression of the fundamental frequency signal.

The V-band cascode frequency tripler was measured with a DC to 40-GHz coaxial probe, a V-band waveguide probe, and a V-band power sensor. Fig. 3 shows measured output power against the output frequency at input power of 2.5

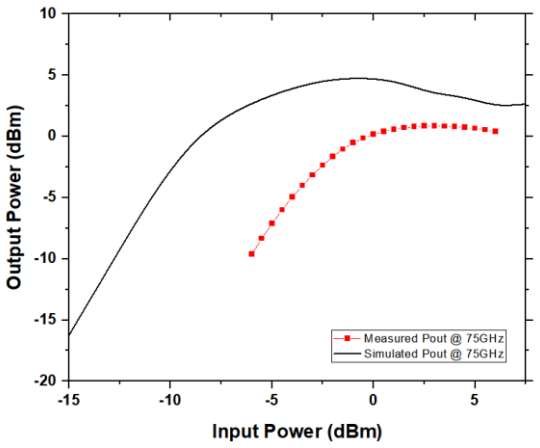

Fig. 4. Simulated and measured output power vs. input power of the V-band cascode frequency tripler at 75 GHz.

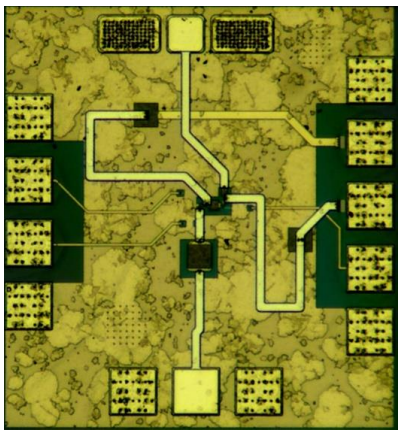

Fig. 5. Chip photo of the V-band cascode frequency tripler.

dBm, together with the simulation results. The measured maximum power is 0.84 dBm at 67 GHz, with a 3-dB bandwidth of 59 – 72 GHz. Compared to simulated values, the measurement shows slightly smaller output power and bandwidth. The linearity performance is shown in Fig. 4, which shows simulated and measured output power against the input power at fixed output frequency of 75 GHz. The maximum measured output power is 0.83 dBm, in comparison with the simulated value of 4.7 dBm. The difference between measured and simulated results is due to mismatched input impedance. The mismatched input impedance of the total frequency multiplier can be changed dependent to measurement setting. The chip photo of the fabricated V-band tripler is shown in Fig 5. The total size of chip is 618 x 671 m^2 including DC and RF pads.

III. D-BAND BOOTSTRAPPED GILBERT-CELL DOUBLER

The D-band bootstrapped Gilbert-cell frequency doubler converts differential signals around 75 GHz to differential signals in the D-band near 150 GHz. Fig. 6 shows the schematic of the D-band bootstrapped Gilbert-cell frequency doubler developed in this work. The operation of the Gilbert-cell frequency doubler is based on a pair of differential-mode mixers that performs the self-mixing, leading to x2 frequency multiplication. In order to drive the Gilbert-cell frequency doubler, a V-band Marchand balun is inserted at the front to convert the single-ended output signals of the preceding cascode tripler to differential signals. The signal from the balun is amplified by transistors Q_1 and Q_2 before reaching the doubler. For the suppressions of the harmonics of the amplified signal, a pair of small capacitors (C_5 and C_6) is added in shunt with the emitters of Q_3 - Q_6. One of the challenges in the design of Gilbert-cell doublers is to obtain balanced differential output. It is difficult to simultaneously achieve both amplitude and phase balances at the output with the Gilbert-cell configuration [9]. In this work, 90° phase difference was imposed between TL_5 (TL_8) and TL_6 (TL_7) to address this issue. The input and output large-signal *S*-parameters of the doubler is matched to differential 100 ohm for the maximum power delivery.

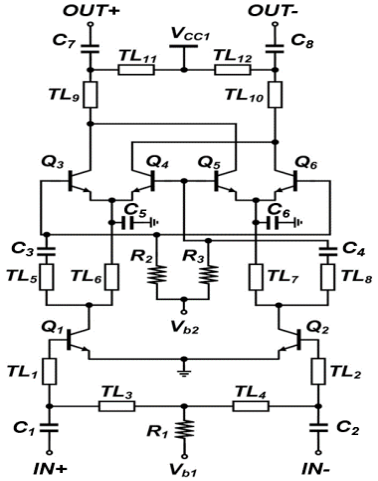

Fig. 6. Schematic of the D-band bootstrapped Gilbert-cell frequency doubler.

The characteristics of the D-band frequency doubler are presented with simulation only due to the difficulty in the measurement of differential signals. For the output power harmonic balance simulation, the input and output of the D-band bootstrapped Gilbert-cell frequency doubler was terminated with differential 100 ohm. Simulated output power vs. output frequency of the D-band doubler at -3dBm of input power is shown in Fig. 7. The simulation result indicates that the D-band frequency doubler has a 3-dB bandwidth of 140 – 164 GHz and the maximum output power of 6.13 dBm at the output frequency of 150 GHz. Fig. 8 presents the output power of the D-band frequency doubler swept against the input power with a fixed frequency of 150 GHz. The maximum output power is 6.3 dBm at input power of 0 dBm.

IV. WR3.4 PUSH-PUSH DOUBLER

The schematic of the WR3.4 push-push frequency doubler is shown in Fig. 9. A D-band marchand balun is attached at the front of the WR3.4 doubler to convert single-ended D-band signals into differential D-band signals to drive the push-push frequency doubler stage. The push-push frequency doubler converts the differential D-band signals which comes from the D-band marchand balun to the single-ended signals around 300 GHz. As shown in Fig. 9, the push-

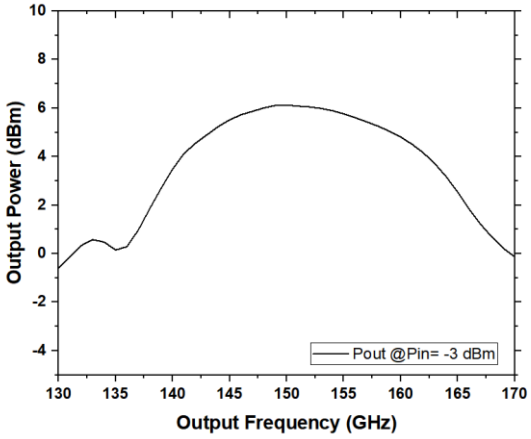

Fig. 7. Simulated output power vs. output frequency of the D-band bootstrapped Gilbert-cell frequency doubler.

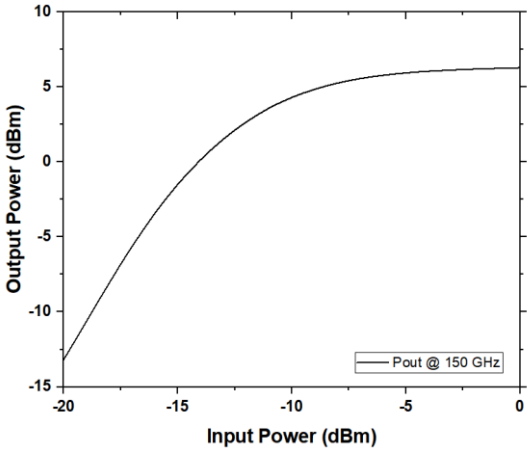

Fig. 8. Simulated output power vs. input Power of the D-band bootstrapped Gilbert-cell frequency doubler.

push frequency doubler consists of a differential transistor pair Q_1/Q_2 with a shared collector node. Q_1 and Q_2 are differentially driven, and the harmonic signals generated from the transistor nonlinearity are combined at the common collector node. At this node, the even harmonic signals are reinforced while the odd harmonics are cancelled out, due to the nature of the differential topology. The final selection of the harmonics is carried out by the output matching network, which is designed to filter out unwanted harmonics while maintaining a certain level of bandwidth by employing a single stub matching with TL_4.

The WR3.4 push-push frequency doubler is characterized with a D-band waveguide probe with a D-band signal source for input power injection, and a WR3.4 waveguide probe that leads to a VDI Erickson PM5 power meter (PM5) for output power measurement. Fig. 10 presents the simulated and measured output power shown as a function of the output frequency of the doubler. The simulated bandwidth of the frequency doubler is 267 - 325 GHz, while the measured bandwidth is 278 - 325 GHz. The simulated and measured output power of frequency doubler swept with the input power is shown in Fig. 11. The maximum measured output power at 300 GHz is 0.5 dBm, which is 2.8 dB smaller than the simulated output power at the input power of 7dBm. However, as indicated by the plot, the measured output power is not fully saturated due to the limitation in the available input power, and it may increase further with a stronger input drive. The chip photo of the fabricated WR3.4 push-push frequency doubler is shown in Fig. 12, and the total size of chip is 459 x 700 μm^2.

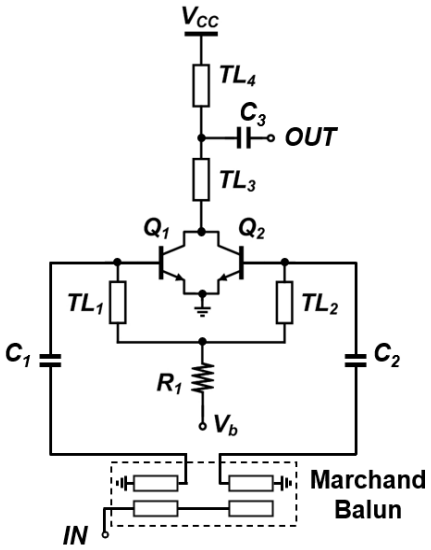

Fig. 9. Schematic of the WR3.4 push-push frequency doubler.

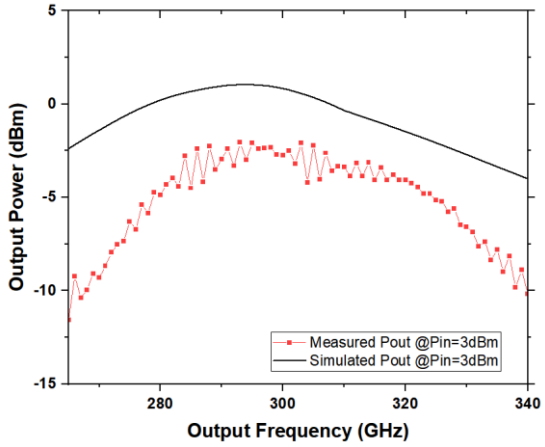

Fig. 10. Simulated and measured output power vs. output frequency of the WR3.4 push-push frequency doubler.

V. WR3.4 X12 FREQUENCY MULTIPLIER CHAIN

The designed x12 frequency multiplier chain was fabricated in Teledyne 250-nm InP HBT technology. The chip photo is given in Fig. 13. With the input signal injected through a DC to 40-GHz coaxial probe, the output power was measured with a VDI Erickson PM5 power meter (PM5) through a WR3.4 waveguide probe.

The measured output power of the multiplier is presented in Fig. 14, for which the input power was set to 9 dBm as was needed to saturate all three multiplier stages. Also included in the figure are simulation results with two different input power levels for reference. The measurement shows that the multiplier chain operates over an output frequency range of 246 – 318 GHz. The wide operation range was helped by the intended frequency mismatch between multiplier stages. One can observe a fluctuation in the mid-band, which arises from

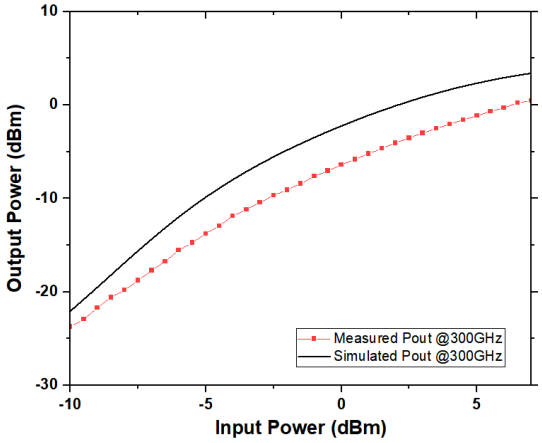

Fig. 11. Simulated and measured output power vs. input power of the WR3.4 push-push frequency doubler.

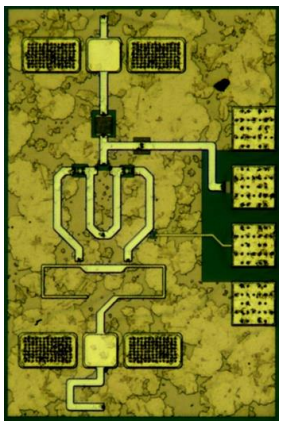

Fig. 12. Chip Photo of the WR3.4 push-push frequency doubler.

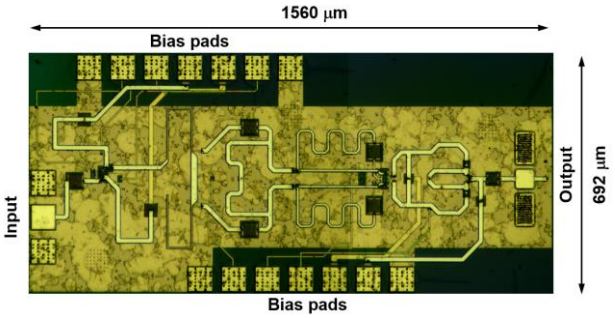

Fig. 13. Chip photo of the fabricated x12 frequency multiplier chain.

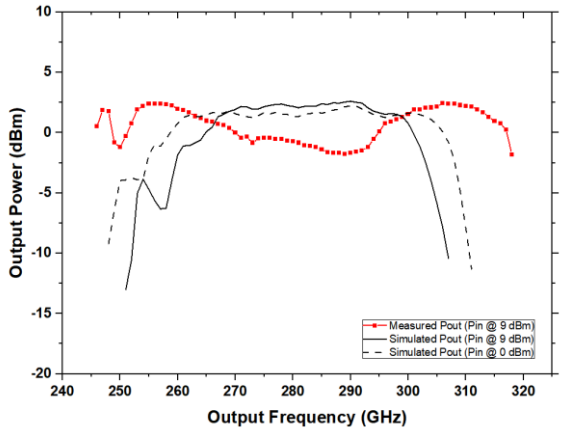

Fig. 14. Simulated and measured output power vs. output frequency of the frequency multiplier chain.

a slight red-shift and reduced bandwidth of the 1st stage tripler measured output that disturbed the designed frequency alignment. It resulted in increased operation frequency range, but caused response variation slightly off the 3-dB boundary. The measured output power maintained values beyond -1.8 dBm, the maximum reaching up to 2.5 dBm. The saturation output power and the conversion gain of the circuit measured at 300 GHz are shown in Fig. 15 with the input power level swept from 1 to 10 dBm. It shows a saturation power of 1.6 dBm and a peak conversion gain of -3.6 dB at the input power 3.5 dBm. To verify the sufficient suppression of unwanted harmonics, the output power spectrum of the multiplier chain was simulated with the input signal of 25 GHz as shown in Fig 16. It is observed that a suppression higher than 23.4 dBc (against $6f_0$) was obtained. The multiplier chain consumed 131 mW in total, which is divided into 51/52/28 mW for each of 1st/2nd/3rd stage. Table I compares this work with previously reported multiplier chains operating beyond 200 GHz.

VI. CONCLUSION

A WR3.4 x12 multiplier chain has been developed in a 250-nm InP HBT technology. All the individual blocks of the frequency multiplier chain were characterized with measured and/or simulated data. The V-band cascode frequency tripler showed a bandwidth of 59 – 72 GHz and maximum output power of 0.83 dBm by measurement. The D-band Gilbert-cell frequency doubler exhibited a simulated bandwidth of 140 – 164 GHz and maximum output power of 6.13 dBm. The WR3.4 push-push frequency doubler displayed a measured bandwidth of 278 – 325 GHz and the maximum output power of 0.5 dBm. Finally the integrated x12 frequency multiplier chain showed a measured saturation output power of 1.6 dBm and a peak conversion gain of -3.6 dB at 300 GHz, with a 5-dB bandwidth of 246 – 318 GHz. It is expected that the multiplier chain can serve as a wideband high-power signal source for various WR3.4 applications when properly driven by an external signal source.

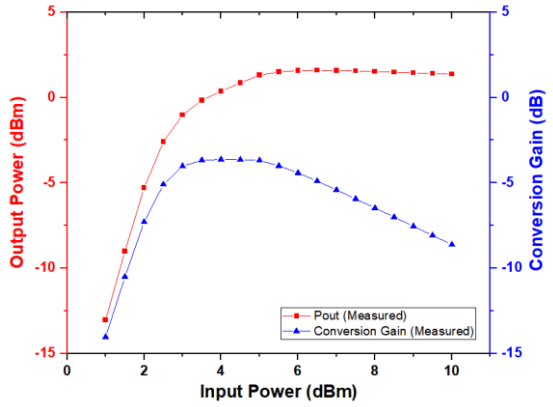

Fig. 15. Measured output power and conversion gain vs. input power of the frequency multiplier chain at output frequency of 300 GHz.

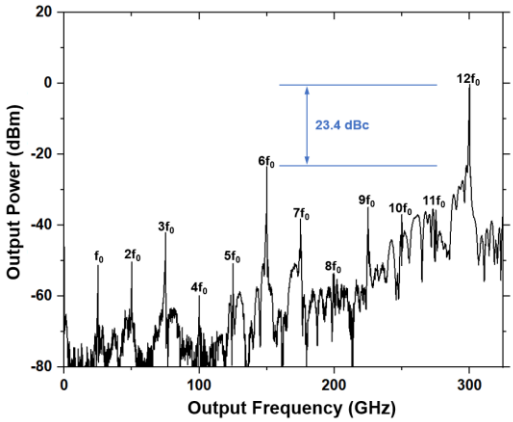

Fig. 16. Simulated output power vs. output frequency. Input frequency (f_0) is 25 GHz ($12f_0$ = 300 GHz) at 9-dBm of input power.

TABLE I. Comparison of frequency multiplier chains above 200 GHz

Technology	circuit	BW/ GHz	P_{out}	P_{DC}	Ref
0.13-mm SiGe HBT	x18 + 2 amp	317 – 328	-3	420	[1]
0.13-mm SiGe HBT	x16	235 – 275	-6	300	[3]
0.13-mm SiGe HBT	x8	210 – 291	-7.7	0.24	[4]
35-nm GaAs HEMT	x8 + 3 amp	220 – 320	2.5	-	[5]
25-nm InP HEMT	x18 + 4 amp	310 – 345	8	445	[6]
0.8-mm TS InP DHBT	x4	280 – 330	-7	40	[7]
250-nm InP HBT	x12	246 – 318*	1.5	131	This

*5-dB bandwidth

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