Design of a Low Power Transmitter for Biomedical Application in 180nm CMOS

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***Abstract* - In this study, we propose a low-power transmitter system for biomedical applications. In particular, it aims at the development of a low-power transmitter targeting a capsule endoscopy among biomedical applications. It is necessary to transmit about 4 pictures per seconds for 8 hours for accurate endoscope. However, due to the limitation of the battery, it is difficult to transmit 4 pictures per seconds for 8 hours with a general battery. Therefore, by making a low-power transmitter, we improve the accuracy of the wireless endoscope regardless of the capacity of the battery. The proposed transmitter is consisted of counter-assisted digital PLL (Phase Locked Loops) and digital PA(Power amplifier) that consumes lower power than analog PA. The currently targeted low-power transmitter is a transmitter capable of 16 QAM modulation in order to have a data rate of 20Mbps at the frequency of the ISM band (433 ~ 435 MHz) and supply voltage is 1V for low power. This system was designed with TSMC Mixed-Signal RF 0.18um process.**

***Keywords*—16QAM, Biomedical, Capsule endoscopy, Low power, Transmitter**

I. INTRODUCTION

In recent years, interest in capsule endoscopes has been increasing. In the case of the existing endoscope, the patient has to endure pain and side effects, since the tube had to be inserted into the body to proceed with the endoscope. However, through the capsule type endoscope, an environment has been created in which the person receiving the endoscope can comfortably receive the endoscope and escape the difficulties.

In the case of a capsule endoscope, a high-definition picture is transmitted outside the person's large intestine, small intestine, and internal organs for about 8 hours per procedure. Also, for accurate medical treatment, high-definition pictures must be sent out as much as possible. In order to do so, a lot of power consumption is inevitably required, which means that the endoscope's battery has to be large. Therefore, the capsule is inevitably enlarged, which can adversely affect the body of the capsule type endoscope.

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In this work, we propose a low power transceiver operating at high data rate, and thus enable accurate diagnosis with the transceiver system by transmitting high-quality pictures outside the human body for more than 8 hours. The type of transmitter to be proposed is as shown in Fig. 1, and it is largely composed of Counter-assisted Fractional N PLL[1],[2] and Digital power amplifier[3].

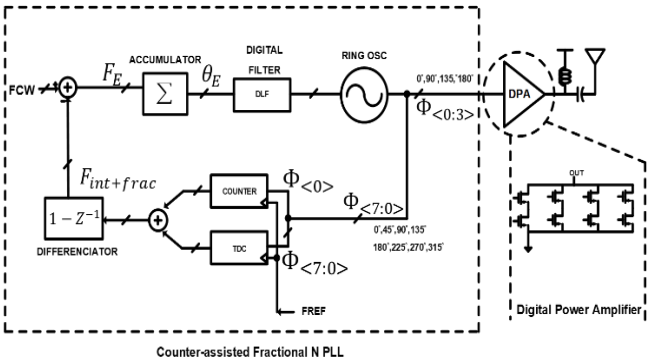


Fig. 1. Overall Architecture of Proposed Transmitter system

II. IMPLEMENTATION

A. Counter-assisted Fractional N PLL

In order to make a low-power transmitter, the overall structure of the transmitter must be simplified to reduce power consumption elements. Also, the power consumption of Phase Locked Loop(PLL) and Power Amplifier(PA), which account for the largest proportion of the power consumption of the transmitter. So, research is needed to reduce the amount of electricity.

In this system, Counter-assisted PLL that does not need a divider was used compared to general PLL which requires a divider. (Fig. 2) [4],[5],

In the case of a PLL that requires a divider, Delta-Sigma Modulation (DSM) must be used to generate the desired frequency, and this increases the output noise of the PLL. Since the noise characteristic of the PLL must be good for 16QAM modulation, a noise canceling circuit must be added to remove this noise, which increases the total power consumption of the entire PLL. On the other hand, since the PLL used in the proposed transmitter does not require a divider and DSM, it not only reduces power consumption due to simplification of the structure, but also reduces noise

caused by DSM.

Also, this system was designed to fractional PLL that makes multiple of fractional value of reference clock. Since Reference clock is 18MHz and wanted output frequency is 435MHz, we select fractional PLL architecture.

B. Digital Power Amplifier

In order to reduce power consumption of PA, digital PA was used. In general, analog PA used to modulate 16 QAM is divided into a phase multiplexer that selects a phase and an amplitude control circuit that controls the amplitude of the output signal of PA. Phase and power control circuit consume power independently. On the other hand, in the case of a digital PA, power consumption is lower than that of an analog PA by combining a part that can be used jointly among a phase multiplexer and an amplitude control circuit.

III. CIRCUIT DESIGN METHOD

A. Time to Digital Converter (TDC)

Resolution of the TDC required to create the desired frequency of the current PLL should satisfy about 20ps. In general, the resolution of TDC is created through a delay chain, but in the TSMC 180nm process, the 1 delay time of the inverter is about 100ps, so it was difficult to satisfy the value with the delay chain. So, a small delay was created using a varactor capacitor using nMos FET, and the desired TDC 1bit resolution could be created using that value.

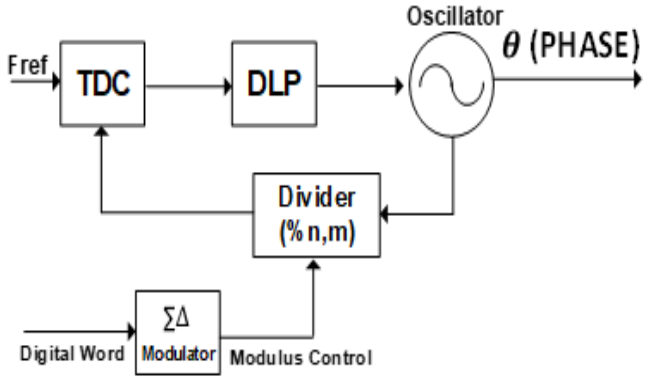


Fig. 2. Fractional N PLL using delta-sigma modulator

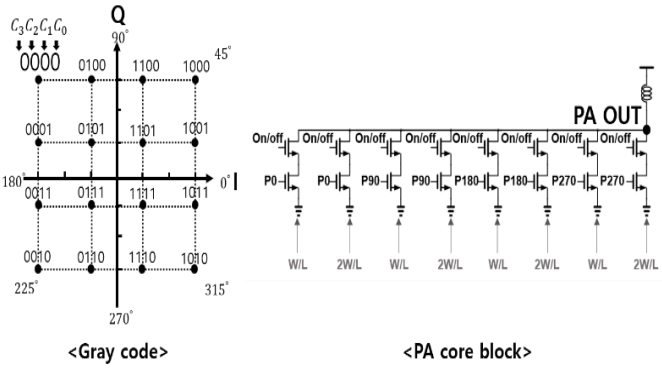


Fig. 3. 16 QAM constellation and PA core block

B. Digitally Controlled Oscillator (DCO)

Oscillator is a circuit that directly creates the desired frequency in the PLL and has a great influence on the overall noise characteristics of the PLL. The designed oscillator is a ring oscillator. The oscillator used for RF communication can be largely divided into an LC oscillator using an inductor and a ring oscillator using a delay cell. Each has its own advantages, but the transmitter currently under development must enter a capsule endoscope, and, as mentioned above, size can also be an important issue. In the case of a ring oscillator, it has the advantage that it can be implemented in a smaller size than that of an LC oscillator, so it is intended to use a ring oscillator. The overall block of the ring oscillator is shown in Fig. 4.

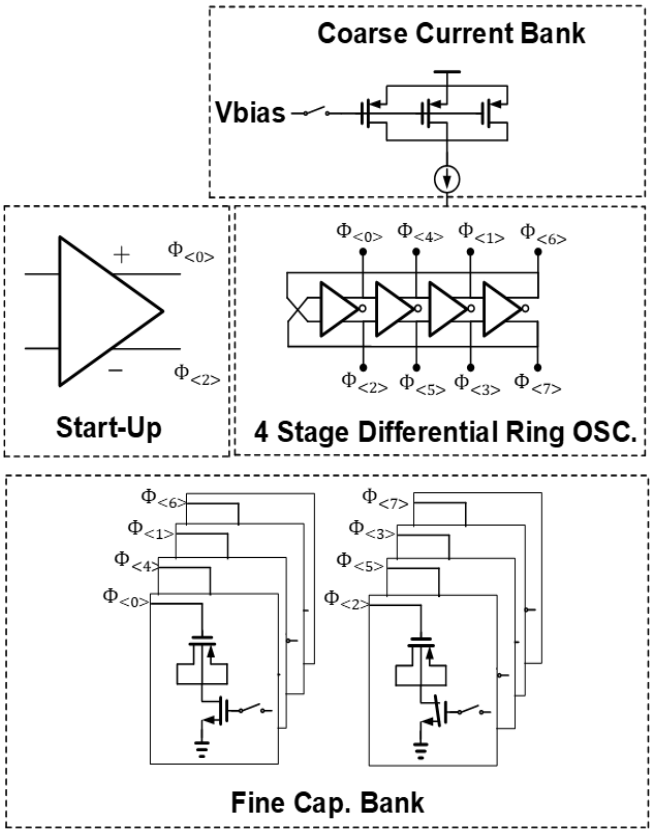


Fig. 4. Overall block of Ring DCO

To explain the above block, the first 4 stage ring oscillator was made using a delay cell, and the reason for using 4 stages is that it needs 4 outputs with 90 degrees difference.

Second, the fine cap bank was made using a varactor cap. To make the desired PLL bandwidth, a frequency change amount of 100Khz per 1LSB is required. To make this frequency, a 0.5fF capacitor is required, and the smallest mim cap in the process is larger than this value, so it was implemented using a varator cap. 100Khz frequency was changed by turning on and off the switch under the varactor cap.

Third is the current bank for coarse lock. In the case of coarse lock, since the frequency range is wide and the chip size must be increased to change this range using a capacitor, we tried to make the chip size smaller by changing the

frequency using the current, not the capacitor.

Finally, explain the start-up circuit. In the case of an even-order ring oscillator, there is a probability that it can theoretically go to a point where oscillation cannot occur. [6] In order to overcome this shortcoming, when the first circuit is operated, it is possible to oscillation by artificially giving the voltage difference between the two nodes.

The DCO frequency resolution used in this system can be divided into two categories. The first is fine resolution using varactor capacitor and the second is coarse lock resolution using current bank. In the PLL lock procedure, at first narrow the frequency range using coarse lock, and then create the correct frequency through fine lock. Fine lock resolution is 100Khz and coarse lock resolution is 1.7MHz. And PLL lock range is from 415MHz to 480MHz.

As mentioned above, the noise properties of DCO have a great influence on the properties of the entire PLL. Currently, the characteristics of DCO are as shown in Figure 6. Phase noise was -71.4 dBc/Hz at 100KHz offset, -98.7 dBc/Hz at 1MHz offset, flicker corner frequency was 30KHz, and cycle jitter was 3ps.

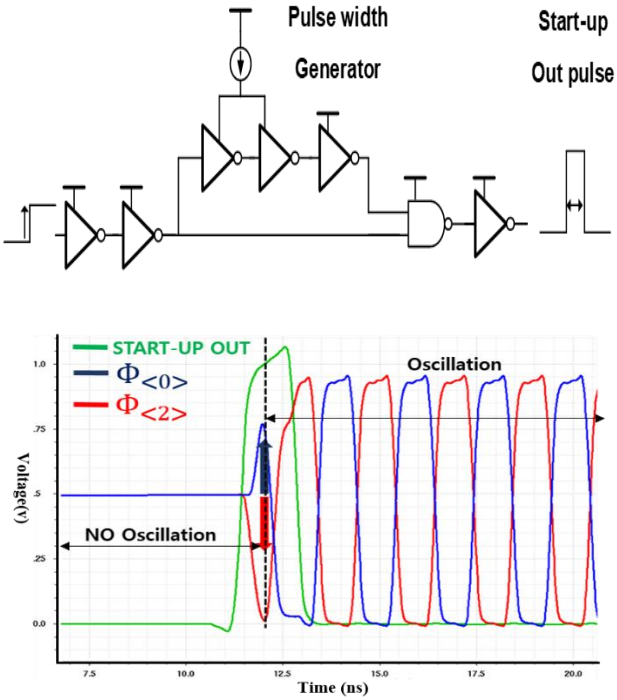


Fig. 5. Start-up circuit and sinario of oscillation

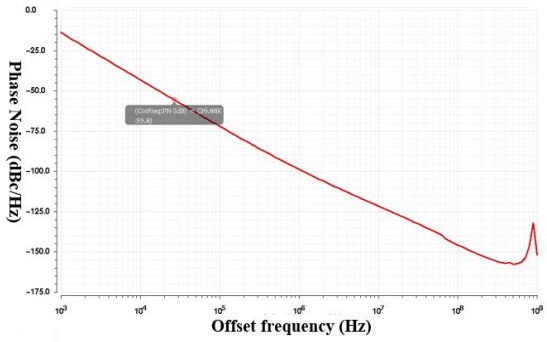


Fig. 6. Phase noise of the DCO in cadence simulation

IV. RESULTS AND DISCUSSIONS

A. Simulation Results using MATLAB

The PLL system is verified using matlab. In the case of matlab, there are two main methods. One is code and another is simulink. The verification method using code is a method of verifying by converting a non-linear circuit into a linear method. It has the advantage of being able to quickly check, but it may differ from the actual circuit in terms of accuracy. On the other hand, the method using Simulink takes longer and has higher complexity than the code, but it also includes non-linear characteristics, so more accurate results can be obtained. The result obtained using matlab code is shown in Fig. 7 below.

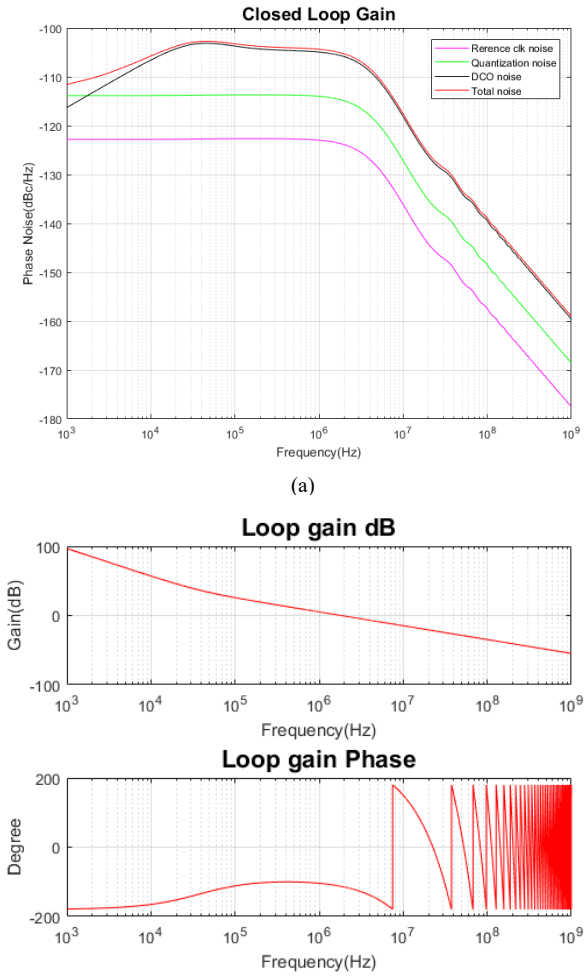


Fig. 7. PLL phase noise using code (a), PLL loop stability using code (b)

As can be seen from the simulation results through the matlab code above, the PLL is a negative feedback system, so stability check is essential. Through the current code simulation, it was confirmed that it has a phase margin of about 60 degrees. Through this simulation, expected in-band noise is about -105 dBC/Hz, bandwidth is 3MHz. After first checking the PLL system by code simulation, simulation was performed using Simulink for more detailed confirmation. The results are attached to Fig. 8 below. In-band noise of simulink simulation is -105dBc/Hz and bandwidth is about

5MHz. When the phase noise value obtained through Simulink is converted into degrees, it is about 0.8 degrees, and the maximum noise value for 16QAM modulation excluding PA amplitude noise is less than 6.5 degrees.

PA noise is check using cadence simulation. As a result, the expected EVM value of PA is less than 5%, and when converted to degree, it is about 3°, and this value is adjustable for 16 QAM even if it is summed up with PLL noise. It can be seen that there is no problem in performing modulation. Fig.9 is post simulation result using cadence for changing amplitude when code is changed.

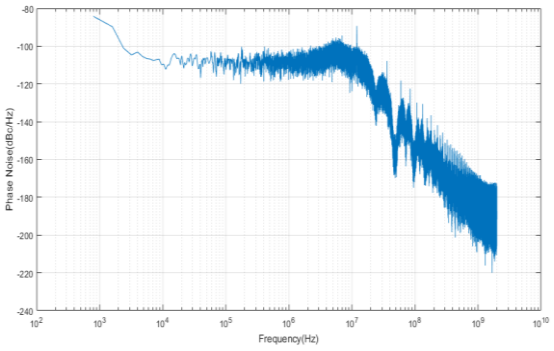


Fig. 8. PLL phase noise using Simulink

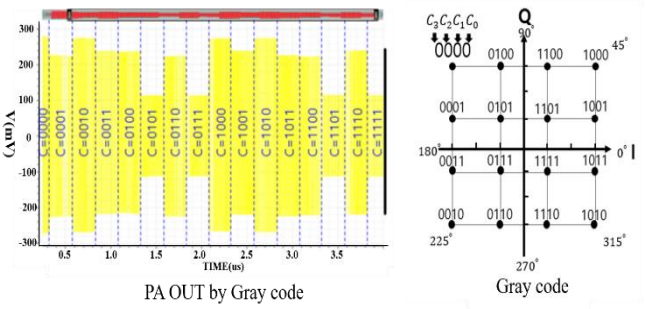


Fig. 9. PA amplitude variation simulation using cadence

B. Chip result

Fig.10 shows the measurement setup. Using computer and arduino, setting digital parameter in chip. and PLL out is measured using signal analyzer. Signal generator is used for generating PLL reference clock. The PLL chip test result is shown in Fig. 11. Fig.11(a) represents the frequency step. frequency step in measurement is 140Khz when reference clock is 18MHz. This value is same as expected value. Fig.11 (b) is phase noise of PLL. Expected value of in-band noise is about -105dBc/Hz. But measurement result has big difference than expected value using matlab. Difference between simulation and measurement value is about 30dBc/Hz. And adding noise seems to be random noise like a TDC quantization noise. Theoretically, in order to obtain the above value, if a value of several MHz is randomly generated, the result can be obtained as shown in the figure 11 above. Expected problem is Timing issue of digital loop filter. When output of digital loop filter is wrong value, this wrong value goes into DCO input. That means frequency variation is occurred.

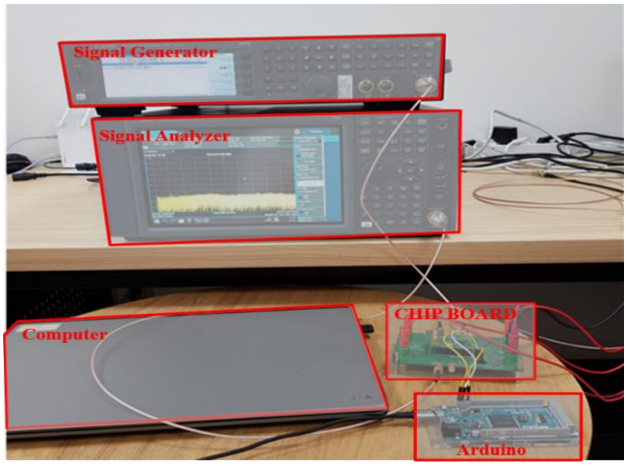
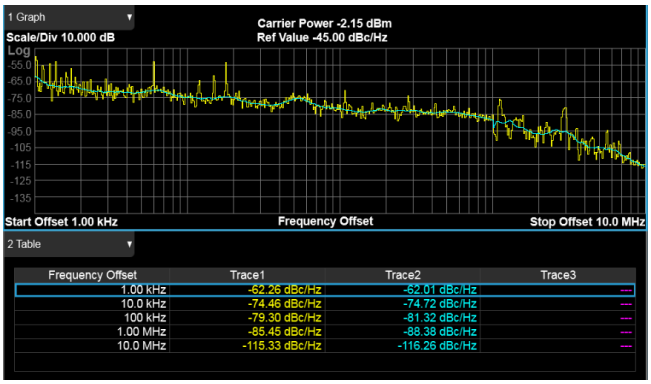


Fig. 10. Measurement setup

(a)



(b)

Fig.11. Measurement of frequency step of PLL (a) Phase noise of PLL (b)

This problem makes PLL unlocked. After the PLL is unlocked, it goes back to the lock and this happens randomly. This randomly repeated lock and unlock phenomenon makes In-band noise worse than expected. To solve this problem, more reliable verification is needed in the circuit simulation stage.

PLL is composed of many blocks, and it handles higher frequency than general circuits. so PLL simulation takes a lot of time. To reduce this simulation time, when running a simulation, it is often predicted and a certain part is omitted. In the case of this simulation, when performing the post extraction simulation, only the capacitor was extracted and simulated without extracting the resistance.

The reason for this is that the resistance value added only the delay in the version where only the capacitor was

extracted, and it was determined that there would be no problem with the operation sufficiently because it operates in digital overall.

Since all blocks could not be extracted at once, the whole simulation was performed by cutting them into TDC, DCO, and DLF and connecting them to the testbench after each extraction. At this point, it is predicted that the above phenomenon will occur due to an unexpected timing issue. Table 1 shows specifications of designed PLL.

TABLE I. Performance of PLL

Parameters	Value
Process	18MHz
Supply	1V
Frequency band	415 ~ 480MHz
Phase noise at 250KHz	-85dBc/Hz
Current	4.5mA
Power consumption	4.5mW

C. Chip layout

Fig.12 shows the top layout of designed transmitter. The chip area is 1300um X 1000um.

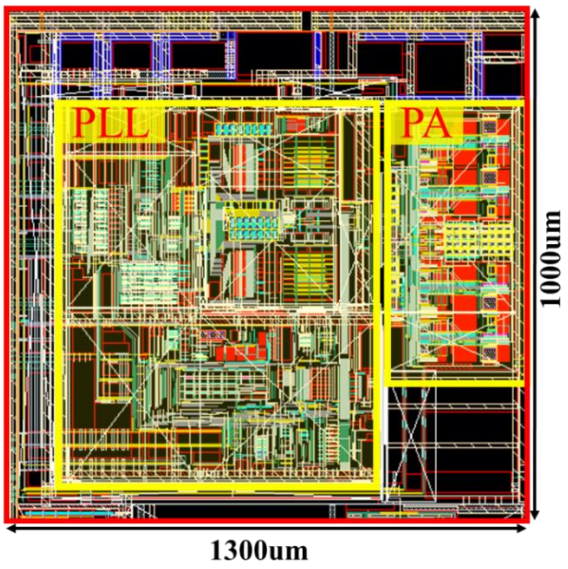


Fig.12. Chip layout of proposed transmitter.

IV. CONCLUSION

Through the capsule type endoscope, the patients can get out of the pain and side effect that can be experienced with conventional endoscopy. However, in order for the capsule endoscope to be as accurate as a conventional endoscope, it must guarantee a high date rate to export high-quality pictures taken inside the human body. Also, the capsule endoscope cannot accommodate a large capacity battery due to its size limitation. Low power design should be applied to operate more than 8 hours

This study tried to reduce power consumption by using counter-assisted fractional N PLL and digital power amplifier for high date rate and low power design of 20Mbps and achieve 16QAM noise performance for 20Mbps. However, due to the timing issue of the PLL digital stage, in-band noise was worse than expected, making it difficult to achieve the target 16QAM, but it would be a good study if a new system was constructed and the debugging point was modified

ACKNOWLEDGMENT

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