Design of a low noise analog Front-End System for Sonar Signal Conditioning Receiver

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***Abstract* - This paper presents the design of a low noise analog front end system for sonar signal conditioning receiver with Parallel to Series Interface in very noisy environments. When measuring distances in the ocean through sonar, the input signal level to the receiver can change drastically depending on the distance between the transmitter and objects. Thus, a receiver with low sensitivity and a wide dynamic range is proposed in this work. In order to minimize the Input-Referred (IR) noise for the high sensitivity of the receiver, a low noise pre-amplifier is proposed and implemented, ultimately achieving a noise of 11 nV/√Hz at 50 kHz. The decimation factor of the digital filter placed after the SDM in the SD ADC can be controlled so as to reduce the power consumption. Through the use of these techniques in the SD ADC, we can implement reconfigurable sampling rates from 1.5 MS/s to 12.5 MS/s with low power consumption. In order to overcome the limitation of the number of pins for sensor application, a Parallel-to-Serial (P2S) interface is proposed and designed in the receiver. The Low Noise receiver in this paper is implemented in a 0.18 µm CMOS process and the die area is 14.44 mm2. The total power consumption of this chip under a supply voltage of 2.4 V is 46.8 mW. The measured sensitivity and dynamic range are -100 dBV and 100 dB, respectively. The measured SNDR at the output of the SD ADC is 82.02 dB when the input signal frequency and sampling frequency are 7 kHz and 6.25 Msps, respectively.**

***Keywords*—Band pass filter, Low noise, Parallel-to-serial interface, Receiver, Sigma-Delta ADC, Sonar sensor**

I. INTRODUCTION

Sonar systems have been widely used to measure distances between objects in the ocean, and they have been actively studied from various perspectives such as sensor modeling and signal processing of the ultrasonic signal. The environment has many noise sources and the receiver is exposed to all of these noise sources. The presence of all of these noise sources in the ocean environment degrades the performance of the receiver. In the sonar system environment, requires a receiver with low noise, and the Input-Referred (IR) noise should be lowered so as to improve the Signal-to-Noise Ratio (SNR) and sensitivity of the receiver. On the other hand, as the distance between the object and the Receiving equipment is shortened, the input signal level of the receiver will increase, which can lead to nonlinear harmonic distortion in the receiver.

In order to process the data from sonar sensors, the sonar signal conditioning receiver requires a pre-amplifier, Variable Gain Amplifier (VGA), filter, and Analog-to-Digital Converter (ADC). As the amplitude of the signal from the sonar source is dependent on the distance between the sonar source and receiver, the receiver should have a wide dynamic gain range, low noise, and a high signal to noise ratio (SNR). In addition, in order to process small and large input signal levels depending on the distance, high dynamic range and Automatic Gain Control (AGC) are required. In this paper, SDM uses variable sampling rates in order to lower the power consumption. Moreover, for the object detection in the ocean environment, the signal is processed in the time domain, and the timing resolution is critical because the sonar system requires many samples in the time domain. For the processing of many samples in the analog front-end, a high data rate is required. The recent trends are focusing more on sensor arrays than single sonar sensors. Sensor arrays can be advantageous in terms of reducing the area and lowering costs accordingly [1-3]. In this paper, we propose a receiver with a low noise pre-amplifier and wide dynamic range for sonar sensors.

The pre-amplifier in the proposed receiver has a low IR noise of 11 nV/√Hz at 50 kHz. It can also apply the DC bias point of 1.2 V to the external sonar sensors, since they do not have the DC bias voltage required for proper MOSFET operation. A receiver takes a signal from each sensor of the sensor array and processes it in a single channel. For a sensor array, a technique integrating the separate multichannel circuits for signal processing is essential. The proposed receiver also includes the Sigma-Delta ADC (SD ADC) with reconfigurable decimation factor, and the sampling frequency can be varied with the oversampling ratio (OSR). In this paper, we propose and design a five-channel low noise receiver with SD ADC with a reconfigurable sampling rate of 1.5 MS/s – 12.5 MS/s.

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II. PROPOSED LOW NOISE ANALOG FRONT END

A. Low Noise Analog Front End (AFE) Architecture

Since the ocean measurement environment requires the use of a low noise receiver due to the presence of various noise sources, one of the most important issues is increasing the signal-to-noise ratio (SNR) in the high-resolution receiver. In order to increase the SNR, it is necessary to first lower the noise level of the input signal to the ADC as shown Fig 1. SD ADC is implemented to achieve high resolution for the high sensitivity sonar sensor application by applying variable oversampling and a chopping scheme in the amplifier. In addition, the Sigma-Delta Modulator (SDM) in the SD ADC uses the clock splitting technique and adopts a digital filter with an adjustable decimation factor for a reconfigurable sampling frequency. A Parallel-to-Serial (P2S) interface is integrated for a multichannel receiver due to the limitations of the pins. The SPI Controller is designed to control the gain of IC according to the input signal level.

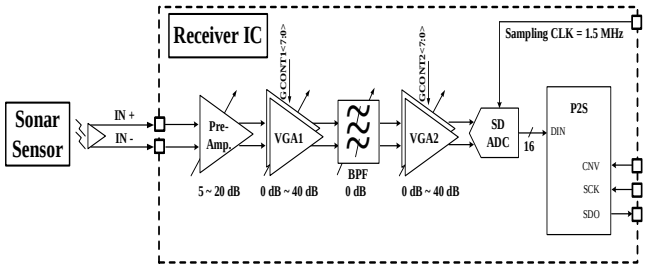

Fig. 1. Block Diagram of Low Noise Analog Front End(AFE) Architecture

B. Pre-Amplifier

. In the receiver proposed in this paper, the pre-amplifier is designed to lower the noise power for high SNR at the output of the ADC. In general, the IR noise of the pre-amplifier dominantly determines the noise performance of the whole receiver. Therefore, in order to design a receiver with low noise, it is important to minimize the IR noise of the pre-amplifier. In addition, the pre-amplifier suppresses the noise from VGA1 and BPF by providing a gain of 20 dB. A schematic of the pre-amplifier is shown in Fig. 2. The low noise structure is implemented by controlling the bias current of the pre-amplifier, and the low power operating mode and the low noise operating mode are selected.

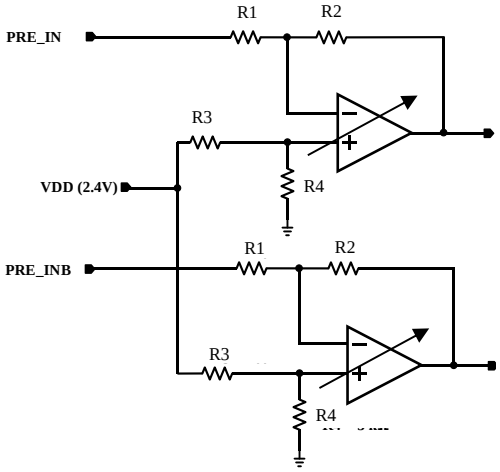

Fig. 2. Schematic of pre-amplifier.

As shown in Fig. 3, presents the noise simulation result of the pre-amplifier, showing the noise of 11 nV/√Hz at 50 kHz.

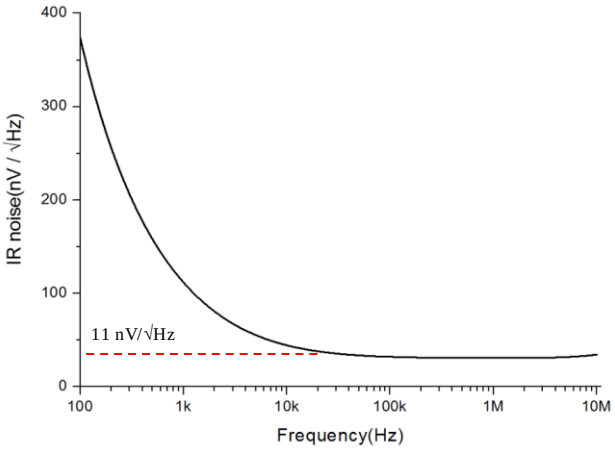

Fig. 3. Simulation Result of pre-amplifier.

C. Variable Gain Amplifier

In sonar application, receiver have many choices for amplifying incoming fine signals. In case of too much amplification, the signal saturation occurs, so we need to detect the magnitude of the incoming signal, select the gain according to the detected signal, and pass it to the next stage. As shown in Fig. 4, the design was carried out to select gain of 5 dB to 20 dB. After the measurement result, it was confirmed that the gain of 5 dB to 20 dB is amplified even when the voltage of 100 mV is applied. Further, our proposed design is to be adjustable using a resistive feedback structure by 1-dB step control depending on the input signal level. As the signal amplitude grows, a lower gain is provided in order to satisfy the input voltage range of the SD ADC.

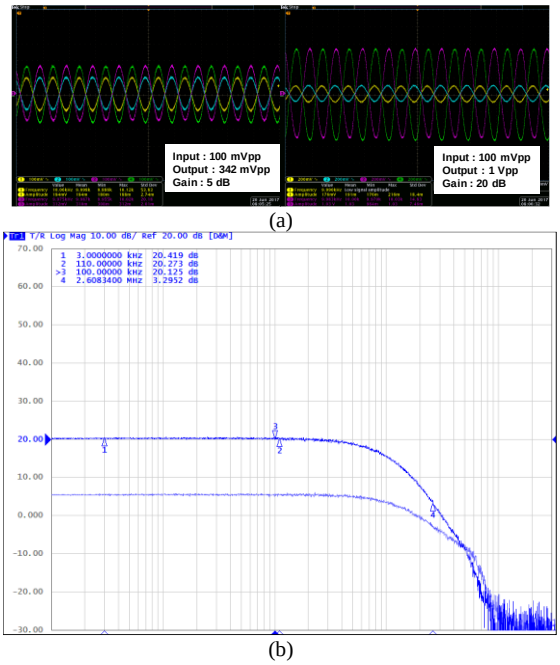

Fig. 4. VGA measurement result (a)using oscilloscope (b)using Network Analyzer

D. Variable Gain Amplifier

An Active-RC Band-Pass Filter (BPF) is implemented in the proposed receiver in order to cancel the dc offset and suppress noise at high frequency. In sonar applications, a band pass filter is required in a very narrow band, and a lot of noise and different frequencies are input depending on the surrounding objects, and thus a band pass filter is needed to remove fine noise from the surroundings. Therefore, a band pass filter suitable for sonar applications needs a band pass filter that maintains a flat band and has high attenuation in the pass band. A schematic of the BPF is shown in Fig. 5. The BPF is designed as a fourth order, Chebyshev type.

As can be seen in Fig. 5, the results measured by the network analyzer have a pass band of 3 kHz to 180 kHz with a very narrow pass band of 177 kHz.

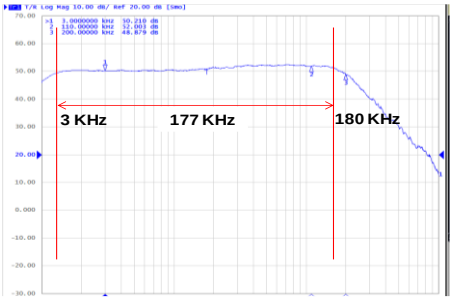

Fig. 5. Band Pass Filter Measurement Result using Network Analyzer

Compared with the simulation result, the change of 177 kHz to 177 kHz was confirmed, and the cut-off frequency was also confirmed to have the cut-off frequency of 3 kHz and 180 kHz in the simulation result of 2 kHz and 173 kHz. In addition to the network analyzer, the oscilloscope is used to check the actual waveforms and to measure the distortion in Fig. 6.

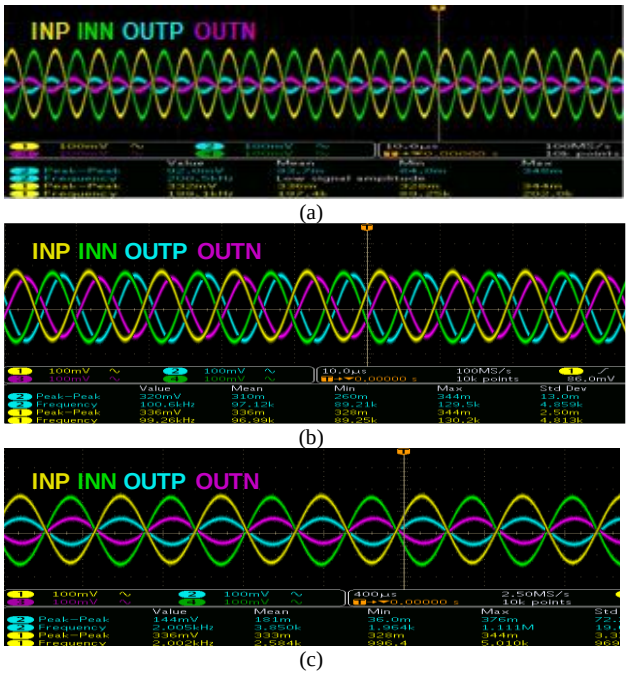

Fig. 6. Band Pass Filter Measurement Result using Oscilloscope; (a) 200 kHz Input Frequency and -9.3 dB measurement result (b) 100 kHz Input Frequency and 0.2 dB measurement result (c) 2 kHz Input Frequency and -5.5 dB measurement result

E. Sigma-Delta ADC

Fig. 7 shows the proposed simplified SD ADC designed in this work. In this application, we designed it to have a high resolution for the ocean measurement environment. In order to reduce the noise, the SDM is designed to push the noise to a higher frequency so that it can be filtered by the following digital filter. A decimation filter is designed to control the decimation factor so as to lower the current consumption.

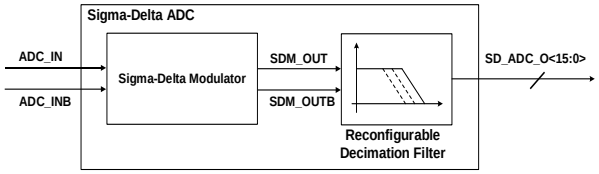

Fig. 7. Simplified block diagram of the proposed SD ADC.

Fig. 8 shows a block diagram of the SDM. The second order discrete type SDM with a Cascaded Integrator Feed-Back (CIFB) structure is implemented.

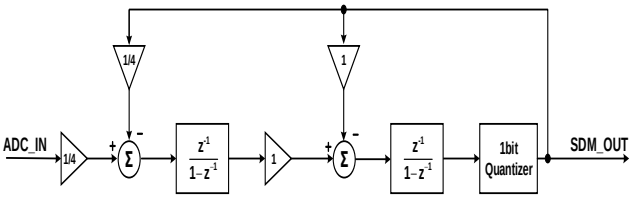

Fig. 8. Block diagram of the Sigma-Delta Modulator (SDM).

The proposed SD ADC mainly consists of an SDM and a digital filter. The digital filter cuts the noise on the high frequency band. The main function of the SDM is to push the noise to a higher frequency than the input signal frequency. In addition, the order of the SDM determines the slope of the output noise shaping. The use of a higher order SDM leads to sharper output noise shaping on the frequency domain. In order to apply a digital filter to the high order SDM, the digital filter should have high power and a large area with a cascaded structure. In the conventional design, the decimation factor of the digital filter is dependent on the OSR of the SDM. In this paper, a digital filter with a controllable decimation factor and controller is presented.

The SDM in this paper has a second order configuration, as shown in Fig. 7. For the small area, a since type filter is adopted for the proposed receiver. The block diagram of the proposed decimation filter is shown in Fig. 19 to include the Integrators and Comb filters with a cascaded structure. The controller is used to control the decimation factor. Using the CONTROLLER block, the register width and proper clocking within the filter stages can be selected. The Integrator clock is the same as the sampling clock (Fs) of the SDM, whereas the Comb can be operated with the sampling clock divided by the decimation ratio (Fs/D). This process helps the decimation filter reduce the power dissipation at the Comb stage of the CIC filter. This clock is controlled by the CONTROLLER block according to the requirements of the decimation ratio. The register size can be varied through the CONTROLLER by changing the decimation ratio. This is because integration.

F. Parallel to Series Interface

The proposed receiver implements the serial interface circuit inside the IC. For pin-constrained applications, a P2S interface is necessary to transmit the data [4].

Fig. 9 shows a block diagram of the P2S-S2P used in the proposed receiver, where SYNC is the synchronization signal, DIN means parallel data input, and SDO is serial data output. The P2S interface is designed inside the IC and S2P is in the FPGA board. The ADC outputs the parallel data, which then goes to the P2S interface, whose output is serial form data. This P2S-S2P interface has two synchronization modes: high throughput mode (HTM) and highly synchronized mode (HSM).

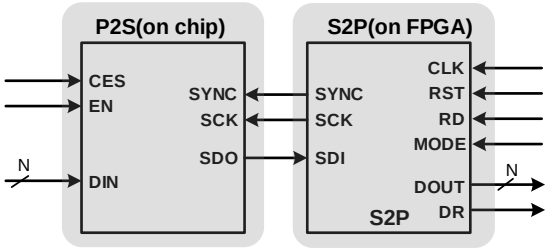

Fig. 9. P2S and S2P block diagram.

In HTM, at first, SYNC is pulled down and the MODE signal is high. Then, P2S receives data from DIN, and at the active edge of clock SCK, transmits it to SDO. SDO is then transmitted in serial from MSB to LSB. In this mode, no overhead bits or extra clock cycles exist. At the time that the communication between the P2S and S2P interfaces begins, P2S and S2P are synchronized once at the negative edge of SYNC. First, MODE is pulled down, and the mode HSM in which P2S and S2P synchronize, is enabled after all serial data is sent and received. Only when RD is high, P2S takes the sample and transmits it to P2S. This mode is selected due to the features of the proposed receiver, which does not require continuous data. In order to achieve high performance P2S interface operation, fsck (the serial clock frequency) is necessary. This is given in Equation (1).

$$f_{SCK} \geq F_{ADC} \times N \tag{1}$$

In Equation (1), N is the resolution and FADC is the sampling frequency of ADC. The P2S and S2P interfaces are in a synchronous finite state machine (FSM) model-based design.

The timing diagram of each piece of data is presented in Fig. 23. In this paper, the P2S circuit is only enabled when EN from the control logic is pulled high. For P2S, the positive or negative active edges can be selected by the clock edge select signal (CES). In the POWER_UP stage, the P2S controller moves to ENABLE. Then, the controller goes to the SYNC_DET state and holds on to the SYNC negative edge. When SYNC is released from S2P, the P2S controller jumps to the next stage, LOAD_STX. In the LOAD_STX state, the parallel data DIN is loaded from the internal register transmitting the MSB to SDO. Then, in the SHIFT_STX state, if SYNC is kept low, the internal register value is shifted one bit to the left, and the MSB of the register is transferred to the SDO pin, remaining for N-1 SCK clock cycles. If HTM is enabled, the controller moves state to LOAD_STX in order to take an SD ADC sample. The controller then either returns to the LOAD_STX state so as to receive the next ADC sample or jumps back to SYNC_DET for resynchronization in the case of HSM. The FSM for the S2P controller is shown in Fig. 15(b). The data remain in the POWER_UP state after reset for one clock cycle, then go to MODE_SEL state, and the MODE signal from control logic selects the mode of either HTM or HSM. When the MODE is asserted, HSM is enabled and the controller changes direction toward the HTM_MODE state. In this state, SYNC is pulled low so as to allow for synchronization between S2P and P2S. In addition, S2P enables the SCLK clock and begins receiving serial data at SDI from S2P. The bits are shifted in serial inside the internal register. There is a counter for checking the number of bits received from P2S. If N bits are received, N-bit DOUT loads the register bits. Additionally, in order to announce to control logic that the data have been received, RD is changed to pulled high for one clock.

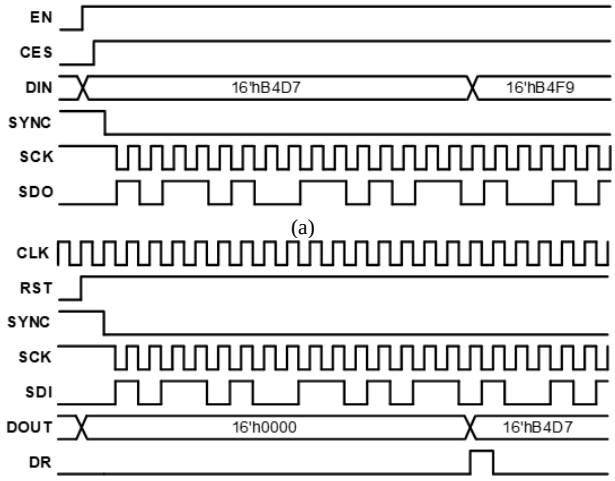

Fig. 10. Serial interface timing diagram; (a) P2S timing diagram (b) S2P timing diagram

III. RESULTS AND DISCUSSIONS

The low noise analog front end receiver is implemented to implement functions such as sensor modeling and ultrasonic signal processing that can be widely used for measuring the distance between objects. Sonar Applications have many noise sources and the receiver is exposed to all these noise sources. The proposed circuit is a receiver that can operate in many noise environments. Fig. 11 shows the evaluation board for the proposed receiver. It employs a low noise low-dropout regulator (LDO) and the Connector to FPGA Board.

Fig. 11. Analog Full-Path Measurement Result

The design of the proposed sonar signal conditioning receiver produces a digital signal with a Sigma-Delta ADC and a Parallel to Series Interface via pre-amplifier, VGA, and BPF. As a result, low noise analog front end system suitable for sonar application is realized, and low band underwater signal can be used for communication. As a result of measurement, 1 Vpp is applied to Sigma-Delta ADC input through the test pin result in each Analog Block shown in Fig. 12, and it shows the result that ADC isolation and operation is possible. As shown in Fig. 13 and Fig. 14, 13.5546 ENOB and 86.58 SNR were confirmed, and the low noise result of at least 11.81 nV / √Hz was confirmed within the pass band.

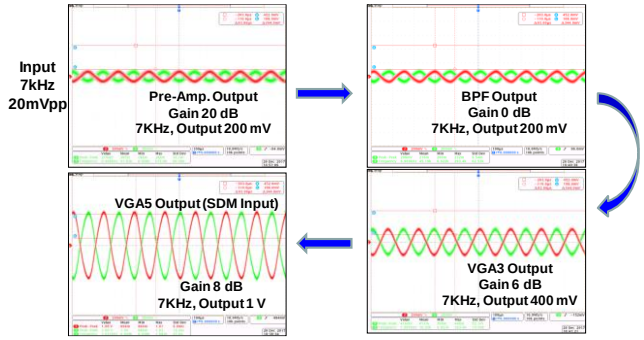

Fig. 12. Analog Full-Path Measurement Result

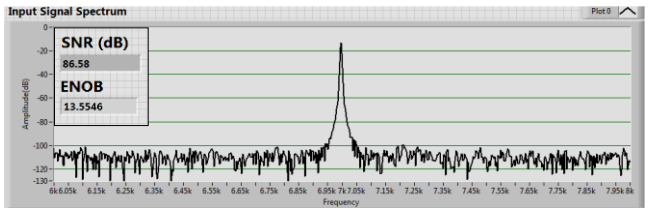

Fig. 13. Sigma-Delta ADC Measurement Result

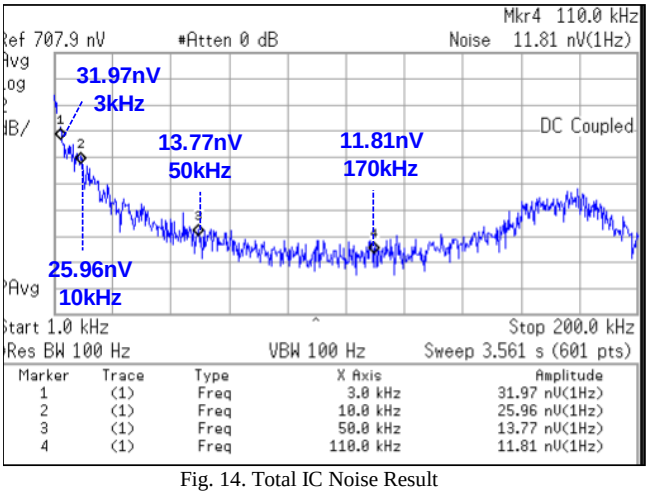

Fig. 14. Total IC Noise Result

IV. CONCLUSIONS

The proposed a low-noise receiver for receiving dynamic amplitude signals, particularly for low frequency and narrow band width systems for ocean sonar sensor application.

In particular, the implementation of narrow bands has the greatest strength as a circuit having immunity against noise components at ambient frequencies that can be generated ocean sonar sensor application. Since ocean sonar sensor application has various noise sources present, we design the proposed receiver with 11.81 nV/ √Hz @ 170 kHz noise performance. Furthermore, the power consumption of the receiver in the ocean environment should be lowered for the sake of portability. This proposed receiver applies several design techniques, including automatic amplitude sensing architecture in VGA. In addition, SDM in the SD ADC is designed with the clock splitting technique. Also SD-ADC has 13.55 ENOB and 86.58 SNR complete the design of underwater operation. Further, the digital filter in the SD ADC is designed with a controller so as to lower the power consumption.

TABLE I.

Performance summary of the proposed receiver

	This work	[5]	[6]
Process (nm)	180	130	65
Power consumption (W)	46.8 m	6.5 m	68 u / 1-ch. (Only for SDM)
Dynamic range (dB)	5 - 20	N/A	40
IR Noise (nV/√Hz)	13.77 @ 50 kHz	2200 @ 10 kHz	N/A
Bandwidth (Hz)	3 k - 170 k	< 10 k	25 k
Sampling frequency (Hz)	1.5 M – 12.5 M	31.25 k	10 M
Area(mm²)	14.44	25	0.03

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