Design Methodology for Capacitively Coupled Continuous-time Delta-sigma Modulator

Chae Gang Lim[1] and Chul Woo Kim[a]
Department of Electrical Engineering, Korea University
E-mail : [1]lcg@kilby.korea.ac.kr

Abstract – **This paper presents a design methodology for high-linearity capacitively coupled (CC) continuous-time delta-sigma modulator (CTDSM). The third-order loop filter enables sufficient noise-shaping with a low oversampling ratio (OSR). The chip is implemented in a 180-nm CMOS process with an active area of 1.65 mm^2, drawing 232.2 uA at a 1.8 V supply. The proposed CC-CTDSM has a 19.4 nV/√Hz input-referred noise density, 1.9 uV offset, 0.08% gain error, 16 ppm integral nonlinearity (INL), and 140 dB common-mode rejection ratio (CMRR) within an input range of 60 mV$_{pp}$.**

With -110.1 dB total harmonic distortion (THD), excellent dynamic linearity performance is achieved owing to the CCIA-integrated design and chopping artifact rejection technique.

Keywords—**CCIA, Chopping, Continuous-time Delta-sigma Modulator (CTDSM), High-linearity**

I. INTRODUCTION

A sensor readout IC is a fundamental circuit block used in instrumentation, bio-medical, and automotive applications. Consumer electronic sensors such as temperature, humidity, and acceleration sensors output electrical signals close to a DC with an amplitude of tens of millivolts. Readout ICs should have low noise, low offset, a high common-mode rejection ratio (CMRR), and high input impedance. In addition, the output of piezoresistive accelerometers, used in car crash and tactical weapon testing, and bio-potential signals such as electrocardiogram (ECG) and electroencephalogram (EEG) are AC responses. Owing to the increasing diversity in sensor applications, the demand for high dynamic linearity performance has increased.

As shown in Fig. 1, a CCIA is a capacitive gain amplifier that adopts chopping as a dynamic offset cancellation technique, thereby achieving low noise and low offset. The CCIA is suitable for measuring DC signals because the gain is determined by the ratio of C_{fb} and C_{in}, which is insensitive to mismatch and exhibits high gain accuracy. However, when measuring AC signals, spikes caused by chopper switching and the nonlinearity of the CCIA limit the dynamic linearity of the entire system. In [1], a THD of -76 dB was achieved at an input range of 80 mV$_{pp}$. Achieving higher dynamic linearity using CCIA necessitates a considerably larger quiescent current than that consumed by noise requirement. This is inefficient in terms of noise-dominated designs. Consequently, a sensor ROIC with high dynamic linearity (THD < -100 dB) using the CCIA has not been reported thus far.

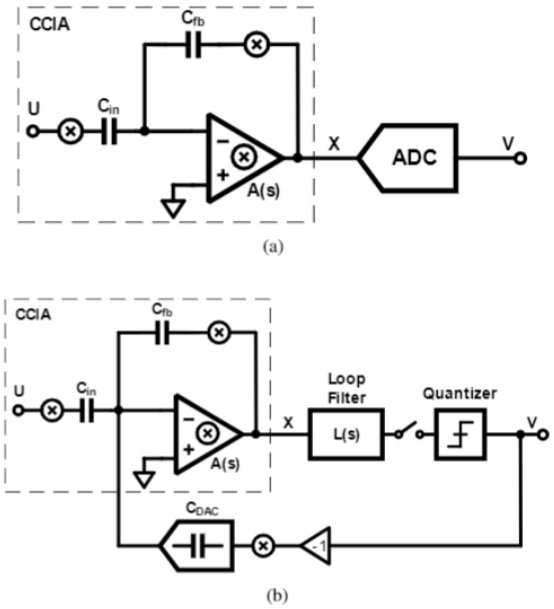

Fig. 1. (a) sensor ROIC with a CCIA, (b) capacitively coupled CTDSM.

In this paper, we present a CC-CTDSM, as shown in Fig. 5. The CTDSM embeds the CCIA at the front-end to desensitize the nonlinearity of the CCIA. This architecture facilitates a highly linear sensor ROIC. As the CCIA is incorporated in the modulator, the CCIA only deals with the shaped quantization noise as the in-band STF is unity. The effective signal range is shrunk and the op-amp lies in a more linear swing range. Because it hardly provides a signal-dependent error, it can significantly increase the ROIC linearity. However, the CCIA chopper causes problems in the proposed CC-CTDSM.

The chopping artifacts generated in the CCIA are rejected with sampling frequency chopping and optimized RRL, and

a. Corresponding author; ckim@kilby.korea.ac.kr

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chopping-induced in-band noise increase, distortion, and loop instability are avoided. Due to this feature, the proposed CC-CTDSM can employ the non-return-to-zero (NRZ) digital-to-analog converter (DAC) as the main feedback DAC of the modulator, which has alleviated amplifier speed requirement and better stability than the return-to-zero (RZ) DAC. Furthermore, no extra analog filters are located before or inside the ROIC owing to the inherent anti-aliasing characteristic of the CTDSM. This ROIC enables accurate sensing of AC signals since the internal chopping spikes are totally suppressed and the harmonic distortions of the CCIA are desensitized in the modulator loop.

The prototype chip is implemented in a 180-nm CMOS technology. It achieves 19.4 nV/√Hz, -110.3 dB THD, 1.9 μV input-referred offset, 0.1% gain error, and 16 ppm INL over an input range of 60 mV_{pp}.

II. DESIGN CONSIDERATIONS FOR CC-CTDSM

A. System Design

The chopping frequency of the proposed CC-CTDSM is equal to the sampling frequency. This condition forces a significantly higher chopping frequency to achieve sufficient quantization noise shaping. It enables to build a high-order loop filter with a 5-bit quantizer. Hence, this is possible to get a sufficient SQNR with a low OSR. In this article, a 3rd-order loop filter is used with an OSR of 40. The signal bandwidth is 1 kHz, and the maximum out-of-band gain of the NTF is 2.5.

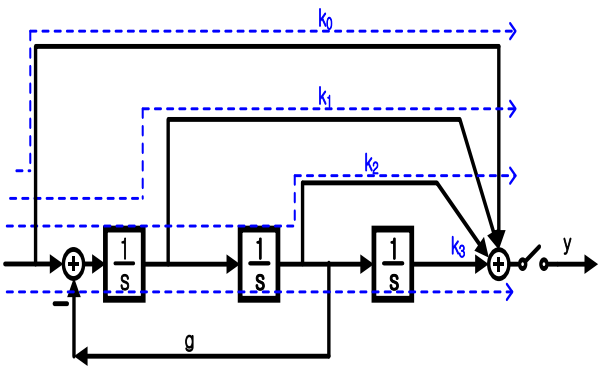

Fig. 2. CT loop filter coefficients

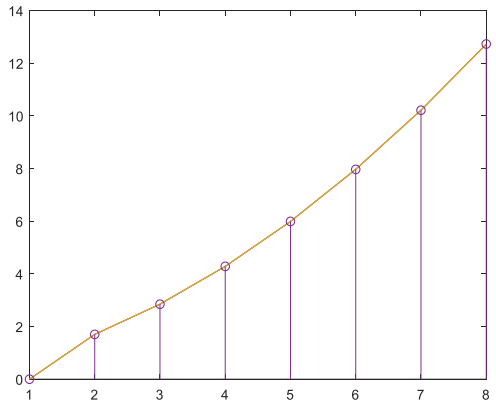

Fig. 3. Impulse response of the DT loop filter and CT converted one

In order to build a noise transfer function (NTF) of the system, we used the Delta-Sigma toolbox to synthesize the NTF. The excess loop delay is assigned by 0.5*Ts* for the quantizer and DAC process time. The NTF is synthesized in discrete-time transfer function and converted into continuous-time format through impulse response matching as shown in Fig. 2. We can take into account the non-idealities of the amplifiers used in integrators. In the case of the first integrators, the amplifier parameters are extracted from CADENCE simulations. The two-stage miller-compensated amplifier gain is 130 dB and the bandwidth is 6 time of the sampling frequency. The impulse response of the DT and CT loop filters are shown in Fig. 3 and their difference is presented in Fig. 4.

In Fig. 5, the gain of the CCIA, G (= C_{in}/C_{fb}) is fixed to 50 to amplify the millivolts range of the transducer output for the following ADC. As the CCIA itself is a closed-loop

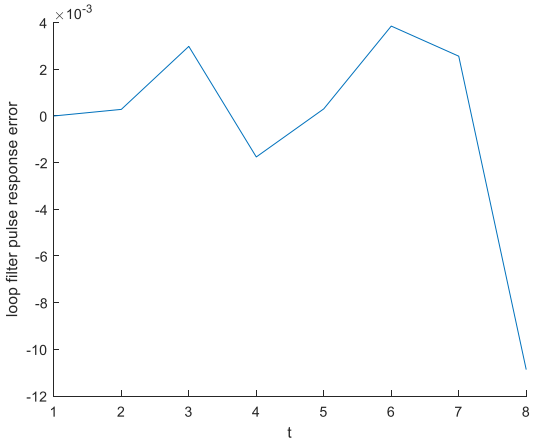

Fig. 4. Impulse response difference between DT and CT

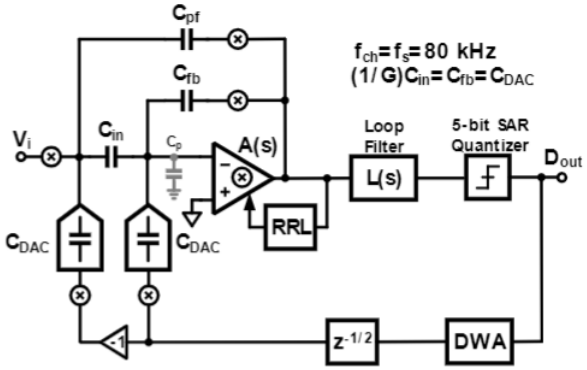

Fig. 5. Top block diagram

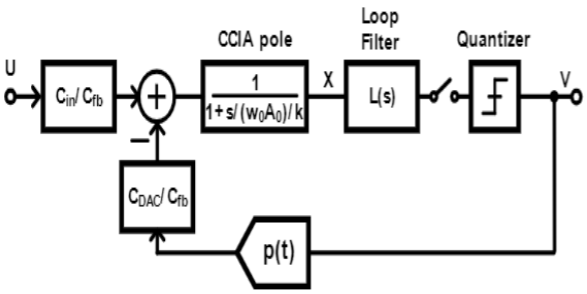

Fig. 6. Linear model of the proposed CC-CTDSM with a CCIA pole

system, the finite bandwidth effect is simplified by generalizing CCIA as a one-pole system. Assuming that the op-amp has one pole, the CCIA provides an extra delay in front of the loop filter. The linear model of CC-CTDSM, including finite bandwidth of CCIA, is presented in Fig. 6. It is desirable that the CCIA bandwidth be sufficiently high to disregard the excess loop delay. In this design, the dominant pole of CCIA is near the sampling frequency, f_s. The delay is $1/(2\pi f_s) \approx 0.16$Ts in the first-order approximation. This delay can be compensated by an excess loop delay compensation circuit, as shown in Fig. 7.

B. CCIA design

Fig. 8 shows a circuit diagram of the CCIA. A two-stage miller compensated op-amp is implemented with the RRL. The CM bias resistor is implemented using subthreshold biased transistors [2]. Both NMOS and PMOS transistors are used to provide a fast CM settling time. The resistance exceeds 50 MΩ in the steady state at half VDD bias, which has negligible noise contribution.

Fig. 9 shows a schematic of the two-stage op-amp. The op-amp input stage is a folded-cascode OTA with PMOS input transistors. The tail current source of the input stage is boosted for a higher CMRR. The source transistors of the cascode stage are biased in strong inversion to reduce their thermal noise. The output choppers of the op-amp are placed between the current sources to avoid reduction in the op-amp gain due to parasitic capacitors. The first-stage transconductance G_{m1} is 342 μS. The DC gain of the op-amp is 130 dB, the unity-gain frequency is 5.4 MHz, and the phase margin is 66° as presented in Fig. 10.

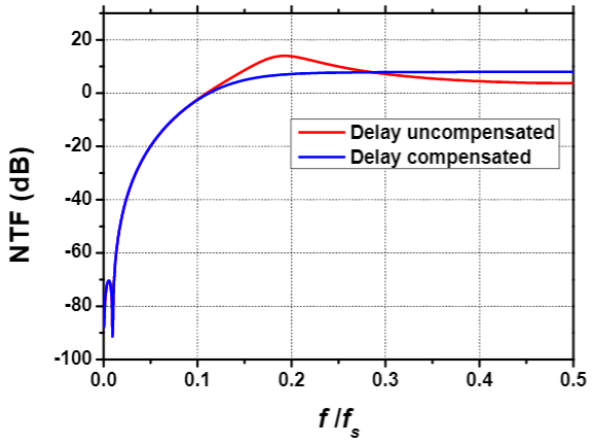

Fig. 7. NTF of CC-CTDSM with CCIA with delay compensation

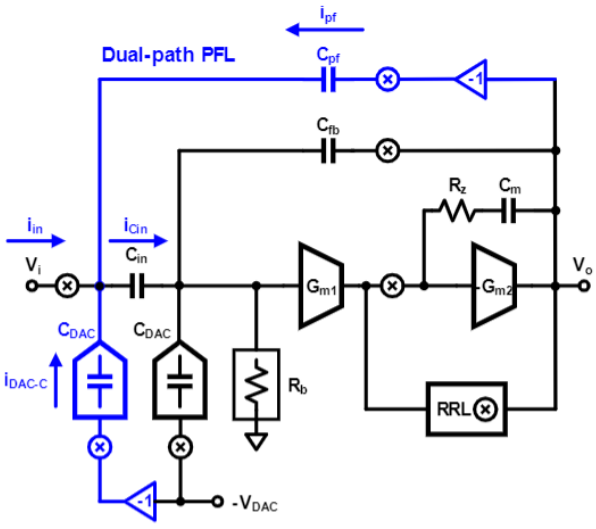

Fig. 8. Front-end of CC-CTDSM (impedance boosting loop, bias resistor, two-stage op-amp, and RRL)

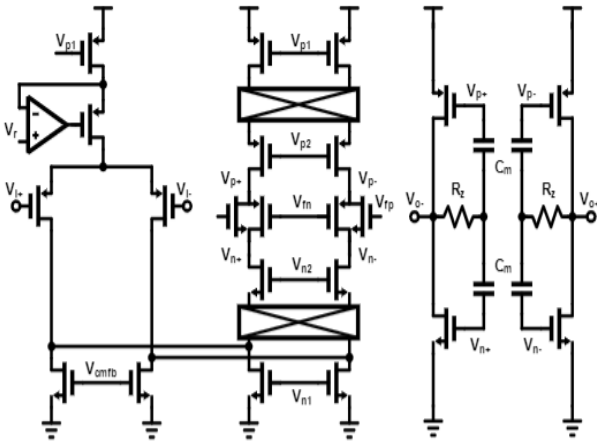

Fig. 9. Schematic of two-stage op-amp used for CCIA

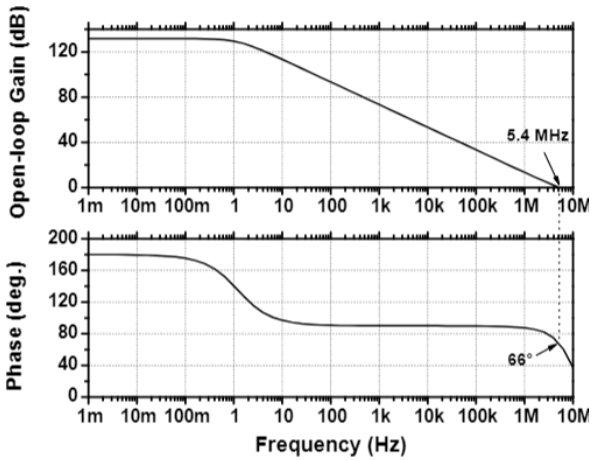

Fig. 10. Simulation results of the open-loop gain and phase of the op-amp.

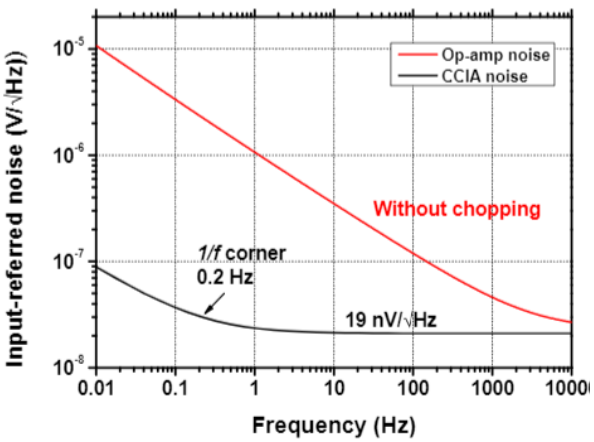

Fig. 11. Input-referred noise density of the op-amp and chopped CCIA.

The input-referred noise of the proposed system is dominated by G_{m1}. The G_{m2} noise and the following loop filter noise are attenuated by the open-loop gain of G_{m1} and closed-loop gain of the CCIA, respectively. As shown in Fig. 11, the CCIA input-referred noise is 19 nV/√Hz and the *1/f* corner is 0.2 Hz. The *1/f* noise is sufficiently attenuated by a chopping frequency of 80 kHz. The closed-loop pole of the CCIA is 80 kHz, which does not influence the transfer function of the following integrators.

The compensation transconductance G_{m3} and sensing capacitor C_s in the RRL determine the conversion gain, which involves noise-folding. For minimizing noise-folding, G_{m3} and C_s is set to 4.8 μS and 100 fF, respectively. In addition, A_{int} is a folded-cascode OTA with a 90-dB DC gain to achieve a steep loop gain of the RRL.

C. CTDSM design

Fig. 12 shows the loop filter used in the CC-CTDSM. A third-order loop filter with an optimized NTF zero is implemented for energy-efficient quantizing compared to the low-order design. The CCIA structure is utilized to avoid an extra feedback DAC. Capacitor C_{FF1} and C_{FF2} provide a feedforward gain. The first integrator is chopped because the preceding capacitive gain stage does not completely suppress the 1/f noise of the integrator. To avoid chopping aliasing, the chopping frequency of the integrator is also equal to the sampling frequency. For optimized NTF zero, the resonator resistor should be 675 MΩ, which is excessively bulky. Instead, the T-network comprises Rx, Ry, and R_z, which form an equivalently large resistance of $R_z(R_x/R_y)$ [3]. The input resistor, R_1, dominates the loop filter noise because the first integrator attenuates the noise in the following stages. However, driving an excessively small R1 is a burden on CCIA. Therefore, R_1 of 500kΩ is used in this design. Besides, R_2 and R_3 are 25 and 50 MΩ, respectively, thereby lowering the op-amp output loads.

All capacitors in the loop filter have a 5-bit tuning range of 50% from nominal value to compensate the RC time constant variation. In addition, a dedicated RC calibration [4] circuit is implemented as shown in Fig. 13.

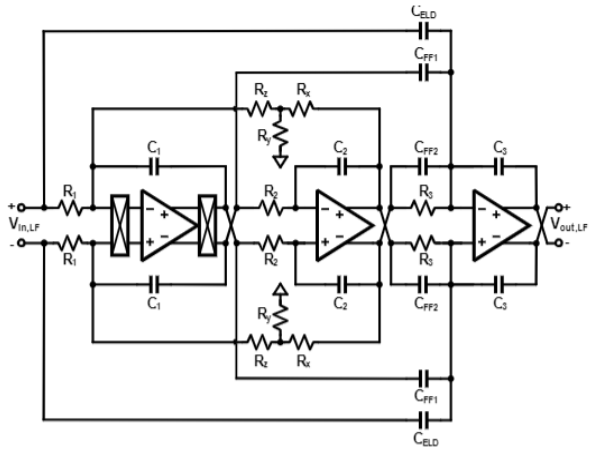

Fig. 12. Loop filter of the CC-CTDSM

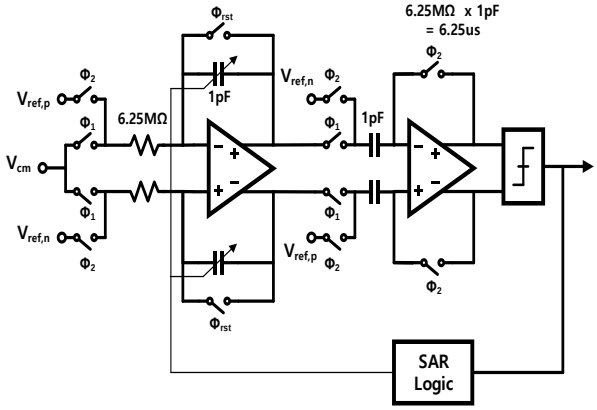

Fig. 13. RC calibration circuit.

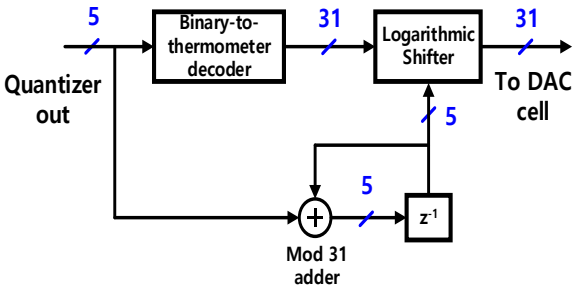

Fig. 14. Block diagram of DWA.

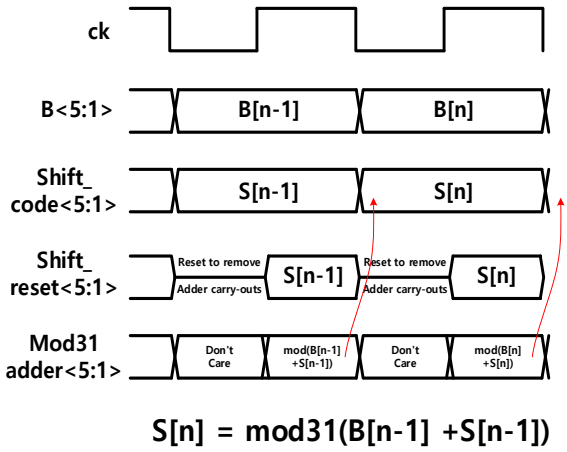

Fig. 15. Timing diagram of DWA.

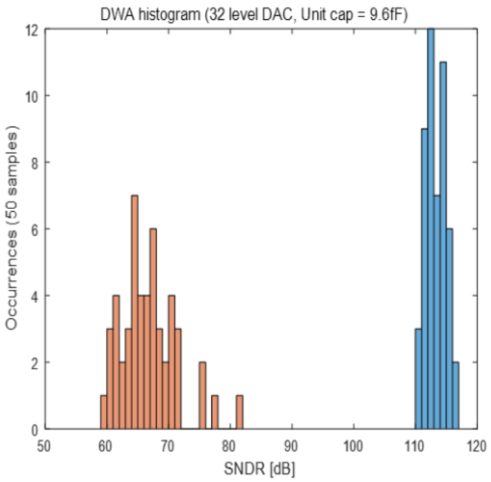

Fig. 16. Behavioral simulation results of DWA.

As the 5-bit quantizer and DWA logic contribute to the operation time, an excess loop delay should be assigned to secure modulator stability. Therefore, a half-cycle of the sampling frequency is assigned. An ELD compensation path is easily implemented because loop filter input contains a feedback DAC component. The C_{ELD} and C_3 ratios comprise the compensation gain. The DWA logic is implemented as Fig. 14. Its timing diagram and operations are presented in Fig. 15. Through the behavioral simulations, the modulator can guarantee over 110 dB SNDR after the DWA as shown in Fig. 16.

The SAR-type quantizer has the highest power efficiency under slow (80 kS/s) and low-resolution conditions (5-bit). Fig. 18 shows a single-ended diagram of the 5-bit SAR quantizer used in this design. The unit capacitor of the capacitive DAC of the SAR quantizer is 10 fF. Asynchronous SAR logic is implemented to avoid the use of an additional clock signal. The main feedback DAC of the CC-CTDSM is composed of a thermometer-based 31-unit CDAC cell, as shown in Fig. 17. The quantizer samples the loop filter output and digitizes it at the falling edge of f_s. After a half clock cycle, the DAC output $V_{DAC,u}$ is updated at the rising edge of f_s. Because the DAC cell incorporates chopping, the update rate of the D flip-flop (DFF) is set as $2f_s$ to generate the opposite data.

A prototype of the proposed CC-CTDSM is implemented using a 180-nm CMOS process. Fig. 19 presents a photograph of the fabricated chip, where the active are, including the RC calibration circuit, is 1.65 mm^2. The chip consumes a current of 232.2 uA at a 1.8 V supply voltage.

Fig. 20 shows measured PSD of the proposed CC-CTDSM with input shorting and Fig. 21 shows sine wave test for a dynamic linearity measurement. Fig. 22 shows measured DC performance of the ROIC. A performance summary and comparison with state-of-the-art sensor

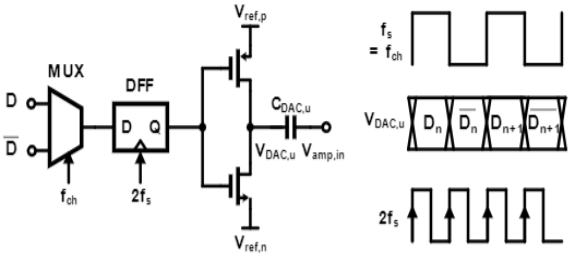

Fig. 17. Unit DAC cell of the CC-CTDSM and timing diagram.

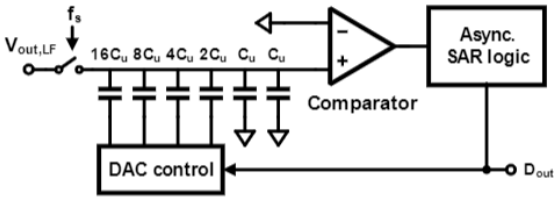

Fig. 18. 5-bit SAR quantizer of the CC-CTDSM.

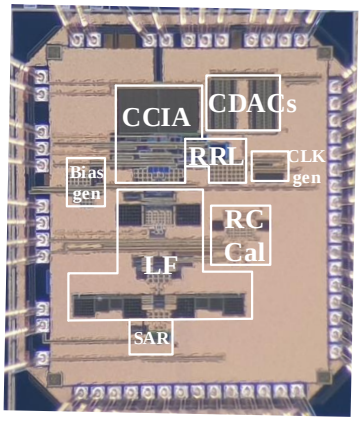

Fig. 19. Chip photograph.

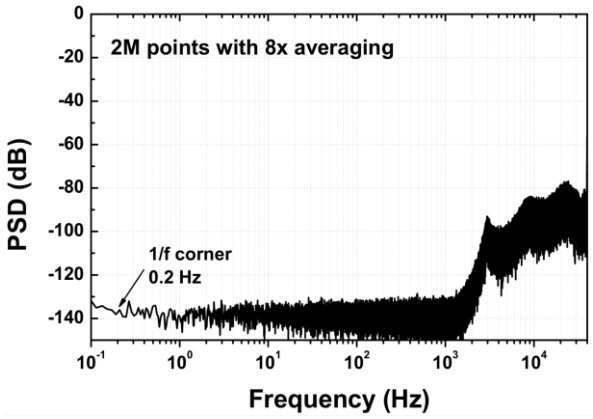

Fig. 20. Measured PSD of input-shorted CC-CTDSM

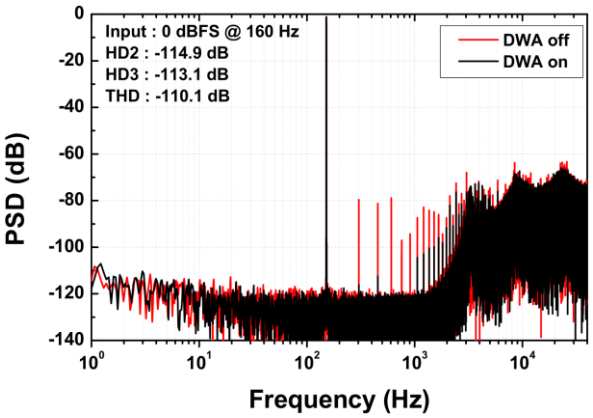

Fig. 21. Measured PSD of CC-CTDSM with sine input.

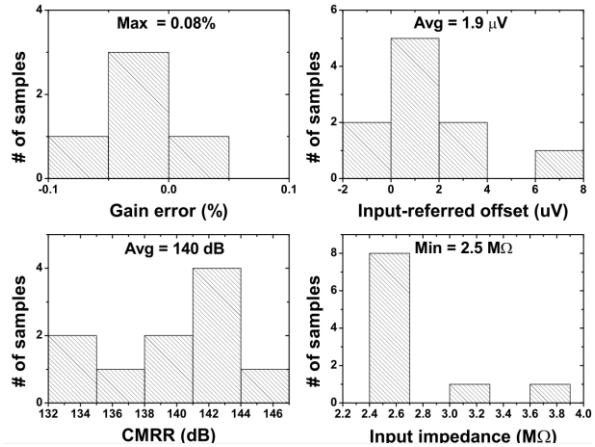

Fig. 22. Measured gain error, offset, CMRR, and input impedance

Table I. Comparison with State-of-the-art sensor readout ICs

	This work	JSSC 2019 [5]	JSSC 2019 [6]	L-SSC 2019 [7]	SOVC 2017 [8]	SOVC 2018 [9]	JSSC 2020 [10]
Architecture	**CC-CTΔΣM**	CCIA+DTΔΣM	CCIA+CTΔΣM	CC-CTΔΣM	CC-CTΔΣM	CC-CTΔΣM	PLL-ΔΣM
Technology (nm)	**180**	130	180	180	40	180	40
Active Area (mm^2)	**1.65**	0.65	0.73	0.75	0.06	1.1	0.025
Supply Voltage (V)	**1.8**	3(A) / 1.5(D)	1.8	1.8	1.2	1	0.8(A) / 0.6(D)
Supply Current (μA)	**232.3**	326(A) / 20(D)	1200	1200	21	6.5	3.4(A) / 3.2(D)
Bandwidth (kHz)	**1**	0.0025–0.04	2	2	2	0.15	10
Input Range (mV_{pp})	**60**	43.75 – 5600	20	16	100	360	100 / 400
CM Input Range (V)	**0–1.8**	0–3	0–3.3	0–3.3	0–1.2	0–1.2	0–0.8
Offset (μV)	**1.9**	1.87	7	300	–	–	50
Input Noise Density ($nV/\sqrt{Hz}$)	**19.4**	44	3.7	4.5	140	265	36
CMRR (dB)	**140**	126	134	137	–	84	83
Gain Error (%)	**0.1**	–	0.3	0.2	–	–	–
FoM* (dB)	**155.0**	169.3(@gain=1)	151.1	148.6	154.0	160.9	172
NEF / PEF	**11.2 / 224.8**	6.6 / 130	5.0 / 45	6.1 / 67.0	22.6 / 612	26 / 676	– / 8.9
THD (dB)	**-110.3**	–	–	–	-82	-104.7**	-91**

* FoM = $10\log(V_{FS}^2/(8 \cdot v_n^2 \cdot P))$ ** SFDR *** PEF = $NEF^2 \cdot V_{DD}$

readout ICs are depicted in Table 1. The left three readout ICs employ the CCIA front-end. These ICs are specialized in DC measurement systems such as a Wheatstone bridge sensor with low input-referred noise, offset, and high CMRR. In contrast, the right three paper are focused on AC measurements, such as Hall sensor or biopotential sensors with high dynamic linearity performance. However, they are not capable of AC measurement. The proposed sensor readout IC, however, is capable of both DC and AC measurement. It achieves 19.4 nV/√Hz, -110.3 dB THD, 1.9 μV input-referred offset, 0.1% gain error, and 16 ppm INL over an input range of 60 mV_{pp}.

IV. CONCLUSION

This paper presents a high-dynamic-linearity CC-CTDSM for sensor readout applications. To obtain a high dynamic linearity, the CTDSM employs a CCIA as the front-end inside the loop; thus, the requirements of the op-amp are relaxed and CCIA processes only shaped quantization noise component and relax the input-dependent issues, i.e. input swing range and harmonic distortions. Using the chopping frequency as the sampling frequency enables us to ignore chopping aliasing and also reject chopping ripples and spikes. The third-order loop filter and 5-bit quantizer allow for a low chopping frequency. The DWA prevents a reduction in linearity by a static mismatch in the main feedback DAC. The prototype chip is implemented in 180-nm CMOS technology, and it is capable of reading out both AC and DC responses. The measurement results prove that the proposed architecture achieves the highest THD among previously reported sensor readout ICs.

ACKNOWLEDGMENT

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Chae Gang Lim (S'14) received the B.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2014, where he is currently working toward an integrated M.S. And Ph. D. degree.

In 2017, he was a Visiting Researcher at the University of Texas at Austin, TX, USA. He received the 21st Korea Semiconductor Design Contest enterprise special prize (Cadence) in 2020. His research interests include sensor readout ICs and oversampling ADCs.

Chul Woo Kim (S'98-M'02-SM'06) received the B.S. and M.S. degrees in electronics engineering from Korea University in 1994 and 1996, respectively, and a Ph. D. in electrical and computer engineering from the University of Illinois at Urbana-Champaign, IL, USA, in 2001.

In 1999, he worked as a summer intern at the Design Technology at Intel Corporation, Santa Clara, CA. In May 2001, he joined IBM Microelectronics Division, Austin, TX, where he was involved in Cell processor design. Since September 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor at the University of California at Los Angeles in 2008 and at the University of California at Santa Cruz in 2012. He is a coauthor of two books, namely, CMOS Digital Integrated Circuits: Analysis and Design (McGraw Hill, 4th edition 2014) and High-Bandwidth Memory Interface (Springer, 2013). His current research interests are in the areas of wireline transceiver, memory, power management and data converters.

Dr. Kim received the Samsung HumanTech Thesis Contest Bronze Award (1996), the ISLPED Low-Power Design Contest Award (2001, 2014), the DAC Student Design Contest Award (2002), SRC Inventor Recognition Awards (2002), the Young Scientist Award from the Ministry of Science and Technology of Korea (2003), the Seoktop Award for excellence in teaching (2006, 2011) and ASP-DAC Best Design Award (2008) and Special Feature Award (2014), Korea Semiconductor Design Contest: Prime Minister Award (2016). He served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference and as a Guest Editor for IEEE Journal of Solid-State Circuits. He is currently on the editorial board of IEEE Transactions on VLSI Systems and the Chair of the SSCS Seoul Chapter. He has been elected as Distinguished Lecturer of the IEEE Solid-State Circuits Society for 2015–2016.