A 2.4 GHz Low Power Low-IF Receiver Employing OOK and FSK Dual-Mode Demodulator for IoT Applications

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***Abstract* – In this paper, a 2.4 GHz low-power low-IF receiver employing a dual-mode demodulator for on-off keying (OOK) and frequency-shift keying (FSK) signals is presented for Internet of Things (IoT) applications. The switched dual-mode demodulator can demodulate both OOK and FSK signals. The proposed receiver consists of a low-noise transconductance amplifier, single-balanced current-mode passive mixer, transimpedance amplifier, variable gain amplifier, and dual-mode demodulator. The proposed receiver was designed in a 65-nm CMOS process and mainly simulated at 2.4 GHz. The receiver achieves a noise figure of 9.9 dB, a maximum conversion gain of 74 dB, and an input-referred third-order intercept point of −26.3 dBm. The active die area of the designed receiver is 0.53 mm^2, and it draws a bias current of 1.8 mA from a nominal supply voltage of 1 V.**

***Keywords*—2.4 GHz, Dual-mode demodulator, Frequency-shift keying (FSK), IoT, Low-power, On-Off Keying (OOK)**

I. INTRODUCTION

The Internet of Things (IoT) is a technology that collects, stores, and analyzes data using sensors and communication on various devices. Developing a technology that can be used permanently without battery replacement is one of the most important issues in IoT sensors. Generally, a wireless communication system is the most power-consuming block in IoT sensors. In order to minimize the power consumption of the wireless communication system, researches on the duty-cycle-based transceiver architecture that turns on the transceiver only at a certain time and the transceiver architecture based on the ultra-low power wake-up radio are being actively conducted [1]–[4]. Because IoT transceivers do not require a high data rate, simple modulation schemes such as on-off keying (OOK) or frequency-shift keying (FSK) are mainly used.

In this paper, a 2.4 GHz low-power low-IF receiver employing a dual-mode demodulator, which can demodulate both OOK and FSK signals is proposed for IoT applications. Section II presents the proposed low-power low-IF receiver architecture and detailed circuit designs. Simulation results are shown in Section III. Finally, Section IV concludes the paper.

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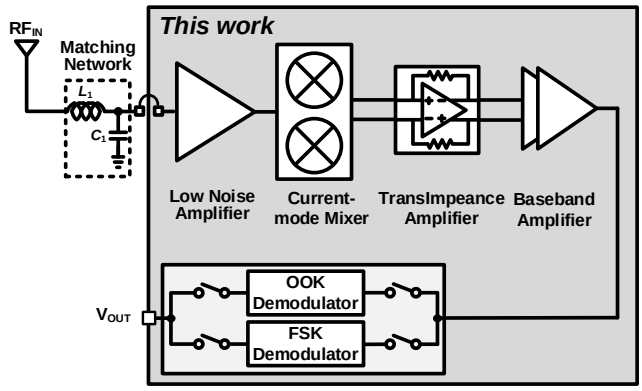


Fig. 1. Block diagram of the proposed receiver.

II. CIRCUIT IMPLEMENTATION

Fig. 1 shows the block diagram of the proposed low-power low-IF receiver with a dual-mode demodulator. The proposed receiver consists of a low-noise transcondutance amplifier (LNTA), single-balanced current-mode passive mixer, transimpedance amplifier (TIA), variable gain amplifier (VGA), and dual-mode demodulator.

A current-reused resistive feedback LNTA is shown in Fig. 2. The resistive feedback LNTA can perform an input impedance matching without a bulky degeneration on-chip inductor. The current-reuse technique increases the voltage gain and reduces the noise figure (NF) with the same current consumption as the conventional common-source (CS) amplifier because the effective transconductance (g_m) becomes $g_{m1} + g_{m2}$ [5]. The R_F provides the real part of the resistive feedback LNTA input impedance. The gate biasing for M_1 and M_2 are separated to support low supply voltage. [6]. The proposed RF LNTA also adopts an input matching network composed of L_1 and C_1 to take advantage of the gain-boosting property of an inductor-degenerated CSLNA (L-CSLNA). The input impedance of the RF LNTA R_{IN_RFLNTA} is $(R_F + R_{oLNTA}) / (1 + g_{mLNTA}R_{oLNTA})$, where g_{mLNTA} is $g_{m1} + g_{m2}$ and R_{oLNTA} is $r_{o1} // r_{o2} // R_{IN\_MIXER}$. The equivalent input matching network can be converted from a parallel RC to series RC network with a narrow frequency band of interest. Therefore, the proposed RF LNTA performs input

power matching with a series *RLC* network. The overall g_m of the proposed RF LNTA is effectively boosted by $\sqrt{(1+Q^2)}$ [7]. The series capacitance C_{SER} and series resistance R_{SER} in the converted series *RLC* network are expressed as $(C_{gs} + C_1)(1 + 1/Q_L^2)$ and $(R_F + R_{oLNTA}) / [(1 + g_{mLNTA}R_{oLNTA})(1 + Q_L^2)]$, respectively. When the L_1 and C_{SER} values are set to resonate at 2.4 GHz, the input impedance of the proposed LNTA is R_{SER}, which is equal to a source resistance R_S. Therefore, Q_L is $\omega_o L_1/R_S$ for the operation frequency of ω_o. The overall transconductance of the proposed LNTA from V_S to the LNTA output current is given to

$$G_{mLNTA} = \frac{\sqrt{1+Q_L^2}}{2}\left(g_{mLNTA} - \frac{1}{R_F}\right) \approx \frac{\sqrt{1+Q_L^2}}{2} g_{mLNTA} \quad (1)$$

It can be known from (1) that the current-reused RF LNTA has a large effective transconductance.

The current-mode single-balanced passive mixer with 50 % duty-cycle local oscillator signal is used for down-conversion. It is shown in Fig. 3. An operational amplifier (OPAMP)-based TIA is used for current-to-voltage conversion and the first-order OB blocker filtering. A modified feedforward (FF) op-amp is utilized due to its inherent wideband characteristic [8]. From the FF op-amp, an intrinsic zero from the FF path compensates the phase of the op-amp without Miller capacitance and accordingly extends the bandwidth of the op-amp. Fig. 4 shows a schematic of a modified FF OPAMP. As the main and FF paths are depicted in Fig. 4, the first, second, and FF amplifier stages are given by M_{1-2}, M_{7-8}, and M_{5-6}, respectively. It is noted that the second stage also acts as an active load of the FF stage so that the extra second stage with a separate current branch is not necessary. Therefore, the internal poles and zeros generated by the parasitic can be

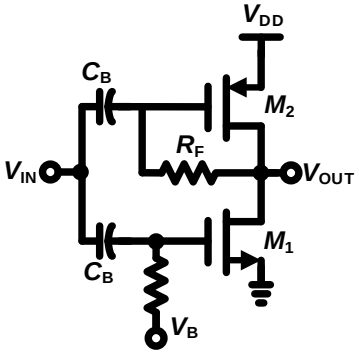


Fig. 2. Current-reused resistive-feedback LNTA

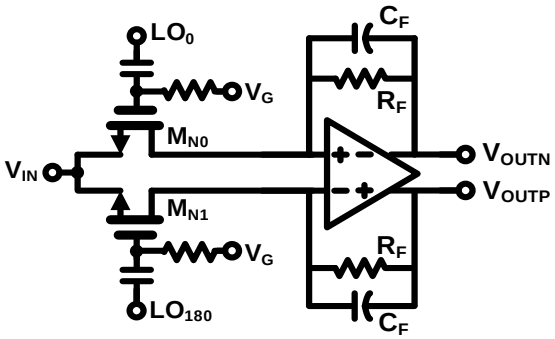


Fig. 3. Single-balanced current-mode passive mixer with TIA

reduced, and this improves the bandwidth of the modified FF structure. The small input impedance of the TIA can limit the voltage swing at the input and output of the mixer which enhances the linearity.

The conversion gain of the receiver RF front-end from V_S to the TIA output voltage is expressed as

$$A_{VRFFE} \approx \frac{\sqrt{1+Q_L^2}}{\pi} g_{mLNTA} R_{FTIA} \quad (2)$$

where R_{FTIA} is a feedback resistor of the TIA.

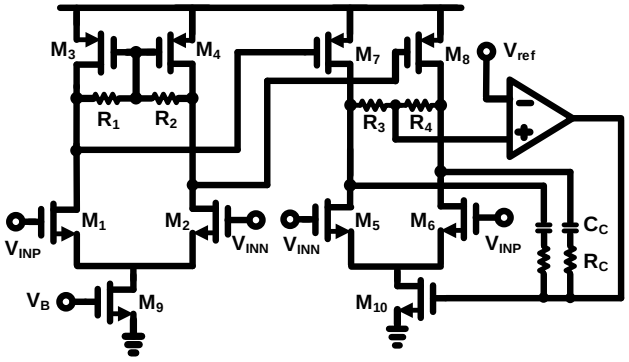


Fig. 4. Modified FF OPAMP

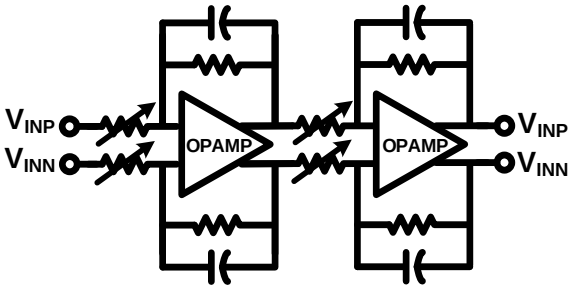


Fig. 5. Two-stage OPAMP-based VGA

The schematic of VGA is presented in Fig. 5. The two-stage OPAMP-based baseband amplifier is designed to have sufficient gain and dynamic range. The FF OPAMP shown in Fig. 4 is also used in VGA.

A switched dual-mode demodulator supporting both OOK and FSK demodulations is presented in Fig. 6. The demodulator scheme is selected according to the input modulation signal. The schematic of the FSK demodulator is presented in Fig. 6(a). The energy charging capacitor C_B is charged and discharged with on-and-off operations of M_{P1} and M_{N1}. If the input frequency is high, each charging and discharging time will be short, resulting in a low charged voltage across C_B. On the other hand, at the low input frequency, the higher voltage is charged in C_B. The comparator compares V_{ref} with the voltage across C_B. The comparator generates a rail-to-rail signal in the low input frequency and a zero voltage signal in the high input frequency. The comparator output voltage and delayed FSK signal are the input signal and clock of D flip-flop, respectively. Because the delayed input signal is used as the clock signal, an additional external clock is not required. The OOK demodulator is shown in Fig. 6(b). The OOK demodulator compares the OOK input signal and the low-pass filtered OOK signal and determinen logic 0 and 1.

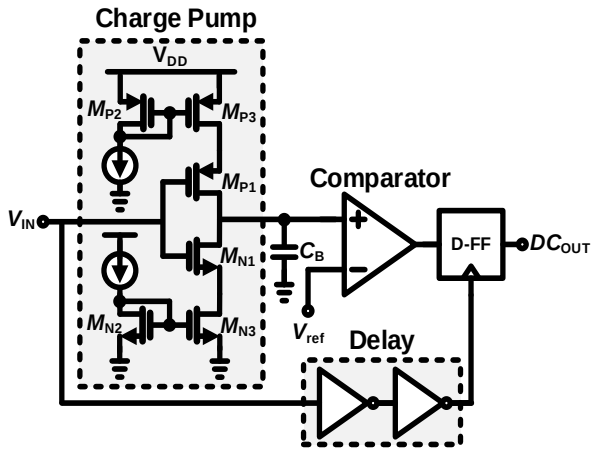
III. SIMULATION RESULTS

The proposed 2.4GHz low power low-IF receiver with a switched dual-mode demodulator was designed and simulated in a 65-nm process. The layout is shown in Fig. 7. The active area is 0.53 mm^2 excluding the bond pads. It consumes 1.8 mW at a supply voltage of 1V. The power breakdown of the proposed receiver according to the operating modes is shown in Table I.

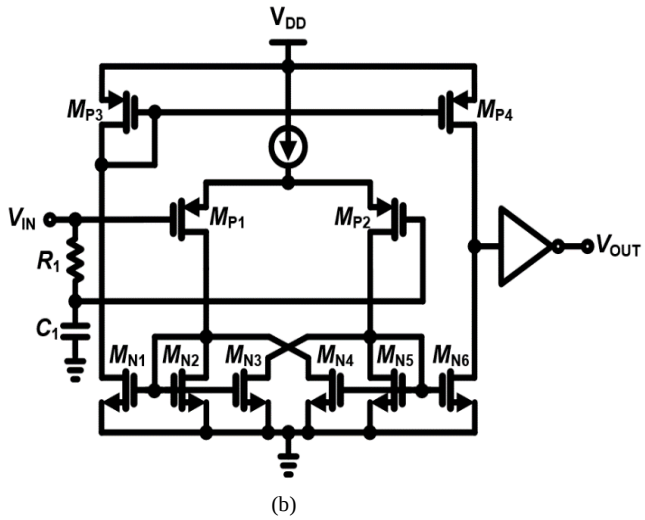
Fig. 8 shows simulated S11 of the designed receiver. The receiver obtained S11 of less than 10 dB in the frequency range of 2-2.7 GHz. The simulated conversion gain of the receiver is depicted in Fig. 9. The conversion gain of 74 dB is obtained. The simulated NF of the receiver is illustrated in Fig. 10. The obtained NF at the IF frequency of 2 MHz is 9.9 dB. The simulated input-referred third-order intercept points (IIP3) is shown in Fig. 11. The two-tone test conditions for IIP3 are $f_1 = f_{LO} + 5$ MHz and $f_2 = f_{LO} + 8$ MHz. The simulated IIP3 of –26.3 dBm is obtained. The simulated transient response of the receiver according to the modulated signals are shown in Fig. 12. The designed dual-mode demodulators can demodulate both OOK and FSK signals.

TABLE I. Simulated Power Breakdown

	Power Consumption (OOK)	Power Consumption (FSK)
LNA	1 mW	
TIA	0.2 mW	
VGA	0.4 mW	
DMD	0.15 mW	0.2 mW
Total	1.75 mW	1.8 mW



(a)



(b)

Fig. 6. (a) FSK Demodulator (b) OOK Demodulator

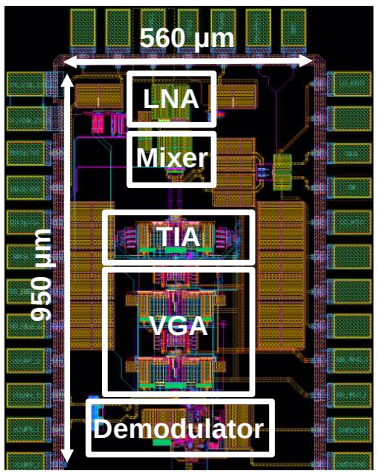


Fig. 7. Layout

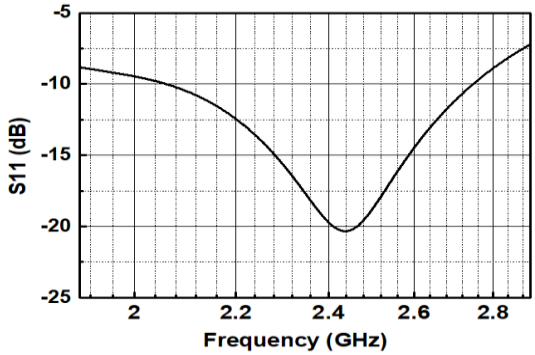


Fig. 8. Simulated S11

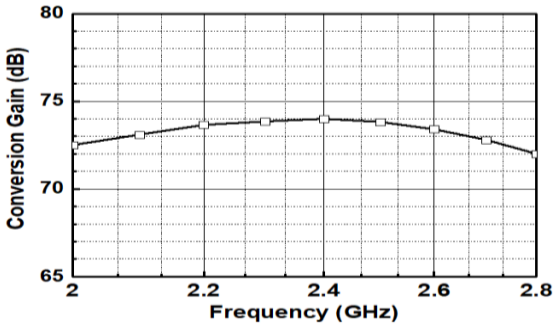


Fig. 9. Simulated conversion gain

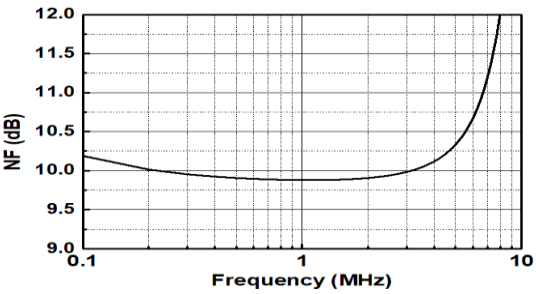


Fig. 10. Simulated NF

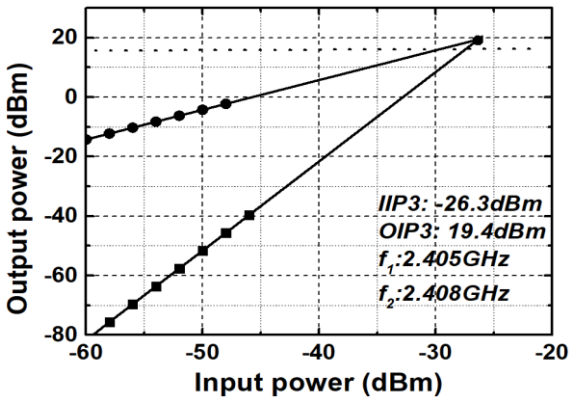
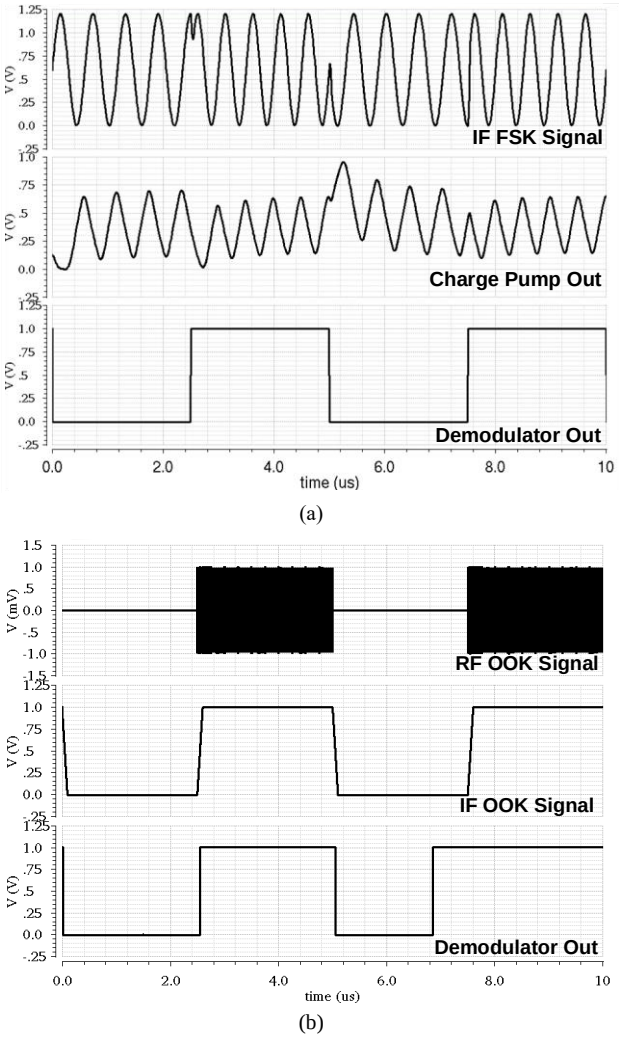


Fig. 11. Simulated IIP3



(a)

(b)

Fig. 12. Simulated transient response: (a) FSK (b) OOK

Table II summarizes the simulated performances of the designed receiver and compares them with those of state-of-the-art receivers. We use a figure of merit (FOM), which is defined as

$$\mathrm{FoM}(dB) = -P_{SEN}(dBm) - 10\log\frac{P_{dc}}{1\,\mathrm{mW}}. \qquad (3)$$

This work can support dual-mode demodulations while achieving the similar sensitivity performance and FOM.

TABLE II. Performance Summary and comparison with previous works

Reference	[9]	[10]	[11]	[12]	[13]	This Work*
Operating Frequency (GHz)	5.5-5.8	0.915	2.4	2.44	5.8	2.44
Process	40nm CMOS	55nm CMOS	40nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS
Modulation	OOK	BFSK	FSK	FSK	OOK/ FSK	OOK /FSK
Power (mW)	0.217	0.499	1.2	0.22	0.47/ 0.49	1.75/1.8
Bandwidth (MHz)	2	1	2	2	1	2.4
NF(dB)	17	N/A	9	22.6	12	9.9
Sensitivity (dBm)	-82	-99	-82.2	-85	-90	-89
Area (mm^2)	0.151	2.25	1	2.4	0.166	0.53
FOM (dB)	88.64	99.01	81.41	91.58	90.27	86.57

*Simulation Results

IV. CONCLUSION

A 2.4 GHz low-power low-IF receiver employing a dual-mode demodulator for OOK and FSK signals is designed in 65-nm CMOS process for IoT applications. The proposed switched dual-mode demodulator can demodulate both OOK and FSK signals. The designed receiver achieves a NF of 9.9 dB, maximum conversion gain of 74 dB, and IIP3 of −26.3 dBm.

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From 2009 to 2010, he was a Post-Doctoral Researcher with KAIST, where he studied a surface acoustic wave (SAW)-less receiver architectures and developed 5.8GHz RF transceivers for DSRC applications. From 2010 to 2014, he was a Senior Engineer with Samsung Electronics Co. LTD., Suwon, South Korea, where he has been involved with studies of the SAW-less software-defined receivers and development of CMOS transceivers for 2G/3G/4G cellular applications and receivers for universal silicon tuners. In 2014, he joined the Department of Electronics Engineering, Kangwon National University, Chuncheon, South Korea, where he is currently an Associate Professor. His research interests include CMOS mmWave/RF/analog integrated circuits and RF system design for wireless communications.