300-GHz Integrated Heterodyne Receiver Chain for Phased-Array with Wide IF Bandwidth

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***Abstract* – This paper presents a fully integrated terahertz receiver chain for phased-array with a wide IF bandwidth designed using a 250-nm InP double heterojunction bipolar transistor (DHBT) technology. The phased-array receiver chain consists of a variable-gain low-noise amplifier (VG-LNA), phase shifter, down-conversion mixer, and injection locking local oscillator (ILO). Each circuit block is designed to be broadband to achieve a wide receiver chain bandwidth.**

The VG-LNA adopts cascaded amplifying stages with a current steering technique to control the gain. While the control voltage (V_{con}) varies from 2 to 3.6 V, the gain varies from 15.6 to 0 dB at 300 GHz. The noise figure is no higher than 15 dB at all V_{con} conditions. The phase shifter uses a current combining structure based on Gilbert cells. The peak conversion gain is -10 dB at 303 GHz and the 3 dB bandwidth is 52 GHz extending from 270 to 322 GHz. The LO employs an injection locking technique. The locking range is from 260 to 328 GHz (22.7%) when a 10-dBm signal is injected. The maximum output power is 0.5 dBm at 300 GHz. The Gilbert-cell-based down-conversion mixer shows a 72-GHz bandwidth extending from 252 GHz to 324 GHz.

The proposed fully integrated phased-array receiver chain shows a wide bandwidth characteristic. When the control voltage is set to 2.0 V, the peak conversion gain is 12.3 dB and the 3-dB bandwidth reaches 45 GHz from 270 GHz to 315 GHz.

***Keywords*—Injection locking local oscillator, Mixer, Phased array, Phase shifter, Variable gain low-noise amplifier.**

I. INTRODUCTION

Recently, the terahertz band has drawn significant attention because ultra-high-speed wireless communication can be feasible using a wide and unallocated frequency resource. Also, it is an attractive frequency band for various applications such as radar for detection, imaging system, and optical signal processing [1, 2]. However, due to the limited transistor speed and high loss at terahertz band, the design of a wideband wireless communication system operating above the H-band (220–320 GHz) is still challenging. Despite those challenging issues, several terahertz transceivers have been reported [3, 4]. However, those transceivers are inappropriate to beam-forming wireless communication systems because there is no phase shifter integrated to control the phase states.

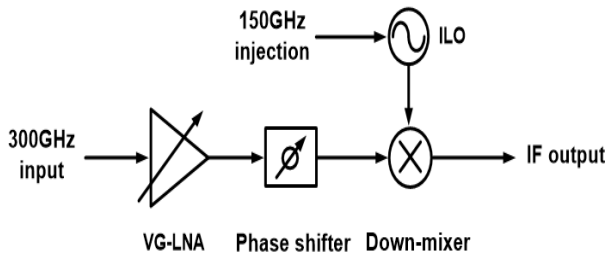

Fig. 1. Block diagram of the 300-GHz phased-array receiver chain.

The terahertz band has high atmospheric absorption and high channel attenuation. Therefore, to overcome the high channel loss, a phased-array system should be employed to implement a terahertz wireless communication system. The phased-array system improves EIPR of a transmitter and SNR of a receiver [2]. As it is essential to maintain uniform magnitude of signal from each array element, a phased array should also include variable gain characteristic. Furthermore, the phased-array system should have a wide operating bandwidth to fully exploit the wideband terahertz spectrum.

In this paper, we designed a 300-GHz wideband phased-array receiver chain which is fully integrated into a single chip using a 250-nm InP DHBT technology. Fig. 1 shows a block diagram of the phased-array receiver chain. The receiver chain integrates a variable-gain low-noise amplifier (VG-LNA), phase shifter, down-conversion mixer and injection-locked local oscillator (ILO). The VG-LNA, phase shifter and down-conversion mixer are designed to be broadband for a wide receiver chain bandwidth. The frequency of the 300-GHz ILO is locked by using a frequency doubler with a 150-GHz injection signal.

The 250-nm InP DHBT technology presents f_{max} of 650 GHz. The process provides four metal layers, a thin-film resistor of 50 Ω/sq, a metal-insulator-metal capacitor of 0.3 fF/μm^2, and a backside via.

This paper is organized as follows. In section II, the design of each circuit block is described together with the simulation results. In section III, the design of a phased-array receiver chain is described along with the simulation results. Lastly, the conclusion is presented in section IV.

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II. CIRCUIT BLOCK DESIGN

A. 300-GHz wideband VG-LNA

A schematic of the VG-LNA is shown in Fig. 2. The first stage also uses a cascode topology for high MAG and low NF. To implement variable gain, the second stage of the VG-LNA adopts a cascode topology with a current steering technique. Lastly, a common-emitter topology is adopted in the last stage to improve the output matching performance. The input is matched for low noise figure and 50-Ω impedance. The output is also matched to 50 Ω. A conjugate interstage matching is fulfilled by L-section lines.

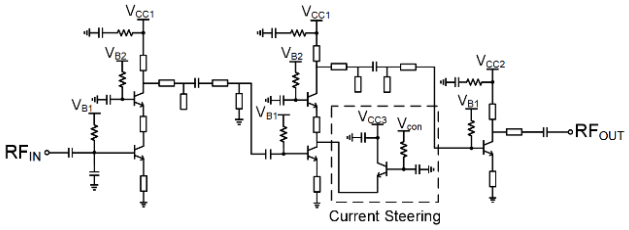


Fig. 2. Schematic of the 300-GHz VG-LNA.

The simulation results of the VG-LNA are shown in Fig. 3. The VG-LNA shows a wide bandwidth performance. When V_{con} of the current steering structure is less than 2 V, $|S_{21}|$ is 15.6 dB at 300 GHz and keeps higher than 12 dB over 247-338 GHz. When V_{con} varies from 2 to 3.6 V, $|S_{21}|$ varies 15.6 to 0 dB and NF varies from 14.1 to 14.6 dB at 300 GHz. Thus, the noise figure does not exceed 15 dB during the control of V_{con}. $|S_{11}|$ and $|S_{22}|$ maintain less than −10 dB from 276 to 328 GHz.

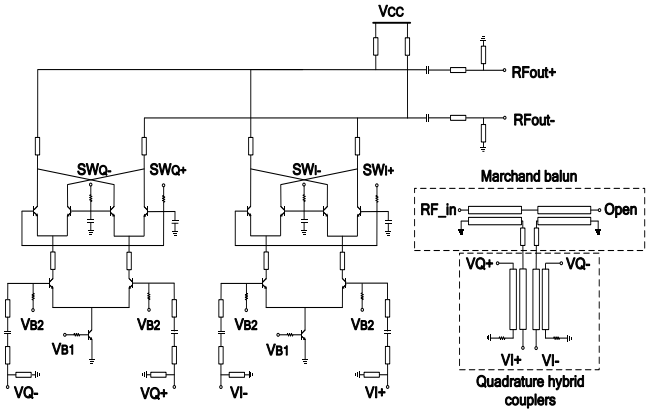
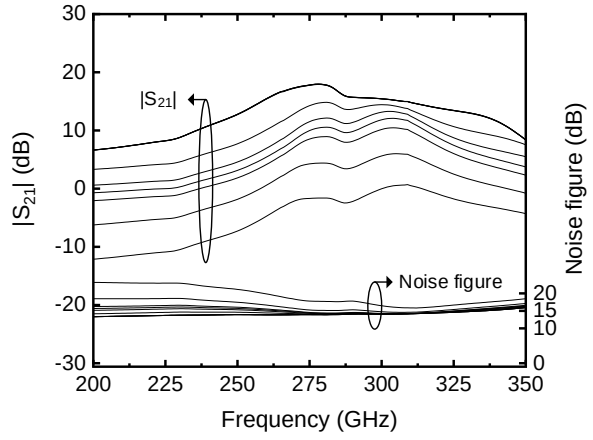
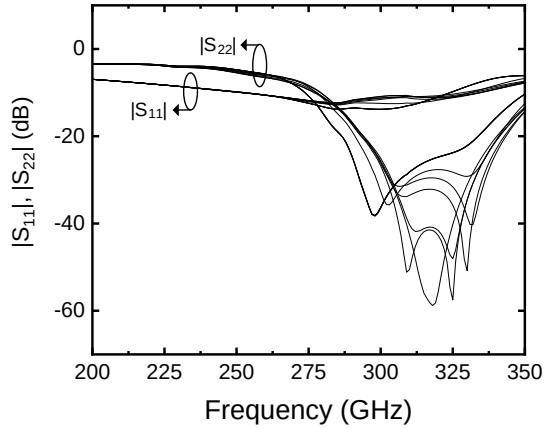


Fig. 4. Schematic of the 300-GHz phase shifter



(a)



(b)

Fig. 3. Simulated (a) $|S_{21}|$, noise figure, (b) $|S_{11}|$ and $|S_{22}|$ of the 300-GHz VG-LNA.

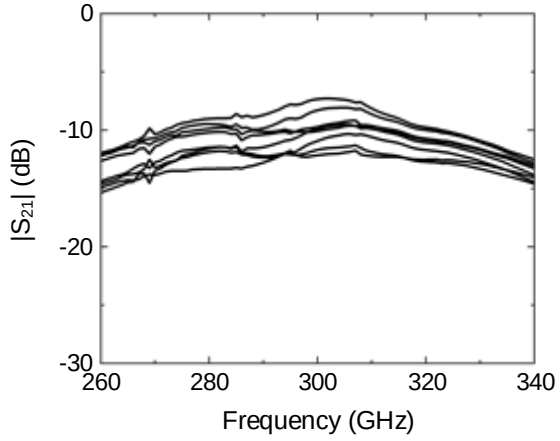


Fig. 5. Simulated $|S_{21}|$ of the 300-GHz phase shifter.

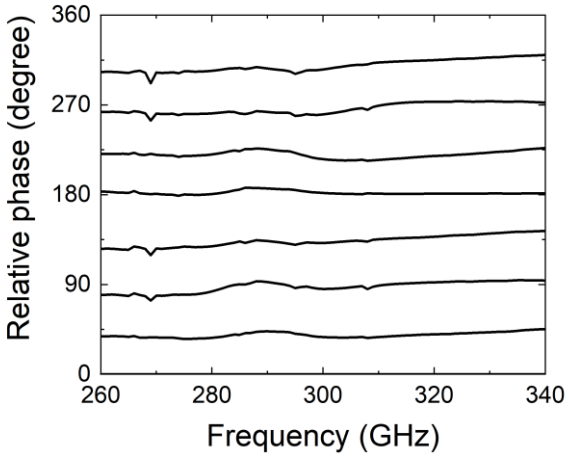


Fig. 6. Simulated phase shift of the 300-GHz phase shifter.

B. 300-GHz wideband phase shifter

A schematic of the 300-GHz wideband phase shifter is shown in Fig. 4. A pair of differential signals is generated by a Marchand balun. Then, each of the differential signals is applied to a quadrature hybrid coupler so that four differential quadrature signals ($V_{Q\pm}$, $V_{I\pm}$) are generated. Two Gilbert cells are combined in a current domain for combining each quadrature signal. The dc current of the Gilbert cells is determined by a tail current source transistor.

By adjusting V_Q and V_I, 3-bit phase states are attained from 0° to 360° at 45° intervals. The $V_{b,on}$ and $V_{b,off}$ are set to 3.5 V and 2.5 V, respectively. To compensate for the phase delay difference that occurred by the balun and hybrid couplers, the lines with different lengths are inserted to the output current combining section. Hence, the output signal of each Gilbert cell is combined without a phase difference, accordingly. The simulated conversion loss of each phase state is shown in Fig. 5. At the V_{Q-} and V_{I-} bias state, the peak gain is -10 dB at 303 GHz and the 3-dB bandwidth is 52 GHz extending from 270 to 322 GHz. $|S_{11}|$ maintains less than − 10 dB from 260 to 340 GHz and $|S_{22}|$ bandwidth, which is under -10 dB is 16 GHz extending from 297 to 313 GHz. Due to the output combining structure of multiple transistors, the output matching is considerably degraded compared to the input matching. The 3-bit phase shift performance is shown in Fig. 6.

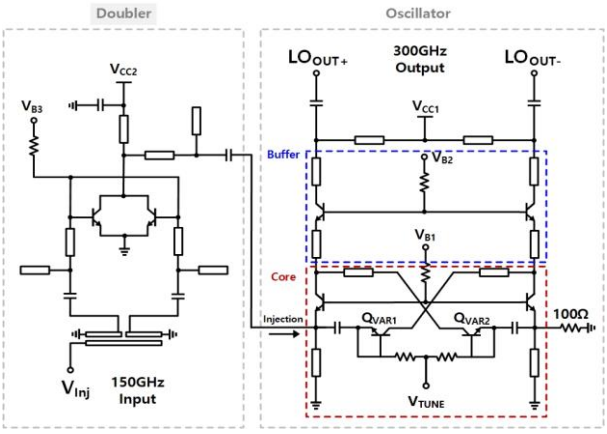


Fig. 7. Schematic of the 300-GHz ILO

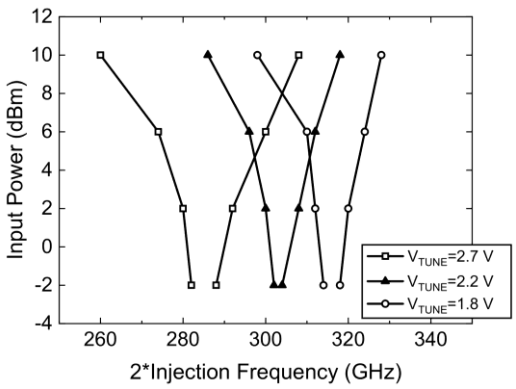


Fig. 8. Sensitivity curve of the 300-GHz ILO

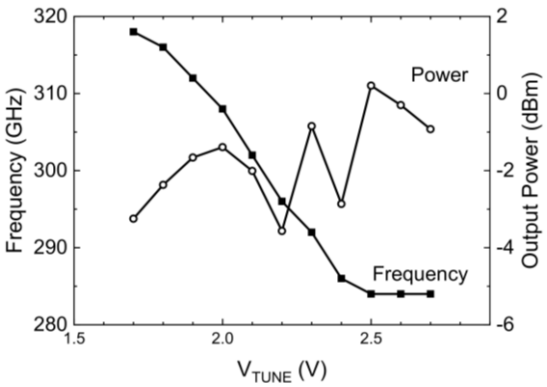


Fig.9. Output power and frequency of the 300-GHz ILO

C. 300-GHz wideband ILO

Fig. 7 shows a schematic of the 300-GHz ILO. A common-base cross-coupled topology is adopted for oscillator core to implement a wide range of negative resistance. For protecting the oscillator core, a common-base stage is used as a buffer between the core and output load. The oscillation frequency is tuned through controlling V_{tune} of the varactor.

A single-ended injection signal at 150 GHz is converted to a differential signal by a Marchand balun. A following frequency doubler generates a 300-GHz signal, which is injected to one port of the oscillator core. To minimize the injection imbalance, a dummy resistance of 100 Ω is loaded to the other port of the oscillator core.

As shown in Fig. 8 and Fig. 9, the tuning range of the free running oscillator is 11.3 % and the maximum power is 0.2 dBm at 284 GHz. The conversion loss of the frequency doubler including the input balun is 8.3 dB. The locking range is from 260 to 328 GHz (22.7%) when a 10-dBm signal is injected. The maximum output power is 0.5 dBm at 300 GHz under the locking condition.

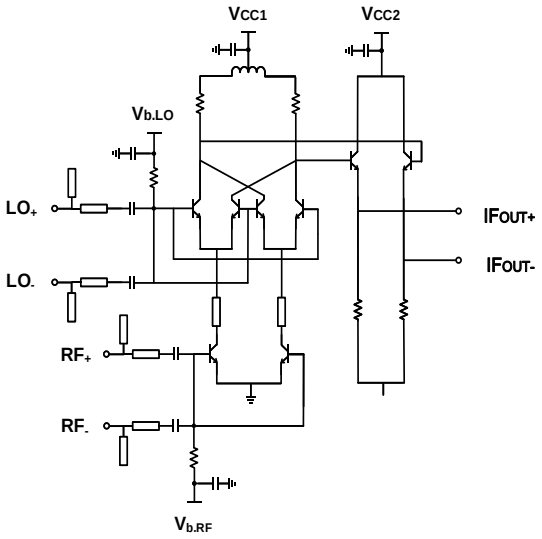


Fig.10.Schematic of the 300-GHz down conversion mixer

D. 300-GHz wideband down-conversion mixer

Fig. 10 presents a schematic of the 300-GHz wideband down-conversion mixer. A Gilbert cell is used as a mixer core for high conversion gain and high port isolation, followed by an emitter follower. The mixer core is pumped by a fundamental LO signal generated by the ILO at 300 GHz. Hence, the transmission lines and open stubs are used for LO and RF ports to be matched to differential 100 Ω. Also, to achieve wideband performance, an inductive peaking technique using a spiral inductor is adopted. The turn number and radius of the spiral inductor are carefully selected considering the IF bandwidth and convenience of layout design. The simulated conversion gain is shown in Fig. 11. The peak gain is 7.4 dB at 266 GHz and the gain bandwidth for 5-dB gain is 72 GHz extending from 252 to 324 GHz. Fig. 12 is the simulated power performance versus the RF input power, showing -7 dBm of IP1dB.

III. 300-GHZ INTEGRATED PHASED-ARRAY RECEIVER CHAIN

A layout of the 300-GHz integrated phased-array receiver chain is shown in Fig. 13. The chip size is 1.2×0.8 mm^2 including probing pads. The VG-LNA, phase shifter, down-conversion mixer, and ILO are integrated in a single chip. To reduce DC bias pads, a resistive bias distributor is used.

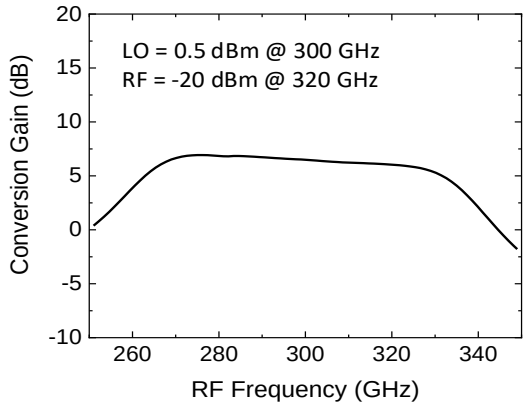


Fig. 11. Simulated conversion gain of the 300-GHz down-conversion mixer

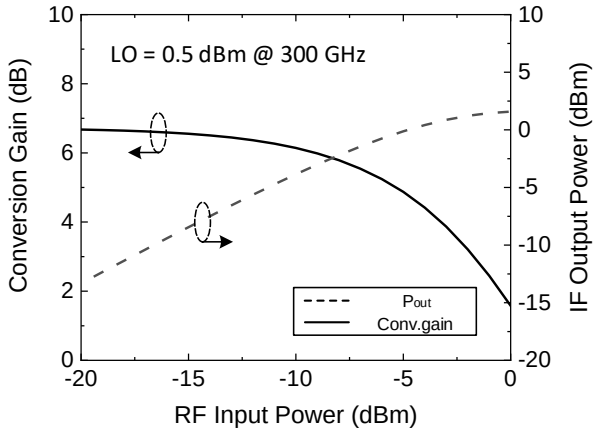


Fig.12. Simulated conversion gain and IF output power of the 300-GHz down conversion mixer

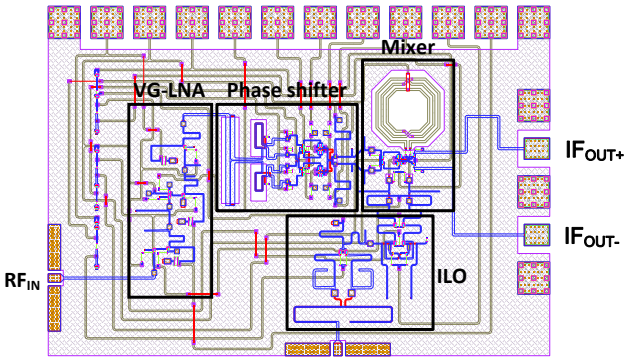


Fig. 13. Layout of the 300-GHz integrated phased-array receiver chain.

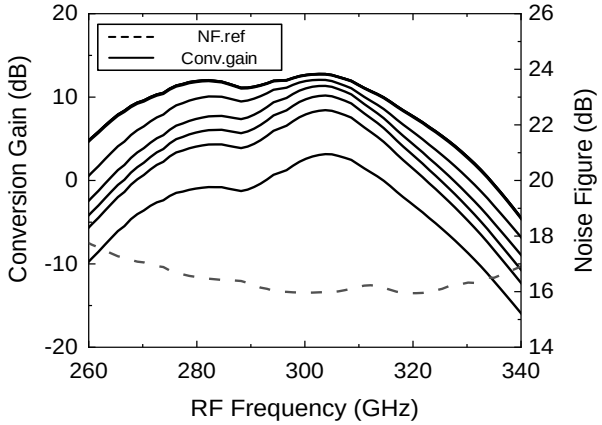


Fig. 14. Simulated conversion gain and noise figure of the 300-GHz phased-array receiver chain when V_{con} varied from 2.0 to 3.6 V.

Fig. 14 represents the conversion gain at various control voltages (V_{con}) of VG-LNA, which vary from 2.0 to 3.6 V at 0.2-V interval. When the reference control voltage is applied, the peak conversion gain is 12.3 dB and the 3-dB bandwidth is 45 GHz from 270 to 315 GHz. The noise figure is below 19 dB over the entire bandwidth. The phased-array receiver chain achieves wideband performance due to the wideband design of each circuit block. The simulated conversion gain versus RF input

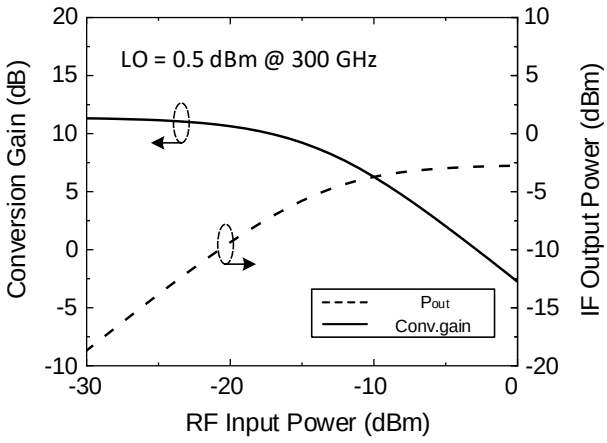


Fig. 15. Simulated conversion gain and IF output power of the 300-GHz phased-array receiver chain.

power at 300 GHz is shown in Fig. 15. The gain begins to be compressed at around -18 dBm. The dc power consumption is 0.3 W.

IV. CONCLUSION

A 300-GHz integrated heterodyne phased-array receiver chain with a wide IF bandwidth is designed in a 250-nm InP DHBT process. The phased-array receiver chain operates at LO frequency of 300 GHz and shows peak conversion gain of 12.3 dB. Also, the 3 dB bandwidth is extended from 270 to 315 GHz and the noise figure is below 19 dB over the entire bandwidth. The proposed phased-array receiver chain can be used for a 300-GHz high-speed wireless communication system.

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REFERENCES

[1] C. Kulesa, "Terahertz spectroscopy for astronomy: From comets to cosmology, " *IEEE Trans. Terahertz Sci. Technol.*, vol. 1, no. 1, pp. 232 –240, Sep. 2011.

[2] S. Kim, J. Yun, D. Yoon, M. Kim, J. S. Rieh, M. Urteaga and S. Jeon, "300 GHz integrated heterodyne receiver and transmitter with on -chip fundamental local oscillator and mixers, " *IEEE Trans. Terahertz Sci. Technol.*, vol. 5, no. 1, pp. 92 –101, Jan. 2015.

[3] M. H. Eissa, A. Malignaggi, R. Wang, M. Elkhouly, K. Schmalz, A. C. Ulusoy, and Dietmar Kissinger, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Sep. 2018.

[4] H. Hamada, T. Tsutsumi, H. Matsuzaki, T. Fujimura, I. Abdo, A. Shirane, K. Okada, G. Itami, H.-J. Song, H. Sugiyama, and H. Nosaka, "300-GHz-band 120-Gb/s Wireless front-end based on InP-HEMT PAs and mixers," *IEEE J. Solid-State Circuits*, vol. 55, no. 9, pp. 2316–2335, Sep. 2020.

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