1-1 MASH based on Pipelined-SAR ADC with a PVT Variation Robust Dynamic Amplifier

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***Abstract* – Noise Shaping-Successive Approximation Register (NS-SAR) Analog-to-Digital Converters (ADCs) offer high SNDR due to low quantization noise and low comparator noise which has NS-capability. However, to achieve high SNDR, the NS-SAR needs a high bit-quantizer rather than high order NTF limited by stability. A high bit-quantizer offers smaller residue at the end of conversion. This problem is again affected by comparator noise same as SAR, although the comparator noise is shaped by given NTF. This work addresses this issue through pipelined MASH structure which allows high SNDR with a low-quantizer and a low oversampling ratio (OSR), maintaining good stability and wide bandwidth (BW). The dynamic amplifier configured in the loop filter enables high speed and low power. Our proposed ADC operates at 100 MS/s, it consumes 1.9 mW from a 1.2 V supply and achieves 86.69 dB-SNDR and 6.25 MHz-BW, when OSR is 8.**

***Keywords*—Analog-to-digital converter (ADC), Multi-stage noise-shaping (MASH), Noise shaping (NS), Pipelined SAR ADC, Successive approximation register (SAR)**

I. INTRODUCTION

In recent years, noise-shaping-SAR analog-to-digital converters (NS-SAR ADCs) have exhibited high signal-to-noise ratio (SNDR) and wide bandwidth (BW) by attenuating comparator noise and quantization noise [1]. Although these benefits relax the conventional SAR ADC disadvantage, the operation amplifier consists of a loop filer that offers power penalty which acts counterpart of low power design. To address this issue, Fully Passive NS-SAR(FPNS-SAR) is another solution that removes the power-hungry amplifier. Although the FPNS-SAR has the ability to power efficiency, the SNDR is degraded by kT/C noise and comparator noise due to high comparator gain. Also, achieving higher SNDR, NS-SAR has a higher quantizer bit rather than high order NTF due to stability. This problem makes smaller residue voltage at the end of analog to digital conversion and thereby needs low comparator noise. These reasons make hard high SNDR in FPNS-SAR.

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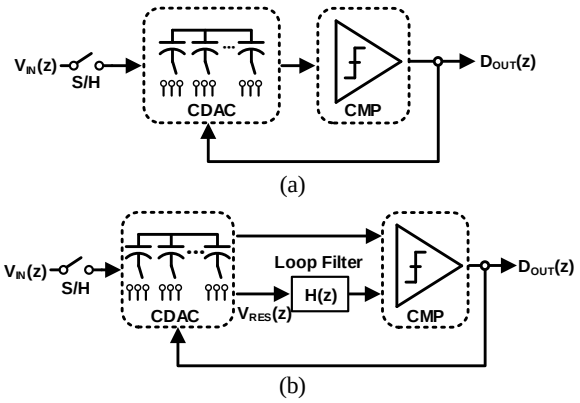

Fig. 1. Block diagram of (a) conventional SAR ADC. (b) NS-SAR ADC.

To solve this limitation, prior works achieved high SNDR by replacing dynamic amplifier with operation amplifier or proposed Major Voting [2] and Tri-level Voting [3] which can reduce the comparator noise. However, NS-SAR consisting of dynamic amplifier achieves high SNDR with low power but still needs high quantizer bit (10 bit) and MV and TLV Logic degrade the performance of BW. In this paper, we propose a pipelined SAR-based 1-1 MASH to achieve high SNDR and wide BW while efficiently lowering the number of quantization bits, which helps to reduce comparator noise. Our prototype maximized SNDR by embedding NS-capability into conventional pipelined SAR ADC. Therefore, our prototype achieves 86.69 dB SNDR with only 5bit, 5bit quantizer for each stage, and 6.25MHz BW. Also, our proposed ADC adopts the dynamic amplifier which proposes a more robust process, voltage, temperature (PVT) variation. Thanks to the dynamic amplifier, our proposed ADC consumes only 1.9 mW power.

II. PROPOSED ARCHITECTURE

A. Review of NS SAR ADC

SAR ADC can be implemented with reasonable resolution, moderate speed, and low power, so many studies are being conducted. However, if a fine quantizer is used to implement high resolution, the comparator noise must be reduced as much as that, so there is a limit. To overcome this, an NS SAR ADC that applies a loop filter to the SAR ADC is being studied. First, Fig. 1 (a) shows a

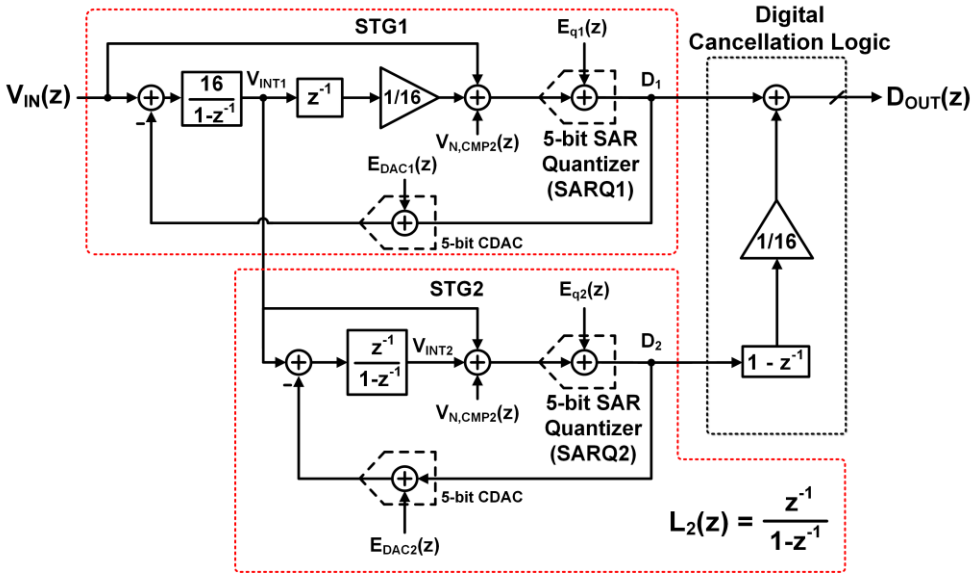

Fig. 2. Proposed ADC block diagram.

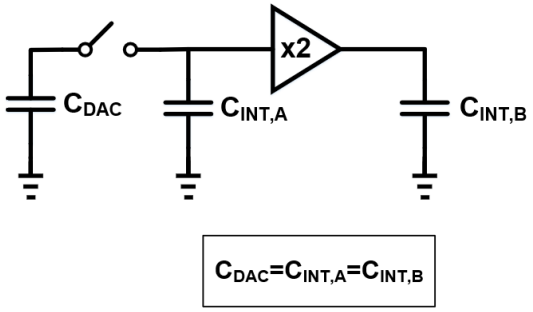

Fig. 3. Proposed integrator circuit implementation.

block diagram of conventional SAR ADC. It operates as follows: First, Capacitive Digital-to-Analog Converter (CDAC) samples the input signal V_{IN}. After the sample phase, D_{OUT} is extracted based on a binary searching algorithm using the CDAC, comparator, and SAR logic. Due to SAR operation,
quantization error ($V_{RES} = V_{IN} - D_{OUT}$) remains in CDAC at the end of the conversion. Fig. 1 (b) shows a block diagram of NS-SAR ADC. It uses V_{RES} for the next conversion and performs noise-shaping by summing V_{IN} and V_{RES} filtered by the loop filter. Through this operation, the NS-SAR ADC effectively suppresses comparator thermal noise and quantization noise of the in-band. Therefore, the NS-SAR ADC achieves high resolution by utilizing NS-capability and oversampling. However, it has a limitation that needs a low-noise comparator due to small V_{RES}. Another way is to increase the order of the noise transfer function to achieve higher resolution. However, this causes stability problems and is difficult to implement. The pipelined structure can be applied together to overcome the limitations of NS-SAR ADC [4]-[6]. However, the prior pipelined NS-SAR ADCs apply NS technique only to the second stage, so there is no noticeable improvement in resolution. Rather, it only causes speed reduction and power consumption improvement due to amplifier. Therefore, this paper proposes a structure that takes advantage of the pipelined structure and minimizes the bottleneck caused by the existing amplifier.

B. 1-1 MASH based on pipelined SAR ADC

We apply NS-SAR ADCs to each stage in pipelined SAR structure as in Fig. 2 [7]. The resulting structure is equivalent to a MASH ΔΣ one, so there needs to be a digital cancellation logic at the end that combines digital outputs from both stages. Each NS-SAR ADC has its integrator as a loop filter, and there is an amplifier between the stages to amplify the integrated SAR residue signal from the first stage (STG1). The amplifier has a gain of 16 (2^5-1) for coarse quantizer resolution N_1 to avoid signal over range, which is a technique often used in conventional pipelined SAR ADCs. Each stage of the integrator (INT1, INT2) consists of a dynamic amplifier and capacitor as shown in Fig. 3. At the end of conversion, capacitor works to sum the residue voltage in C_{DAC} and previous value in $C_{INT,A}$. By amplifying x2 the integrated value, we achieve the first order noise shaping SAR each stage, and each stage transfer function shown as eq. (1), (2). Where L_2 is $z^{-1}/(1-z^{-1})$. After each stage output passes the digital logic cancellation filter as shown in Fig. 2, the final output becomes eq. (3). This eq. (3) offers a lot of information. First, comparator noise of the first stage ($V_{N,CMP1}$) goes to be 0. Unless the noise leakage occurs, this result brings a benefit which saves the power.

$$D_1 = V_{IN} - z^{-1}E_{DAC1} + (1 - z^{-1})\left(E_{q1} + V_{N,CMP1}\right) \quad (1)$$

$$D_2 = V_{INT1} + \frac{L_2}{1 + L_2}E_{DAC2} + \frac{L_2}{1 + L_2}\left(E_{q2} + V_{N,CMP2}\right) \quad (2)$$

$$D_{out} = V_{IN} + E_{DAC1} + \frac{1}{16}(1 - z^{-1})E_{DAC2} + \frac{1}{16}(1 - z^{-1})^2(E_{q2} + V_{N,CMP2}) \quad (3)$$

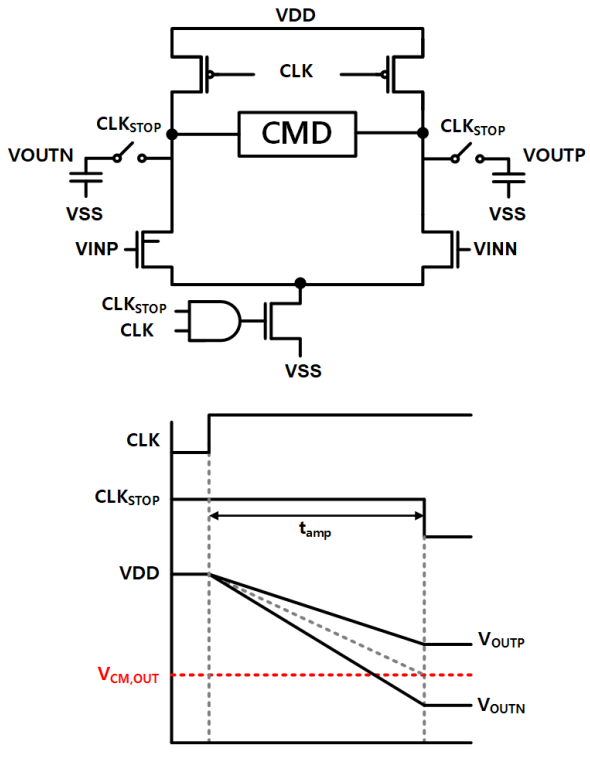

Fig. 4. Conventional dynamic amplifier.

Second, the second stage DAC error from mismatch has inherently NS-capability. This benefit offers PVT robust without DWA, DEM technique. Third, the second stage comparator noise is attenuated by $1/16*(1-z^{-1})^2$. Furthermore, since the lower quantizer bit relaxes the comparator noise, our proposed ADC is hardly not affected by comparator noise compared to prior works [3].

C. Proposed PVT variation robust dynamic amplifier

In a pipelined structure, the residue amplifier is an important block that influences the ADC performance. Only when accurate inter-stage gain is guaranteed, quantization noise and comparator noise in the 1st stage are eliminated. This is the advantage of pipelines that can achieve high resolution. If high gain is not guaranteed, the noise

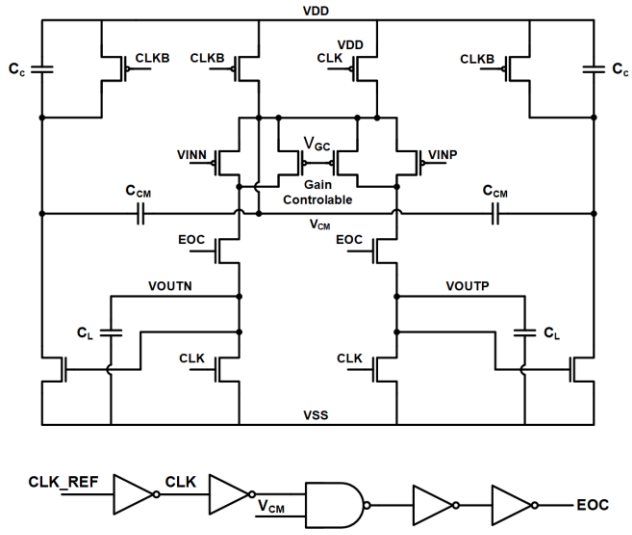

Fig. 5. Proposed PVT variation robust dynamic amplifier.

components of the 1st-stage appear in the form of noise leakage. Therefore, to guarantee high gain, a cascade operational amplifier (OP-AMP) is generally used. However, OP-AMP occupies most of the ADC power consumption due to static power consumption. To compensate for this problem, the proposed dynamic amplifier is used as a residue amplifier instead. Fig. 4 that is the schematic of the conventional dynamic amplifier. Unlike op-amps, dynamic amplifiers do not operate statically, so power consumption can be optimized and can be implemented through a relatively simple structure, so that a large gain can be obtained in terms of area as well. First, during the reset period, the output terminal is charged with VDD. After that, the charged output terminal in the amplification section is discharged, and when the output value meets the desired common voltage, the amplification is ended by making a signal to stop discharging. However, the dynamic amplifier can minimize power consumption, but the gain consists of the trans-conductance and amplification time of the input device, and is very vulnerable to nonlinearity due to PVT variation. Therefore, this paper used a dynamic amplifier with a gain controlling device to

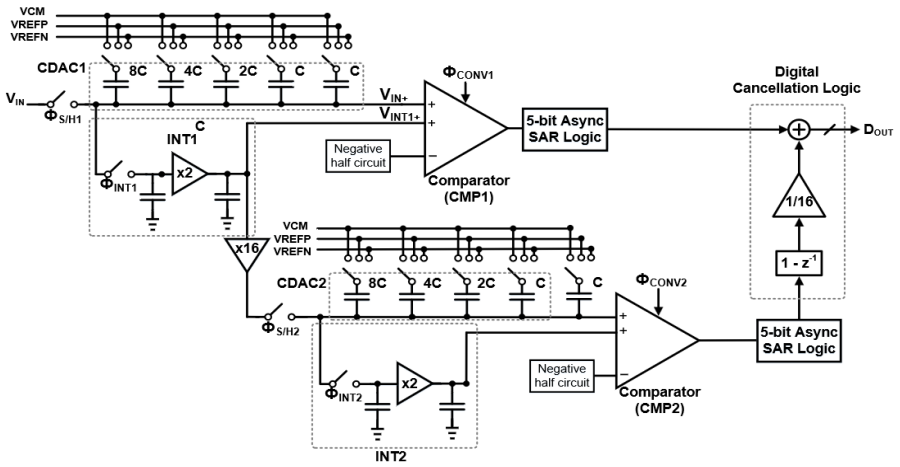

Fig. 6. Top-level circuit implementation of proposed ADC.

compensate for the gain according to the PVT variation. The proposed dynamic amplifier as shown in Fig. 5. Conventional dynamic amplifiers are vulnerable to PVT variation because the gain is determined only by transconductance and amplification time. The proposed structure separates the gain stage and common mode detector circuit in the form of cascode and adds capacitance. Through this, the gain is configured with transconductance and amplification time as well as capacitance, making it more robust to PVT variation. Also, gain error can be compensated by adjusting the V_{GC} of the gain-controlling device.

III. CIRCUIT IMPLEMENTATION

Circuit implementation of the proposed ADC is as shown in Fig. 6. Both stages adopt merged capacitor switching scheme for better energy efficiency, and CDACs and switches are configured accordingly. CMP1 has two input pairs for summing the input and V_{INT1}. The input devices are sized to have 1:1 ratio since V_{INT1} needs to be attenuated by 1, but multiple input pairs of a comparator will generate more thermal noise. To address this issue, additional techniques are often used as in [7] so that comparator thermal noise does not diminish the effect of noise-shaping. In the proposed ADC, noise from CMP1 is canceled out by digital logic, so its input pairs can be freely designed without causing any overhead. Also, the second stage comparator noise does not affect the resolution since noise from CMP2 will be highly suppressed by noise-shaping and the inter-stage gain. Fig. 7 shows the circuit implementation of a multi-input comparator used in the 1st stage. In the 2nd stage, the same structure is used as in the 1st stage. The multi-input comparator is designed considering only the speed and power consumption, and a two-stage dynamic comparator structure, which is power-efficient and has little offset, is adopted. INT1, 2 can be implemented by using a dynamic amplifier for low power consumption and high-speed operation and our dynamic amplifier which is robust to PVT variation minimizes noise leakage by matching analog and digital filters.

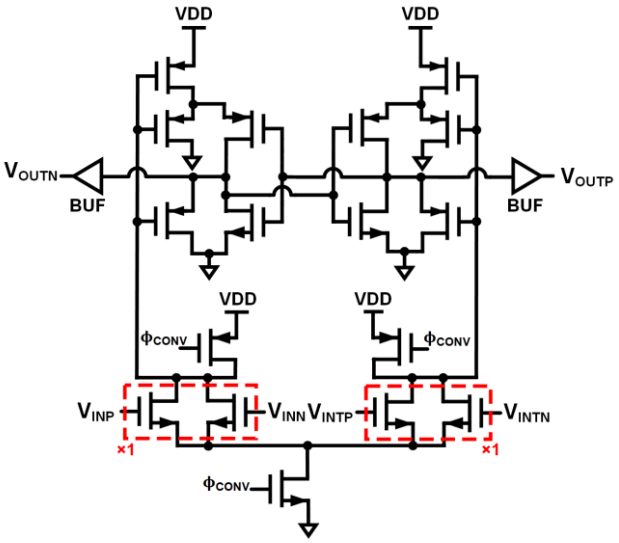

Fig. 7. Multi-input comparator.

IV. SIMULATION RESULTS

The ADC prototype is simulated in 65nm CMOS process and occupies an active area of 390x290um^2. Fig. 8 shows the simulation of power spectral density after digital cancellation process when a 1.73 MHz input tone at -1.1dBFS is applied. The peak SNDR is measured to be 86.69dB with 6.25 MHz bandwidth for OSR of 8 (ideal SQNR is 90dB). The malfunction of the dynamic amplifier embedded between stages degraded the performance of SNDR. The total power consumption is measured to be 1.9mW excluding on-chip regulators and output driving buffers. The dynamic amplifier embedded integrator shows that it minimizes the gain error compared to conventional dynamic amplifier along to corner simulation like Table. 1. Also, as the temperature varies, the gain error is also reduced as shown in Fig. 9. The proposed ADC can achieve high FoM_S (181.6 dB) compared to the prior works as shown in Table II and Fig. 10.

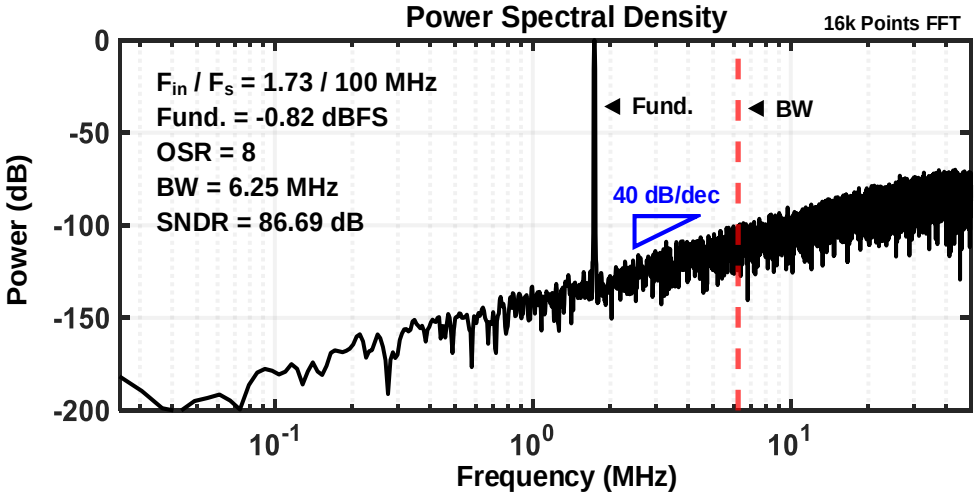

Fig. 8. Simulation result of proposed ADC output power spectral density.

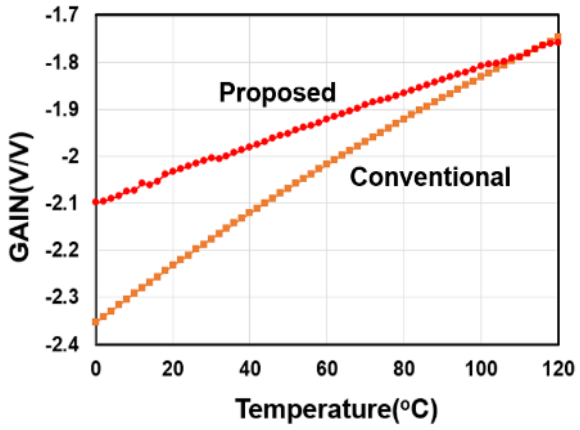

Fig. 9. Simulation result of temperature vs. gain characteristic.

TABLE I. Comparison of corner simulation gain error results.

@ temperature = 27°C	SS	TT	FF
Conventional	-2.6	-2.1	-1.8
Proposed	-2.15	-2.1	-2.01

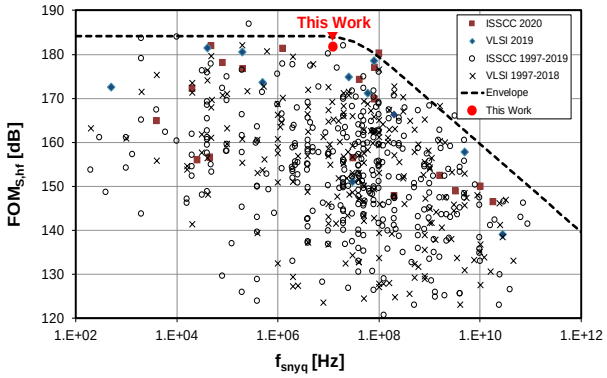

Fig. 10. Bandwidth and FoM_S of ADCs.

V. CONCLUSION

This paper proposes a 1-1 MASH based on pipelined SAR ADC. It can relax comparator noise requirements and achieve high resolution by implementing a 2nd-order noise-shaping. The proposed ADC can also reduce power consumption by using the proposed dynamic amplifier for loop filter. The proposed dynamic amplifier is PVT variation robust, so it ensures good stability compared to prior work.

ACKNOWLEDGMENT

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TABLE II. Performance summary and comparison with the prior work

	This Work	JSSC20 [4]	JSSC20 [5]	JSSC21 [6]
Architecture	Pipelined NS-SAR (1-1 MASH)	Pipelined NS-SAR (0-1 MASH)	Pipelined NS-SAR (0-1 MASH)	Pipelined NS-SAR (0-1 MASH)
Fs (MS/s)	100	200	600	100
BW (MHz)	6.25	12.5	40	6.25
OSR	8	8	7.5	8
Resolution (bits)	10	10	10	11
SNDR (dB)	86.69	77.1	75.2	77.1
Power (mW)	1.9	4.5	2.56	1.38
FoM_S	181.6	171.5	17.1	173.7

$$FoM_S = SNDR + 10 \cdot \log_{10}(BW/Power)$$

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