Frequency Discriminator for the Fine Dust Sensor

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***Abstract* – This work presents a delay-locked-loop (DLL)-based frequency discriminator for a fine dust sensor. Detecting the frequency variations of MEMS resonator according to the fine dust concentration, the proposed frequency discriminator provides digital codes which represents the frequency variations. Since the proposed frequency discriminator is based on the CMOS process, it achieved extremely small area of 0.18 mm^2 and low power of 12 mW, which facilitates the integration into portable device. The proposed DLL-based frequency discriminator covers the input frequency range of 1890 to 2486 MHz with a resolution of 144 kHz, thus it can discriminate input frequencies with 4111 steps. Additionally, to increases the PVT robustness, it used K_{VCDL} compensation technique.**

***Keywords*—Delay-Locked Loop(DLL), Fine dust sensor, Frequency discriminator**

I. INTRODUCTION

Increasing concentration of fine dust is a serious environmental problem these days since it causes respiratory diseases. The problem becomes worse as the industry progresses. Fine dust is tiny dust whose diameter of a particle is smaller than 10um. Then, it cannot be filtered by human organs. Therefore, people with respiratory diseases should avoid going out when its concentration is high. To measure the concentration of fine dust, optical elements are the popular method for the fine dust sensor. However, it has poor accuracy when it detects particles smaller than the wavelength of light [1], and also, according to the direction of light refraction, its accuracy could be worse.

To increase the sensor's reliability, system-on-chip (SoC) based smart integrated circuit (IC) can be an alternative solution. SoC based smart IC consists of detection particles such as MEMS resonators [2] – [4] and the information from the particle is dealt in SoC board. Thanks to high interactivity of a SoC, it has area and cost-efficient characteristics. In this work, we only focused on SoC part, and we assumed MEMS resonators whose frequency is varied with mass exists at the front part of the SoC. Figure 1 shows the MEMS resonators we assumed. When the number of dust increases, which means the concentration of the dust is high, the weight of MEMS resonator increases, then, resonance frequency decreases. In similar way, when the number of dust decreases, the weight of MEMS resonator decreases, then, resonance frequency increases. Then, the following SoC part which is the proposed delay-locked-loop-based frequency discriminator detects the frequency changes in the resonator.

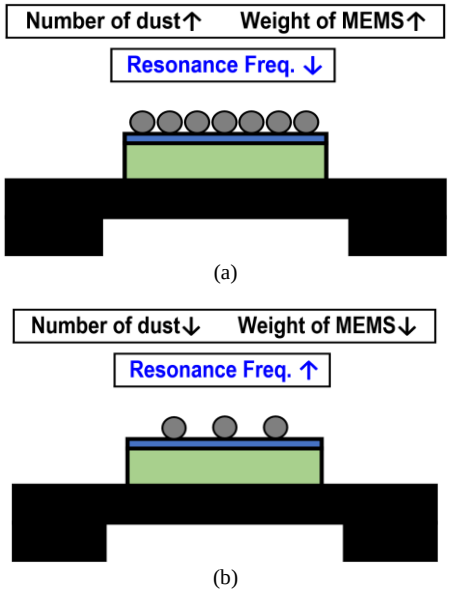

Fig. 1. Operations of MEMS resonators for the fine dust detection in two cases when (a) the number of the fine dust increases and (b) the number of the fine dust decreases.

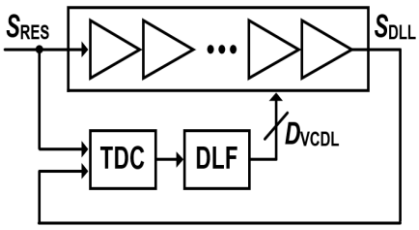

Fig. 2. Basic architecture of a digital DLL.

The rest of this paper is organized as follows. Section II presents the implementation of the proposed delay-locked-loop (DLL)-based frequency discriminator. Section III shows the results and discussion. Section IV provides conclusions.

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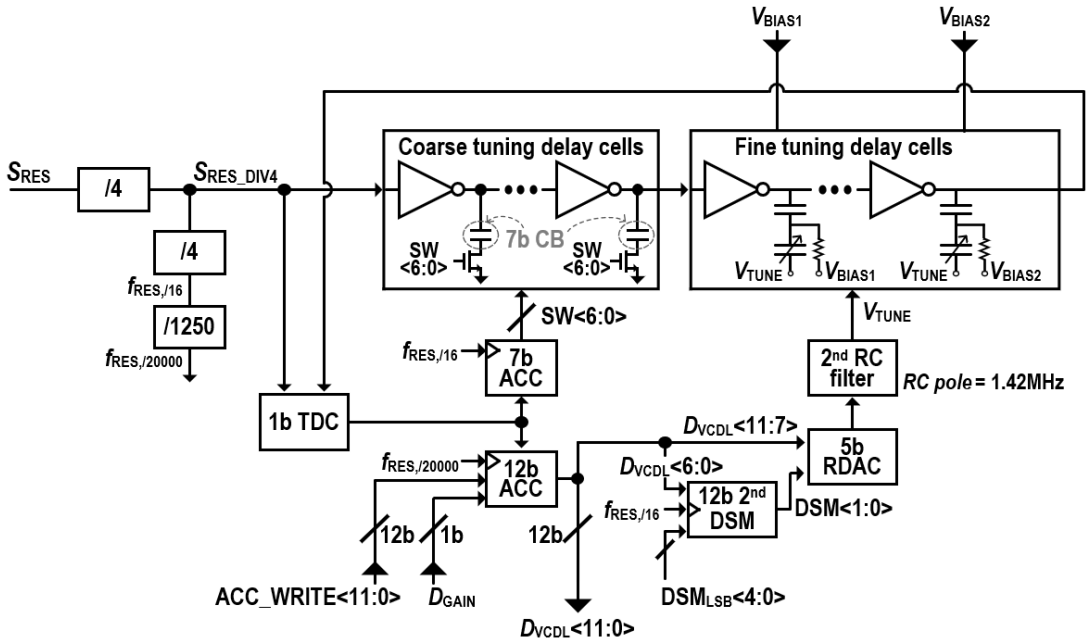

Fig. 3. Overall architecture of the proposed DLL-based frequency discriminator.

II. PROPOSED DLL-BASED FREQUENCY DISCRIMINATOR

A. Basic architecture of a digital DLL

Figure 2 shows the basic architecture of a digital DLL, which consists of delay cells, a time-to-digital converter (TDC), a digital loop filter (DLF) [5]. A DLL has advantages of stability, so it can avoid many design issues in a phase-locked-loop (PLL). However, it is not a frequency multiplier, so its output frequency is same with the input frequency. However, since we want to make a frequency discriminator which is tracking the input frequencies changes. So, a DLL is the proper architecture for our purpose. The operation of the DLL is follows. The TDC detects the delay difference between DLL output, S_{DLL}, and the input clock, S_{RES}, and outputs the difference as a digital code. Then, the code is transferred to the DLF, and the DLF accumulates the code and updates the digital control code of the delay lines of the DLL. Then, the delay of S_{DLL} is calibrated and locked to the period of the S_{RES}. In that situation, the digital code stored in the DLF represents the frequency information of S_{RES}. In this work, we used this characteristic for the input frequency discrimination.

B. Overall architecture of the proposed DLL-based frequency discriminator

The proposed frequency discriminator consists of 7-bit coarse delay cells, fine delay cells, dividers, a 7-bit accumulator (ACC) for the control of coarse delay cells, a 1-bit TDC, a 12-bit ACC for the control of fine delay cells, 4-bit resistor-based digital-to-analog converter (RDAC), a 2nd-RC low-pass filter, a unity-gain buffer, window generators, and a 12-bit 1-1 MASH DSM. MSBs of DSM are from 12-bit ACC, and LSBs of DSM, DSM_{LSB}<4:0> are manually controlled from the outside of the chip. S_{RES} is the input clock of the proposed frequency discriminator, which is assumed as the output of the MEMS resonator. To increase the power efficiency, divide-by-4 divider was used, then, the DLL used S_{RES_DIV4} as an input signal. Input delay ranges of the DLL covers from 1.610 to 2.114 ns which is total 504 ps, which is wide enough to cover the real-time PVT variations. Coarse delay cells cover 304 ps, and fine delay cells covers 200 ps with fine steps, where coarse delay cells are controlled by 7-bit capacitor banks, and fine delay cells are controlled by varactors with K_{VCDL} compensation technique [6].

Figure 4 shows the varactor's K_{VCDL} configurations which are varied as the bias voltage changes to V_{BIAS1} or V_{BIAS2}. Even though one varactor has bell-shaped K_{VCDL} configurations, if we used two different varactors with two different bias voltages of V_{BIAS1} and V_{BIAS2}, we can get the nearly constant K_{VCDL} which is green line of Fig. 4. Using this technique, proposed DLL-based frequency discriminator achieved nearly constant resolution which increases linearity of the fine delay cells. When the fine delay cell's codes are full, then, coarse delay cell's codes are increased. Then, since both cells have same polarity according to control codes, fine delay cells codes decrease

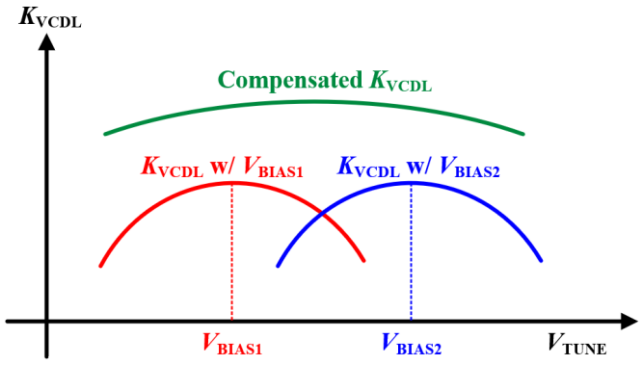

Fig. 4. K_{VCDL} configurations to represent the K_{VCDL} compensation technique.

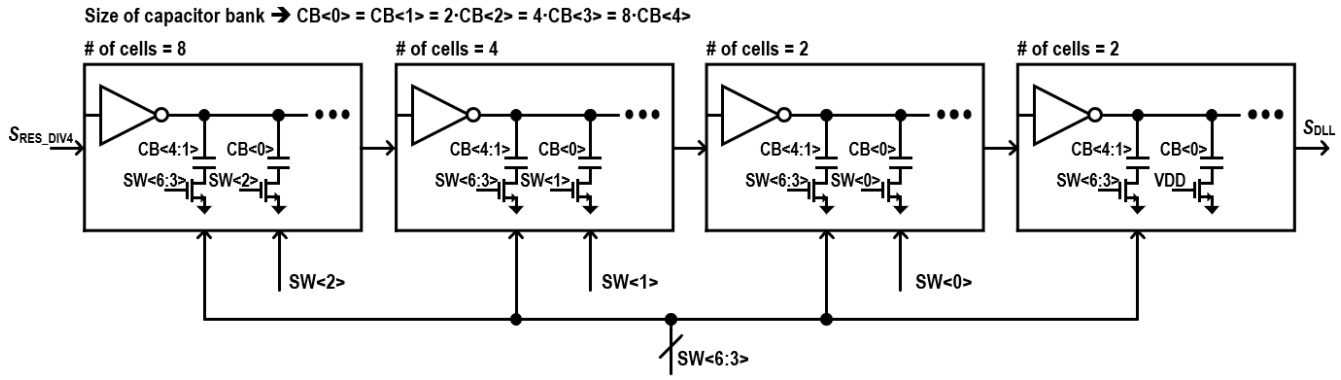

Fig. 5. Implementation of coarse delay cells.

when coarse delay cell's codes increase. By doing so, coarse delay cells increase cover delay range of the fine delay cells.

The operations of the proposed frequency discriminator are as follows. If the frequency of the input signal increases, which means that the fine dust concentration decreases, the 1-bit TDC detects that the delay of the DLL is longer than the period of the input signal, S_{RES_DIV4}. Then, according to the 1-bit TDC's output, the digital code of the 12-bit ACC is updated. The accumulator's digital value is transferred as an analog value through 4-bit RDAC and 2nd-RC filter, which controls the delay of the delay cells to the direction of removing the delay offset between the DLL and the input clock. As a result, after the delay is locked to the appropriate value according to the input signal's frequency, we can get the dust concentration by simply reading the accumulator's digital code number. 12-bit DSM was used to increases the resolution of the fine delay cells, and 2nd-order RC filter was used to reduce large ripples from the DSM operation which can interfere the performance of the proposed frequency discriminator. ACC_WRITE<11:0> was set manually to set D_{VCDL} initially for the convenient measurement. Divide by 4 divider and divide by 1250 divider are used to generate timing signals for the 7b-ACC, 12b-ACC, and 12b 2nd DSM, and unity-gain buffer is used to convert accumulator's digital value to analog value.

C. Implementation of coarse delay cells

Figure 5 shows the implementation of coarse delay cells. It consists of 16 inverter-based delay cells. Among 7-bit of the coarse delay code, 4-bits of MSB, SW<6:3> is connected to all 16 delay cells. To reduce the design burden from parasitic capacitance, 3-bits of LSB are controlled by the number of delay cells to be connected, i.e., SW<2>, SW<1>, and SW<0> are connected to 8 delay cells, 4 delay cells, and 2 delay cells, respectively. Each switch is connected to the gate of NMOS switches which is connected in series with the load capacitance of CB<4:0>, where the capacitor bank has binary sizing, i.e., CB<1> = 2·CB<2> = 4·CB<3> = 16·CB<4>. CB<0> has the same size of CB<1> since CB<0> is connected to only part of delay cells while CB<1> is connected to all 16 delay cells. At the right side two delay cells' CB<0>'s switches' gates are connected to VDD to increases the linearity of total bank.

III. RESULTS AND DISCUSSION

Figure 6 shows the micrograph of the proposed DLL-based frequency discriminator. Fabricated in a 180-nm CMOS technology, it used an active area of 0.18 mm^2. Four same frequency discriminators are merged into same die to increase the accuracy of measurements, and for the measurement, we only used one of four frequency discriminators. Figure 7 and 8 show the measured output DLL codes which represent input frequency changes. The code is the output of 12b ACC, D_{VCDL}, according to the input clock S_{RES}'s frequency, f_{RES}. In Fig. 7, the coarse delay cell's control code, SW<6:0> is 1111111_2, which means it has longest delay. Then, the fine delay cells cover from 1890.0 to 2030.5 MHz. During the range, the DLL output code linearly decreases as the input resonance frequency of MEMS resonator, f_{RES}, increases. Since the fine delay cells covers only 200 ps, the proposed DLL can achieve extremely fine steps which are smaller than 150 fs. When the fine delay cell's control codes are full, the coarse delay cell's control code increases to compensate the fine delay cells. In Fig. 8, the coarse delay cell's control code, SW<6:0> is 0000000_2, which means it has shortest delay. Then, the fine delay cells cover from 2270.0 to 2485.5 MHz. Similarly, the case in Fig. 7, during the range, the DLL output code linearly decreases as the input resonance frequency of MEMS resonator, f_{RES}, increases.

Figure 9 shows transient simulation results which is from a post-layout simulation. It is an output of unity-gain buffer which is connected to the output of RDAC, V_{TUNE}. The highest voltage of RDAC is 1.8-V and the lowest voltage of

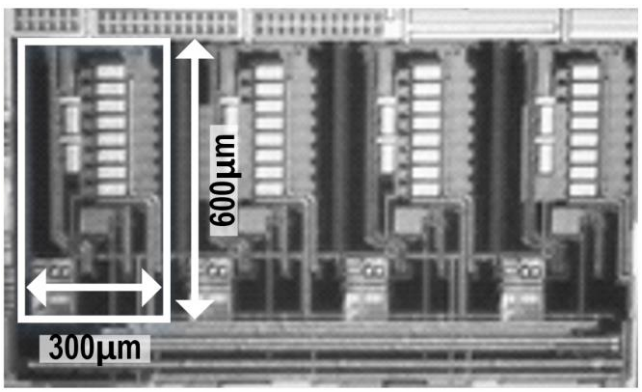

Fig. 6. Micrograph.

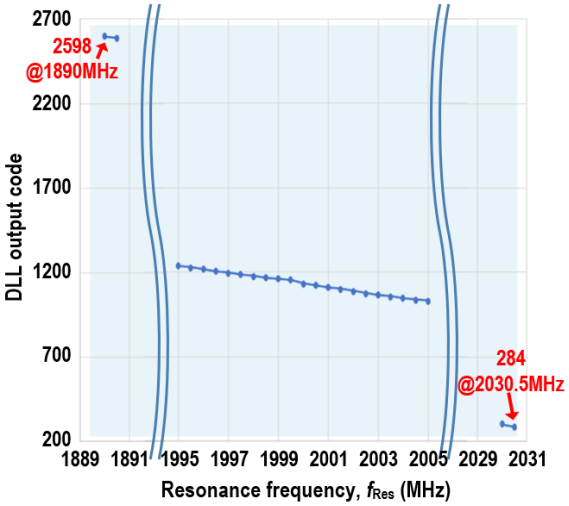

Fig. 7. Measured 12b ACC's output code, D_{VCDL}, according to the input clock S_{RES}'s frequency, f_{RES}, when the coarse delay cell's control code, SW<6:0> is 1111111_2.

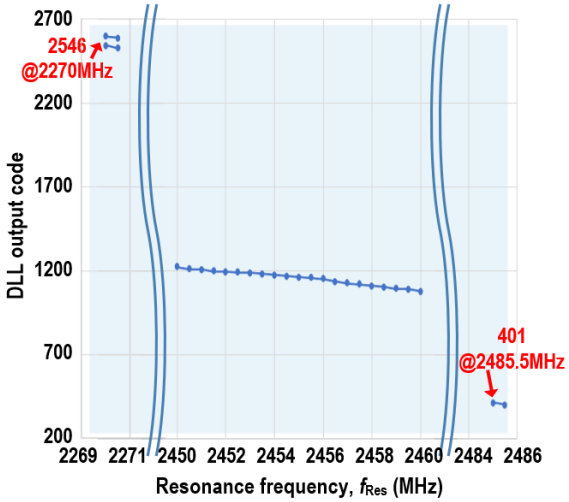

Fig. 8. Measured 12b ACC's output code, D_{VCDL}, according to the input clock S_{RES}'s frequency, f_{RES}, when the coarse delay cell's control code, SW<6:0> is 0000000_2.

RDAC is 0 since the 1.8-V supply was used for the implementation of the proposed frequency discriminator. Then, since the fine control code is 12-bit, the control voltage of fine delay cells, V_{TUNE}, is changed of 0.5 mV per 1-bit. In Fig. 9, first decreases in 10 codes is the process of initial locking. After 100us, the input frequency decreases with 200 kHz steps at 250 us, 350 us, 600 us, and 700 us. At the 480us, the input frequency decreases with 400 kHz steps. Through this, we can also discriminate input frequency with an analog method.

Table I shows the summary of target values and measurement results. Performance metrics are categorized with 5 factors, which are input frequency, output frequency, tuning range, bit number of D_{VCDL}, and the resolution. As echoing other measurement results which are shown in previous figures, the proposed DLL-based frequency discriminator covers input frequency range of 1890 to 2486 MHz, output frequency range of 473 to 621, which is the divided version of the input frequency. The tuning range is 27.06 % which is approximately 10 % wider than the target value. The bit number of D_{VCDL} is 12, and the resolution of D_{VCDL} is 36 kHz.

IV. CONCLUSION

The proposed frequency discriminator was implemented with a simple digital DLL architecture. Except delay lines, other blocks are all synthesized, thus, it achieved extremely small area. To increases the resolution of delay cells, 2nd order DSM was used, and for the linearity, K_{VCDL} compensation technique was used. The proposed frequency discriminator in 180-nm CMOS process consumes only 0.18 mm^2 area and 12 mW of power, where the delay lines consumes 9.5 mW, the digital blocks consumes 2 mW, the RDAC consumes 0.5 mW. Thanks to the high interactivity and low-power architecture, which can reduce the battery size of the sensor, the proposed frequency discriminator is a good candidate for the fine dust sensor market.

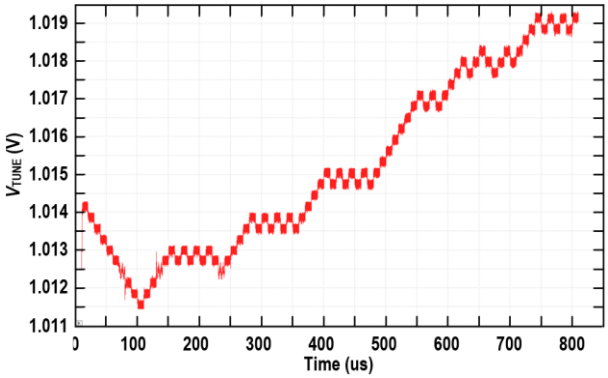

Fig. 9. Transient simulation of V_{TUNE} according to the input frequency changes; input frequency decreases with 200 kHz steps at 100us, 350 us, 600 us, 700us, and 400 kHz steps at 480 us.

TABLE I. The desired specifications and simulation results

Perform. metrics	Target Value	Measurement results
Input frequency (f_{RES})	2000 to 2400 MHz	1890 to 2486 MHz
Output frequency (f_{DLL})	500 to 600 MHz	473 to 621 MHz
Tuning range	18 % <	27.06 %
Bit number of D_{VCDL}	12	12
Resolution	< 50 kHz	36 kHz

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