A Single-Input-Four-Output (SIFO) Switched-Capacitor DC-DC Converter with Ordered-Sequential Switching

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***Abstract* - In this paper, a single-input-four-output (SIFO) switched capacitor DC-DC converter is proposed for low-power SoCs. Ordered sequential switching is proposed for two outputs of the converter to reduce the output ripple voltages and improve current drive capability. In addition, a simple digital regulation loop can be adopted by this technique. The power stage of the converter is composed of 1.8-V/3.3-V transistors, and some of the switches are implemented with 3.3-V native-NMOS to maximize the area efficiency. Moreover, the power efficiency is improved and voltage stress is reduced on the power switches by using a reconfigurable voltage conversion ratio in a wide input range (1.1–1.6 V). The proposed converter has four outputs of 3 V, 2 V, 1.35 V, and 0.9 V with a maximum efficiency of 81% and output ripple voltages less than 50 mV even under a load condition of 100 μA, and produces an output power greater than twice that of existing state-of-the-art converters.**

***Keywords*—Low-power converter, Sequential Switching Scheme, Single-input-four-output Converter, Switched-capacitor DC-DC Converter**

I. INTRODUCTION

In recent years, the need for low-power System-on-a-Chip (SoC) applications has pushed designers toward the use of multiple supply voltages [1], and single-inductor multiple-output (SIMO) switching converters [1]–[10] have been widely used to provide multiple power sources, although the large off-chip inductor is still a problem in terms of area. Unlike a SIMO switching converter, moderate-efficiency and low-cost Switched Capacitor (SC) DC-DC converters are particularly well suited for space-constrained applications. Recently, several SC DC-DC converters with multiple outputs have been proposed [11], [12]. The converter proposed in [11] uses only three flying capacitors for energy harvesting applications to generate two regulated outputs. To reduce the output ripple voltage, they limit the duty cycle for charge transfer to the outputs. However, a duty cycle determined by the input voltage limits the drive capability of the converter. Moreover, 5-V transistors are also required to prevent breakdown of the power switch. The converters described in [12] can generate two outputs by a time-multiplexing technique similar to SIMO. However, this is only applicable to step-down converters.

In this letter, we propose a SIFO SC converter that operates using a new switching scheme — ordered-sequential switching. The proposed switching method is to adjust the switch resistance connected to each output according to the load current. Hence, the duty ratio is not limited, which results in an improvement of the converter's current drive capability with minimum ripple voltage.

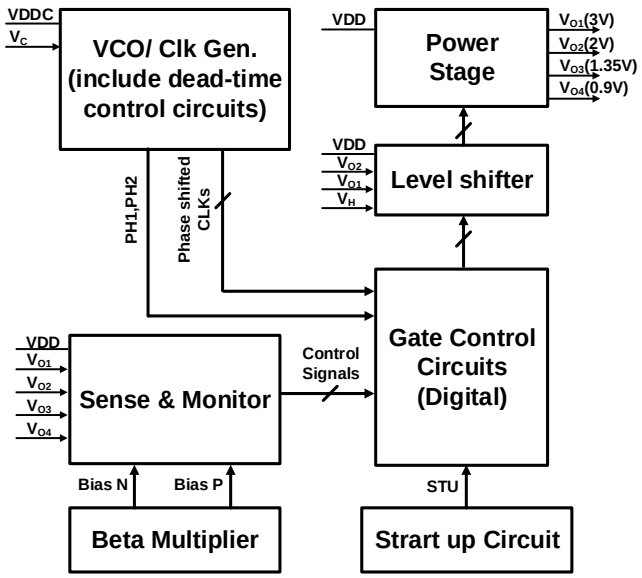

Fig. 1. Top block diagram of the proposed switched-capacitor DC-DC converter.

II. PROPOSED SIFO DC-DC CONVERTER

A. Top Architecture

Fig. 1 shows the block diagram of the proposed SIFO SC sense & monitor, gate control circuits, level shifter, beta multiplier, startup circuit, and power stage. Five flying capacitors, as shown in Fig. 2, are used to generate four outputs (V_{O1}–V_{O4}). The VCO/CLK generator provides system clocks (PH1/PH2) and phase-shifted clocks for the ordered sequential switching function. The Sense & Monitor circuit monitors the four outputs and provides signals to control the duty cycle of the output switches, and determines the voltage conversion ratio(VCR) of the power stage.

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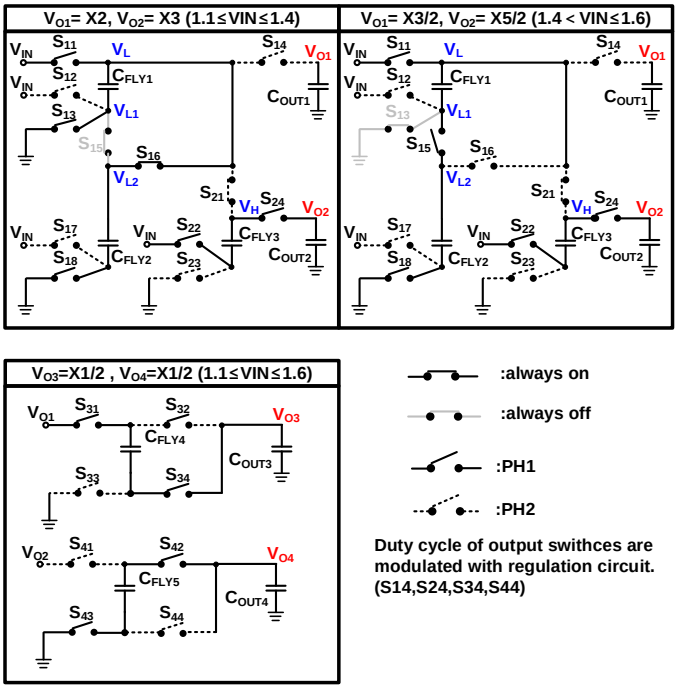


Fig. 2. Switch configuration of the proposed work. Bold lines and dashed lines represent PH1 and PH2, respectively.

B. Power Stage Including Flying Capacitor

Fig. 2 shows the SC power stage, which consists of 20 power switches and 5 flying capacitors. The power efficiency can be increased by changing the VCR according to the input voltage range and by minimizing inevitable charge re-distribution losses. Switches S_{11}, S_{15}, and S_{16}, composed of 3.3 V PMOS, were replaced with native NMOS, which has a negative V_{TH}. This allows for a 50% reduction in the unit switch area. The other switches consist of 1.8 V/3.3 V normal V_{TH} NMOS and PMOS. S_{14} and S_{24} are divided into three parts for ordered sequential switching. Output voltages V_{O1} and V_{O2} can be regulated to 3 V and 2 V, respectively. V_{O3} and V_{O4} can be produced by using regulated outputs of V_{O1}, and V_{O2}, and a 2:1 step-down converter

C. Proposed Ordered-Sequential Switching

SC converters can be modeled using an ideal transformer with a turns ratio equal to the no-load conversion and the output resistance, R_{OUT} [13]. For output voltage regulation, R_{OUT} must be appropriately modulated according to the load current. R_{OUT} can be expressed by a relationship between the asymptotic slow switching limit (R_{SSL}) and the asymptotic fast switching limit (R_{FSL}), as shown in (1). R_{SSL} is a resistance that occurs during the charge transfer state of a capacitor and is inversely proportional to the frequency. R_{FSL} represents a fixed resistance component independent of frequency, such as power switch resistance and inter-connection metal resistance. In this work, ordered sequential switching is proposed to modulate R_{FSL} and R_{SSL} simultaneously; R_{SSL} is modulated by using pulse skipping with comparators and a digital feedback loop. Ordered sequential switching is applied to the output switches connected to V_{O1}/V_{O2} (S_{14}/S_{24} in Fig. 2). Fig. 3 show the the output switch configuration of V_{O1} and the operation at different load conditions. Considering the load current, the size of each output switch is weighted by the ratio of S_{14_1}:S_{14_2}:S_{14_3}=1:2:5 (6 mm, 12 mm, and 30 mm of width are applied to the switches of V_{O1}) and is turned on at different times. The effective on-resistance of the power switches (R_{SW_eff} in (4) represents the resistance in the case when all switches are in the on state) is modulated as inversely proportional to the load current by applying ordered sequential switching. Above, ΔV_O, I_{CO}, I_{T0}, I_L, and VCR denote the voltage change of the output, current of the output capacitor current of the output switch, load current, and VCR in the charging phase, respectively.

At the light load condition, only S_{14_1} is operated with the highest R_{SW_eff}. In contrast, switches S_{14_1}–S_{14_3} are turned on and have the lowest R_{SW_eff} at the heavy load condition. This technique provides the following advantages: 1) utilization

$$R_{OUT} \approx \sqrt{R_{SSL}^{\ 2} + R_{FSL}^{\ 2}} \tag{1}$$

$$\Delta V_o = \frac{I_{CO} \cdot t_{on}}{C_o} = (I_{T0} - I_L) \cdot \frac{t_{on}}{C_o} \tag{2}$$

$$\Delta V_o = \left\{ \left(\frac{VCR \cdot V_{IN} - V_O}{R_{SW\_eff}} \right) - I_L \right\} \cdot \frac{t_{on}}{C_o} \tag{3}$$

$$R_{SW\_eff} = R_{P1} // \left(\frac{D \cdot R_{P2}}{D - 0.5} \right) // \left(\frac{D \cdot R_{P3}}{D - 0.83} \right), D > 0.83, \tag{4}$$

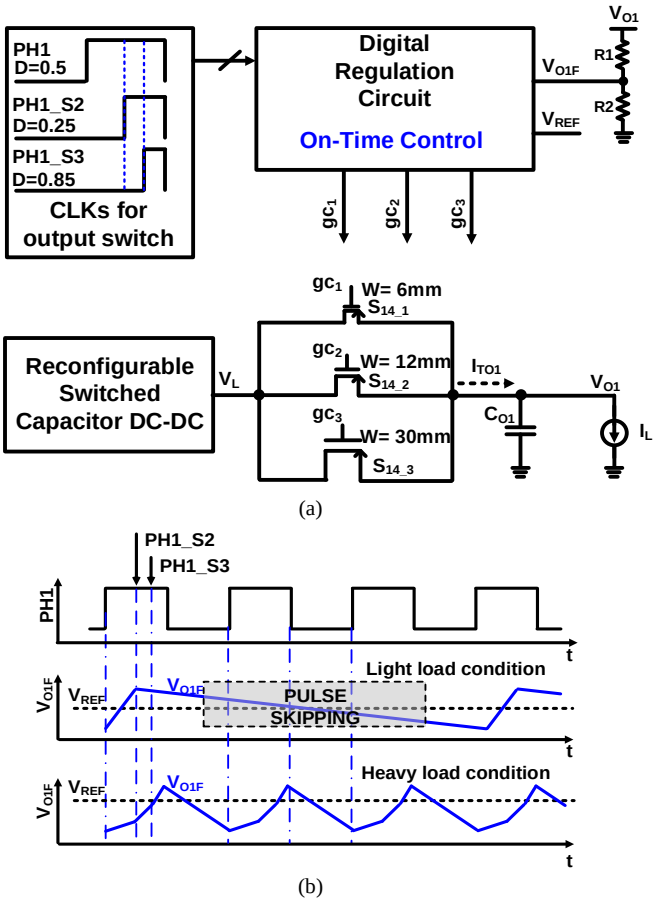


Fig. 3. Ordered-sequential switching configuration with feedback loop and output voltage at different load condition of V_{O1}; (a) regulation circuit for V_{O1}, and (b) waveforms of V_{O1F} under various load conditions.

of the entire duty cycle, 2) fast load transient characteristics, 3) regulation with small ripples by slow changes in the output voltage, and 4) reduction of in-rush current by charge redistribution.

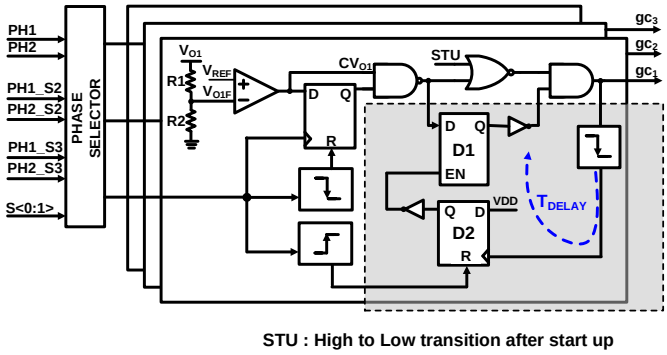


Fig. 4. Digital controller for V_{O1} regulation.

D. Digital Feedback Loop for Output Voltage Regulation

The feedback loop for V_{O1} is shown in Fig. 4. When the feedback voltage of V_{O1} (V_{O1F}) is greater than the reference voltage (V_{REF}) at the rising edge of PH_1, the comparator and combination logic gates turn on switch S_{14_1} connected to V_{O1}. If V_{O1} is less than the reference voltage in a given time, S_{14_2} and S_{14_3} will be turned on sequentially to provide more charge to the output, depending on the load current. The gated D-latch (D1), D-FF (D2), falling-edge detector, and two inverters comprise the T_{DELAY} path represented in Fig. 4. The rising/falling-edge detectors introduce a short pulse at the rising/falling edge. When V_{O1F} is greater than V_{REF}, switches are turned off and V_{O1F} starts to decrease. At that time, the falling edge detector enables the clock signal and sets the gate signal to V_{DD} for the rest of the charging time. The T_{DELAY} path increases the ripple voltage by a small amount but prevents any additional switching within the charging phase. The feedback loop is connected to all the output power switches connected to the outputs of V_{O1}, V_{O2}, V_{O3}, and V_{O4}.

E. Design of Level Shifter and Buffer

When V_{DD} is 1.4 V, the VCRs of V_{O1} and V_{O2} are x2 and x3, respectively. Therefore, V_H shown in Fig. 2 can increase to 4.2 V. Hence, the floating level shifting circuit is implemented to prevent any damage to S_{21} by allowing it to swing from V_{DD} to V_H. Fig. 5 shows the regulating circuit and its waveforms. For the same reason, a level shifting swing circuit between V_{DD} and V_{O1} is used for S_{24}.

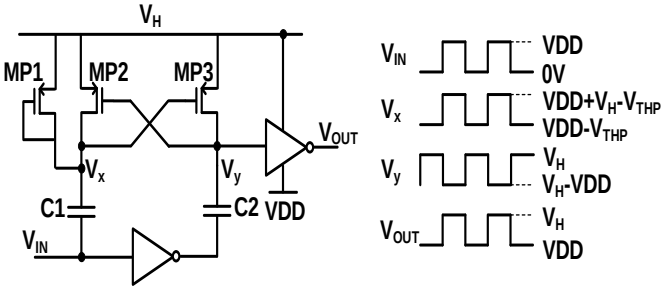


Fig. 5. Floating-ground level shifter used to prevent damage.

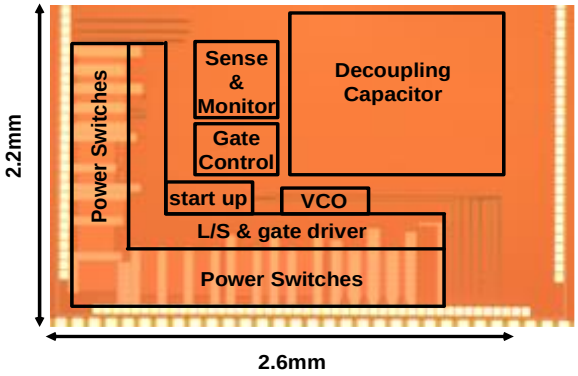


Fig. 6. Chip micrograph.

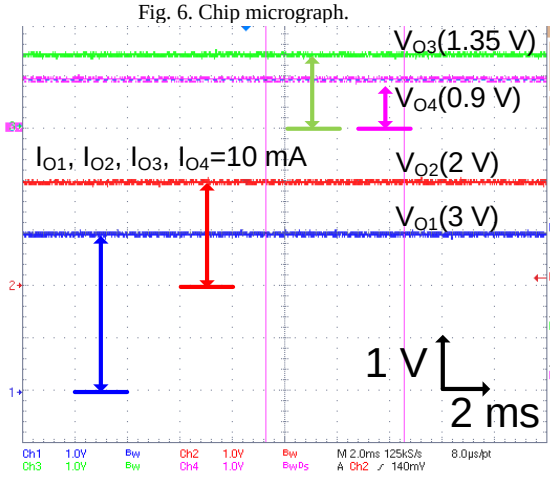


Fig. 7. Measured waveforms of the output voltages with (V_{DD}=1.4 V).

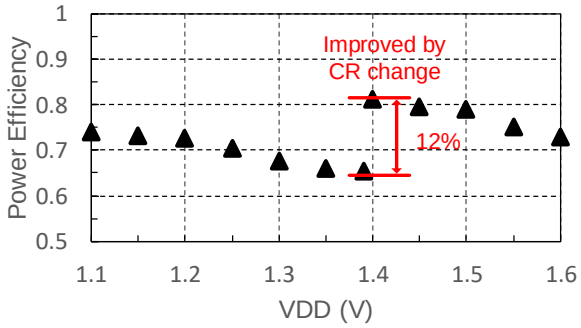
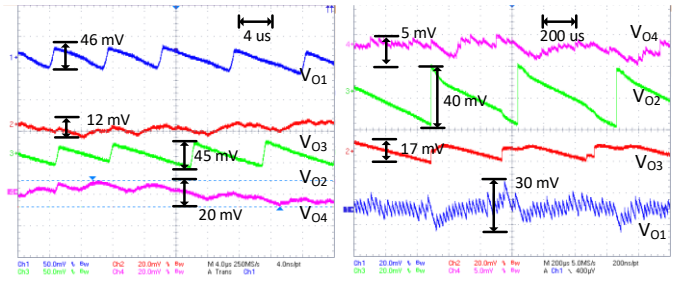


Fig. 8. Efficiency curve of the proposed SC converter at various input voltages (total load current=20 mA).

III. RESULTS AND DISCUSSIONS

The proposed converter is implemented using 0.18 μm standard 1.8-V/3.3-V CMOS technology. For the flying capacitor and output capacitor, MLCC-type 1-μF and 4.5-μF capacitors are used, respectively. Fig. 6 shows the chip micrograph, and the DC output voltages of the converter are shown in Fig. 7 (V_{O1}=3 V, V_{O2}=2 V, V_{O3}=1.35 V, and V_{O4}=0.9 V). The peak efficiency of the proposed SC converter is 81%, where each output delivers 20 mA, as shown in Fig. 8, with the ripple voltage under 50 mV for the entire load range (100 μA–20 mA). The largest ripple voltage value measured was 46 mV, and Fig. 9 shows the measured ripple voltage when the same 100 μA and 10 mA load currents were applied to all outputs with V_{DD} = 1.3 V. Using the proposed ordered switching design, the output

power of the proposed SIFO is increased more than twice with only a 46-mV ripple voltage compared to existing state-of-the-art converters. Finally, Fig. 10 shows the voltages of V_{O1} and V_{O2} according to the measured load transient response when all loads are changed from 100 µA to 20 mA, and indicates a 5% load regulation based on a 2-V output voltage at V_{O2}.



(a) (b)

Fig. 9. Ripple voltages of the proposed SC converter with (a) V_{DD}=1.3 V, I_{O1}–I_{O4}=10 mA, and (b) V_{DD}=1.3V, I_{O1}–I_{O4}=100 µA.

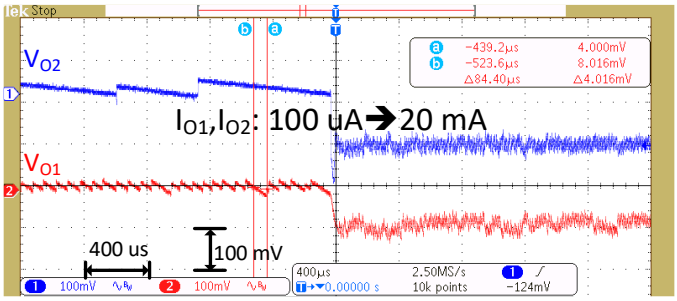


Fig. 10. Transient response of the proposed SC converter (V_{DD}=1.2 V).

TABLE I. Comparison of previous works for low-power applications

	JSSC 15 [11]	ESSCRIC 12 [12]	Proposed
Process [nm]	350	90	180
Application	Energy Harvesting	Ultra-Low Power	Low-Power SoCs
Input (V)	1.1–1.8	1.2	1.1–1.6
Output (V)	2, 3	0.755, 0.32	2, 3, 1.35, 0.9
No. of output	2	2	4
Max. Output Power (mW)	60 (12 mA per output)	1	145 (20 mA per output)
No. of Flying Cap.	2	4	5
Peak Eff. (%)	90	75.3	81
Max. Ripple (mV)	50	N.A.	45

IV. CONCLUSION

A SIFO SC converter with ordered sequential switching, which has a drive capability of 20 mA for each output with less than 50 mV output ripple voltage, is presented in this letter. The reconfigurable scheme is used to improve the efficiency of the converter in the input voltage range between 1.1 V and 1.6 V, and exhibits 81% peak efficiency. The high-current capability of the proposed converter facilitates two more outputs using a regulated output voltage. Moreover, the floating ground level shifter can prevent damage to the switches using only a 1.8-V/3.3-V transistor.

ACKNOWLEDGMENT

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REFERENCES

[1] D. Ma, W. H. Ki, and C. Y. Tsui, “A pseudo-CCM/DCM SIMO switching converter with freewheel switching,” *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.

[2] Y. J. Woo, H. P. Le, G. H. Cho, and S. I. Kim, “Load-independent control of switching DC-DC converters with freewheeling current feed-back,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2798–2808, Dec. 2008.

[3] D. Ma, W.-H. Ki, C.-Y. Tsui, and P. K. T. Mok, “Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode,” *IEEE J. Solid-State Circuits*, vol. 38, no.1, pp. 89–100, Jan. 2003.

[4] K.-C. Lee, C.-S. Chae, G.-H. Cho, and G.-H. Cho, “APLL-based high stability single inductor 6-channel output DC-DC buck converter,” in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 200–201, Feb.2010

[5] T.-Y. Goh and W. T. Ng, “Single discharge control for single-inductor multiple-output DC-DC buck converters,” *IEEE Trans. Power Electron*, vol. 33, no. 3, pp. 2307–2316, Mar. 2018.

[6] H. Chen, Y. Zhang and D. Ma, "A SIMO Parallel-String Driver IC for Dimmable LED Backlighting with Local Bus Voltage Optimization and Single Time-Shared Regulation Loop," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 452–462, Jan. 2012.

[7] W. C. Chen, Y. P. Su, T. C. Huang, T. W. Tsai, R. H. Peng, K. L. Lin, K. H. Chen, Y. H. Lin, C. C. Lee, S. R. Lin, T. Y. Tsai, “Single-inductor Quad-Output switching converter with priority-scheduled program for fast transient response and unlimited load range in 40 nm CMOS Technology,”, *IEEE J. Solid-State Circuits*, vol. 50, no.7, pp. 1525–1539, Apr. 2015.

[8] S. Li, Y. Guo, S. C. Tan, S. Y. Hui, “An off-line single-Inductor multiple-output LED driver with high dimming precision and full dimming range,” *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4716–4727, Aug. 2016.

[9] Y. C. Lin, Y. K. Luo, K. H. Chen, and W. C. Hsu, “Liquid crystal display (LCD) supplied by highly integrated dual-side dual-output switched-capacitor DC-DC converter with only two flying capacitors,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 2, pp. 439–446, Feb. 2012.

[10] Y. Zheng, M. Ho, J. Guo, K. N. Leung, “A single-inductor multiple-output auto-buck-boost DC-DC converter with tail-current control,” *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7857–7875, Nov. 2016.

[11] Z. Hua, H. Lee "A reconfigurable dual-output switched-capacitor DC-DC regulator with sub-harmonic adaptive-on-time control for low-power applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 724–736, Mar. 2015.

[12] N. D. Clercq, T. V. Breussegem, W. Dehaene, and M. Steyaert, "Dual-output capacitive DC-DC converter with power distribution regulator in 90 nm CMOS," in *Proc. Eur. Solid-State Circuits Conf*., 2012, pp. 169–172.

[13] M. Seeman and S. Sanders, "Analysis and optimization of switched capacitor dc-dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

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