22.5–27 GHz High Suppression Frequency Tripler with Excellent Output Power Flatness in 65nm CMOS

Jeong Taek Son[1], Han Woong Choi and Choul Young Kim[a]
Department of Electronics Engineering, Chungnam National University
E-mail : [1]sonkku13@naver.com

***Abstract*—This paper presents a high harmonic suppression frequency tripler with an excellent output power flatness in 65nm CMOS process. In order to achieve a high first, second and forth harmonic suppression, the highly balanced different transformer is employed. The proposed tripler multiplies 7.5 - 9GHz to 22.5 - 27 GHz with ±1.5-dB ripple. It suppresses the harmonic up to 40-dBc and consumes a DC power of 20 mW at a maximum operating point. The tripler occupies a 0.259 × 0.742 mm2.**

***Keywords*—5G, CMOS, Frequency multiplier, Tripler, Harmonic suppression**

I. INTRODUCTION

Recently, as 5G wireless communication technology develops, the demand for it is increasing. 5G wireless communication requires higher speeds and higher bandwidths than previous generations. Therefore, research on a circuit in the millimeter wave band of 24 − 30 GHz that can meet these demands is actively underway. Operation in the mm-wave band can secure a wider bandwidth and implement a smaller chip size. However, in mm-wave, high-performance receiver front-end implementation has difficulties due to additional loss and noise due to high frequency. In particular, it is very difficult to implement a signal source that guarantees a high frequency bandwidth and a precise frequency adjustment performance with low noise to create a local oscillator frequency used for frequency conversion. As an alternative to this problem, when setting a signal source frequency in a high frequency band, it is advantageous to construct a system using a precise frequency source designed at a low frequency and a frequency multiplier, and such a method is widely used. [1]-[2] By multiplying the frequency using a PLL implemented at a low frequency, both stability and high operating frequency can be satisfied. However, the efficiency of the frequency multiplier also decreases when the multiplication factor increases, and the frequency multiplication of more than 3 times in the mm-wave band has a problem of additional power consumption as it is difficult to secure conversion gain without an amplifying stage. The third harmonic conversion efficiency due to the mixing of harmonics is an important performance characteristic.

a. Corresponding author; cykim@cnu.ac.kr,

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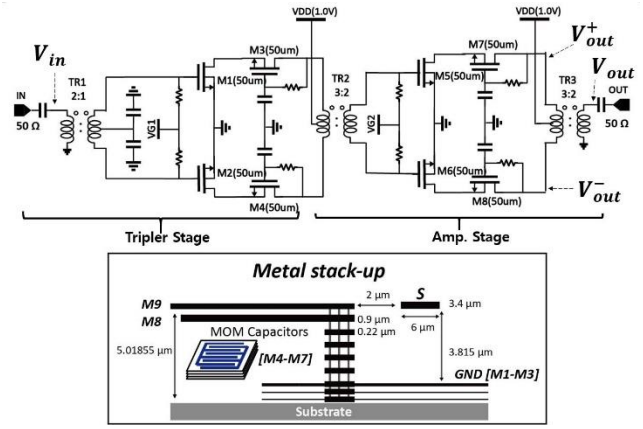


Fig. 1. Schematic of the frequency tripler

This paper presents a high harmonic suppression frequency tripler with an excellent output power flatness in 65-nm CMOS process. In order to achieve a high harmonic suppression, a highly balanced transformer is employed with a differential topology.

II. CIRCUIT DESIGN

A. Topology

Fig. 1 shows the schematic of the frequency tripler to multiply 7.5-9GHz to 22.5-27GHz band signal. In the 1st tripler stage, the 3rd harmonic differential signal is generated, and in the 2nd amp stage, the 3rd harmonic signal is amplified. The input transformer is used to apply a differential signal from the input signal, and each signal is split into opposite phases. The signal generates harmonics due to nonlinear elements, and the output of the differential structure can be expressed by the following equation:

$$V_{in} = \mathrm{A}\cos\omega_{f_0}t \quad (1)$$

$$V^+_{out} = k_1V_{in} + k_2V_{in}^2 + k_3V_{in}^3 + \cdots \quad (2)$$

$$V^-_{out} = k_1(-V_{in}) + k_2(-V_{in})^2 + k_3(-V_{in})^3 + \cdots \quad (3)$$

$$V_{out} = 2k_1V_{in} + 2k_3V_{in}^3 + \cdots \quad (4)$$

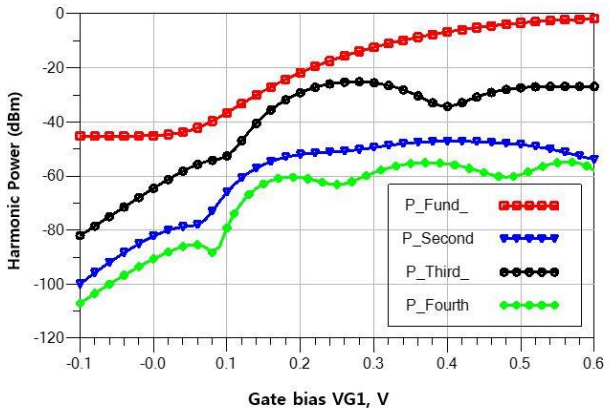


Fig.2. Change of harmonic power of the 1st tripler stage according to transistor gate voltage

Fig. 3. Gain(S21) of the 2nd amp stage

where k_1, k_2, k_3 are constants. The tripler has a differential push-pull operation, and the two differential output signals V_{out}^{+} and V_{out}^{-} shown in Fig.1 can be expressed by eq.(2) and eq.(3). The two signals are converted into single-ended output V_{out} by the output transformer, and the single-ended output remains only odd-harmonic as shown in eq.(4), and the even-order harmonic signal is cancelled.

The tripler of the first stage is a cascode configuration of transistors M1, M2, M3, and M4, and the size is the same as 25 fingers of 2μm. The Transistor M1 and M2 generate harmonic signals due to their nonlinear characteristics, and the M3 and M4 transistors act as CG amplifiers to compensate for the conversion loss to the harmonic signal. The first tripler stage is biased to Class-C with a gate bias of 0.26V after the threshold voltage of 0.38V at the supply voltage of 1V to achieve higher conversion efficiency.

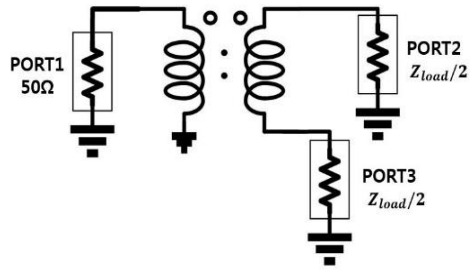
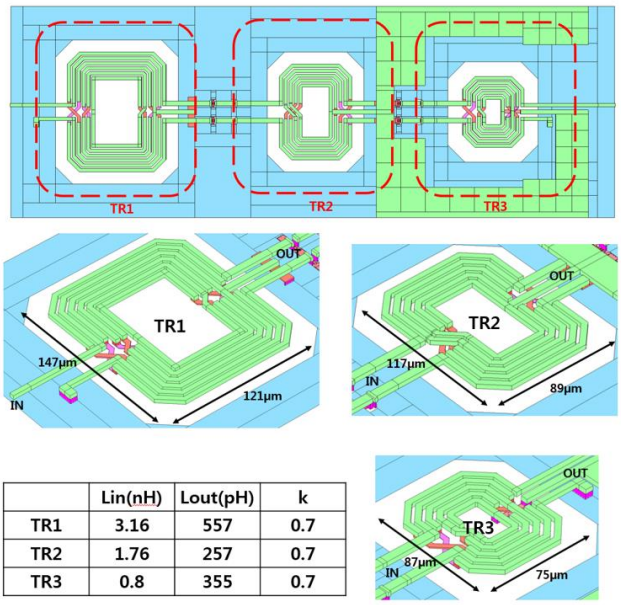


Fig.4. The model of Transformer's imbalance



	Lin(nH)	Lout(pH)	k
TR1	3.16	557	0.7
TR2	1.76	257	0.7
TR3	0.8	355	0.7

Fig. 5. EM simulation structure of the transformers

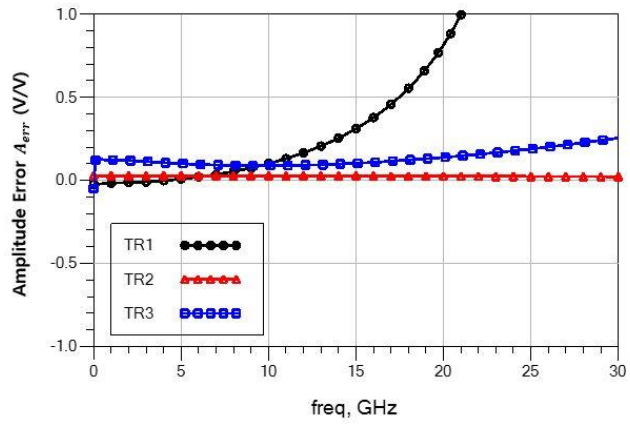
The harmonic power conversion efficiency according to the gate bias is simulated and shown in Fig. 2. Optimized gate bias has high 3rd harmonic power by Class-C bias and 2nd harmonic power suppressed by differential structure. The 2nd stage amplifier also uses transistors M5, M6, M7, M8 cascode configuration and is biased to Class-A with a gate bias of 0.52V to amplify the power at the output frequency to a sufficient level. The 2nd amp stage amplifies the power at the 3rd harmonic frequency and suppresses the fundamental and 2nd harmonic, and the S-parameter S21 simulation result is shown in Fig. 3. High fundamental suppression is achieved by increasing the power ratio of the 3rd harmonic to the fundamental power to the optimal gate bias condition in the Class C bias of the tripler stage and amplifying the 3rd harmonic and suppressing the fundamental at the 2nd amp stage.

B. Transformer

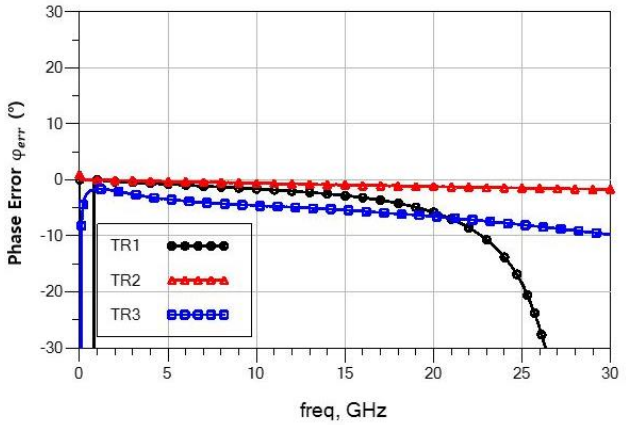
Transformers are used for input and output matching and are used to apply differential signals. To achieve high even-order harmonic suppression according to eq.(1)-(4), the transformer requires high differential symmetry. But it is difficult to implement in a perfectly symmetrical structure of the transformer. The impedance on two port of the input coil are different, as shown in the Fig.4. The one is 50 Ohm, the other is connected to the ground. Thus, the imbalance of symmetrical Transformer is inevitable, Especially at the input transformer(TR1) and output transformer(TR3). The differential symmetrical characteristics of the transformer can be expressed as the S-parameter ratio of the two output signals:

$$S(2,1)/S(3,1) = (1+A_{err})e^{(180^{\circ}+\varphi_{err})} \quad (5)$$

where A_{err}(V/V): amplitude error and φ_{err}(°): phase error



(a)



(b)

Fig. 6. Simulated (a)amplitude error, (b)phase error of differential signal

Transformers are designed to be as close as possible to the same amplitude and 180 degree phase difference through meticulous electromagnetic(EM) simulation to effectively cancel the even-order harmonics. Fig.5 shows the EM simulation structure of the circuit. TR1 is designed to provide the symmetry at the input frequency and inter-stage transformer(TR2) is designed to provide differential symmetry at the 2nd harmonic frequency so that 2nd harmonics can be removed. The TR3 is designed to provide output matching and to be symmetric about the 2nd harmonic frequency. The differential symmetry characteristics of the simulated transformers calculated by eq.(5) are shown in Fig. 6, and in Fig. 6(a), the two differential signals are designed to have only an amplitude error of 0.052 for TR1, 0.025 for TR2 and 0.107 for TR3 and a phase error of 1.308 degrees for TR1, 1.036 degrees for TR2 and 5.615 degrees for TR3 as shown in Fig.6.(b) at frequencies where symmetry is required. The TR2, TR3 transformer includes a center-tap for DC bias.

III. MEASUREMENT RESULTS

The frequency tripler circuit was designed and manufactured in 65-nm CMOS process. The micrograph of the chip is shown in Fig. 7 and the core size is 259x742 μm². The measurement was carried out with on-wafer ground-signal-ground probing, and the output was measured using a

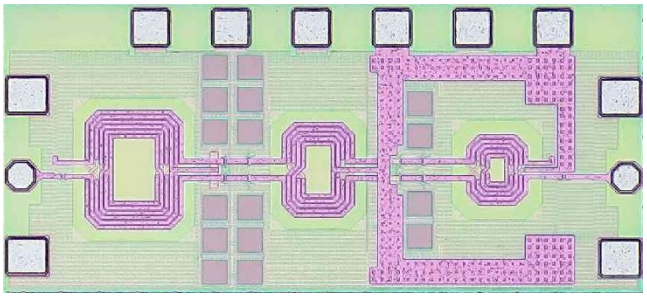
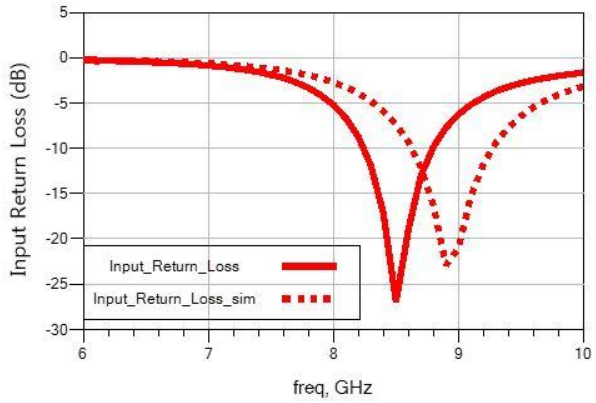
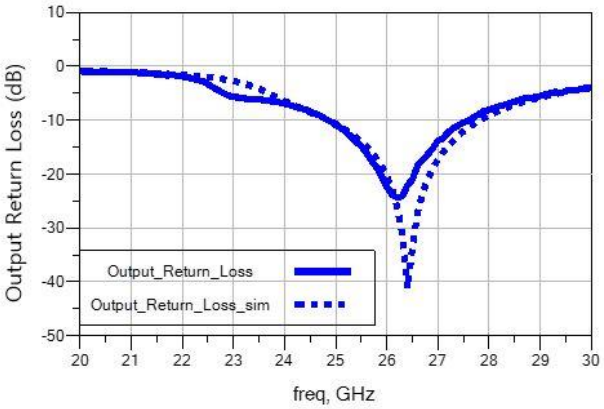


Fig. 7. Chip micrograph of the designed tripler



(a)



(b)

Fig. 8. (a) Input matching and (b) Output matching of designed tripler

spectrum analyzer in the input frequency range of 7.5-9GHz by receiving an input signal from a signal generator. The tripler consumes about 20mW power at a 1V supply voltage.

In order to check the small signal characteristics, the input/output matching characteristics were measured. The input matching of the fabricated chip is shown in Fig.8(a). It was measured to have an input return loss of -5dB at 8-9GHz. The output matching can be seen in Fig.8(b), and the output return loss is lower than -5dB in the output frequency band 22.5-27GHz. The input matching shifted the frequency to about 500MHz below the simulated, and the output matching showed similar characteristics to the simulation. The shifting of input matching seems to be due to the error of the EM simulation of the input matching network.

Conversion loss and 3rd Harmonic output power at 0.5dBm

TABLE I. Comparison of the tripler

Ref.	[3]	[4]	[5]	[6]	[7]	This Work
Process	45nm SOI CMOS	0.18μm CMOS	65nm CMOS	0.11μm CMOS	130nm SiGe	65nm CMOS
Type	x3	x3	x2	x3	x3	x3
Output Freq,(GHz).	27.1-32.4	18-24	22-25	17.7-29.7	24-48	22.5-27
3dB BW(%)	17.8	28.6	12.8	50.6	67	16.7
CL(dB)	22.8	5.7	-5	7.6	2.5	1.28
Fund. HRR(dBc)	13.6	22.44	>44	>6.4	>15	>32.2
2nd HRR(dBc)	20.1	16.1	-	>27	>15	>28.7
4th HRR(dBc)	-	20.18	-	>27	>15	>33.9
Pdc(mW)	25-35	7.5	31	7.2	6.8	20
Area(mm^2)	0.48	1.05	0.47	0.54	0.72	0.192(core)

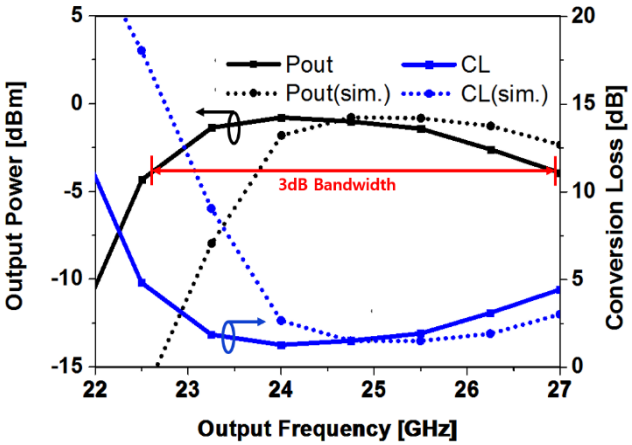


Fig. 9. Conversion loss and output power with a 0.5dBm input power

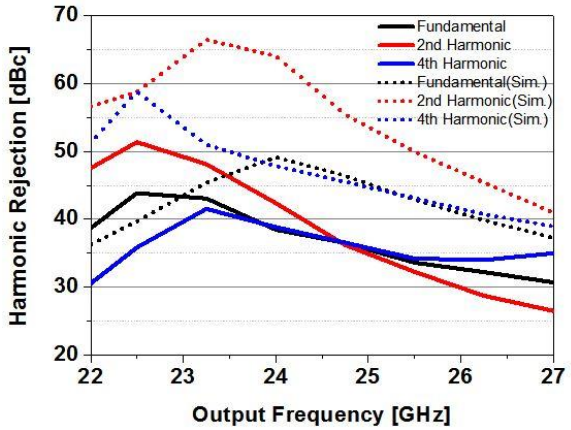


Fig. 10. Measured harmonic rejection with a 0.5dBm input power

Input power is shown in Fig. 9. The output power was measured by changing the input frequency from 7.5 to 9GHz. The maximum conversion loss is 1.28dB at the output frequency of 24GHz and the 3-dB bandwidth is about 4.5GHz, which has a fractional bandwidth of 16.7%. The output power has a ripple of 1.5dB within the bandwidth.

Fig. 10 shows the harmonic suppressions according to the frequency at 0.5dBm input power. The measured fundamental suppression, 2nd harmonic suppression, and 4th harmonic suppression are 30.7dBc, 26.5dBc, and 34.98dBc

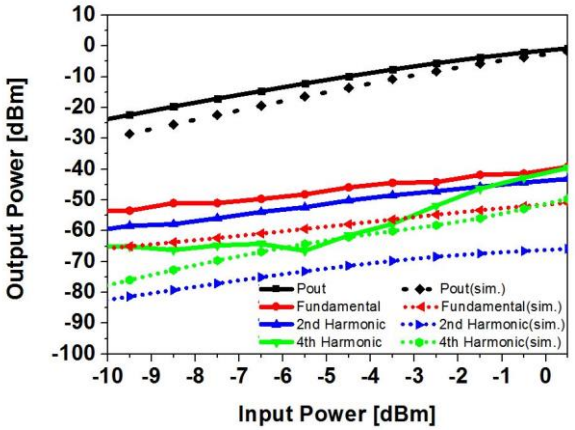


Fig. 11. Harmonic power at the output with a 24GHz output frequency

at 3dB bandwidth. It shows undesired harmonic suppression of more than 38.5dBc at operating output frequency 24GHz with maximum output power. In addition, Fig. 11 shows the result of measured the output power by fixing the input signal frequency to 8GHz and increasing the input signal from -20dBm to 0dBm. the measured maximum output power is -0.78dBm at an input power of 0.5dBm.

The measurement results are summarized in Table I, and a comparison with frequency triplers in a similar frequency band is shown.

IV. CONCLUSION

Using a 65nm CMOS process, a 22.5-27GHz band tripler is presented in this paper. The proposed tripler achieves high harmonic suppression more than 28.7dBc with an excellent output power flatness. Carefully designed differential tripler is utilized to improve the harmonic suppression.

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Jeong Taek Son received the BS degree from Chungnam National University (CNU), Daejeon, Republic of Korea, in 2021, and is currently working toward a MS in Microelectronics Engineering from CNU. His research interests include RF/mm-wave integrated circuit design for wireless communications.

Han Woong Choi received his MS from Chungnam National University (CNU), Daejeon, Republic of Korea, in 2017, and is currently working toward a Ph.D. in Microelectronics Engineering from CNU. His research interests include RF/mm-wave integrated circuits and systems for short-range radar and phased-array antenna applications.

Choul Young Kim received his MS and Ph.D. from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea, in 2004 and 2008, respectively. From March 2009 to February 2011, he was a postdoctoral research fellow at the Department of Electrical and Computer Engineering, University of California, San Diego, USA. Currently, he is a Professor of Electronics Engineering at Chungnam National University. His research interests include RF/mm-wave integrated circuits and systems for short-range radar and phased-array antenna applications, and analog front-end readout integrated circuits for LADAR applications.