Multi-Mode Radar RF Front-end Design

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***Abstract* - In this study, we convert multiple radar modes to time division and design multi-mode radar to detect long-range and multi-targets. In particular, CMOS multi-mode radar transceiver integrated circuits for mode switching are developed to configure the hardware. Design radars that support LFM, FMCW, and CW modes to detect long range, short range, and multiple targets. The 65nm CMOS process is used, and the metal is 9-metal(1P8M_5X1Z1U). The MOS transistor uses RF and analog devices, and the supply voltage is 1.2V. The operating frequency is 23.5-24.5 GHz and the area is 3.54x3.54mm. The design software is cadence (IC615 and IC617), and the EM design software will use sonnet.**

***Keywords*—Front-end, FMCW, LFM, Multi-mode radar, RF**

I. INTRODUCTION

Radar is an electronic device invented to detect and discriminate moving objects without distinguishing between weather conditions and day and night, and cope with situations. Radars are used in place of the human eye in many environments that cannot be easily solved by manpower, especially for security equipment for intrusion detection, automobiles, robots and military applications. Therefore, it must be designed and installed for various environments and purposes in order to maximize its performance.

As countries affected by recent drone attacks continue to emerge, demand for military or civilian anti-drone and surveillance radars is increasing. However, the current radar only detects the location (distance) and speed of the target, so it is not easy to distinguish whether the target is a monitored object (e.g. a drone) or not (e.g. a bird). The identification of the target in not easy, so it does not play a role as an anti-drone. Therefore, in this study, we design a multi-mode radar to simultaneously detect a long-range target and multiple targets through a plurality of radar modes. In particular, we develop a CMOS multi-mode radar transceiver integrated circuit for mode switching and configure hardware. The LFM (Linear Frequency Modulation) radar is suitable for long range detection, and when the target approaches and the target identification is urgent, the Frequency Modulated Continuous Waveform (FMCW) radar is suitable for short range target identification. In the case of multiple targets, Continuous Waveform (CW) and FMCW radars are used simultaneously.

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II. DESIGN METHODOLOGY

A. Continuous Waveform (CW) radar

Called CW radar or CW doppler radar, the doppler effect can be used to calculate the speed at which an object approaches through doppler frequency, as shown in Fig. 1.

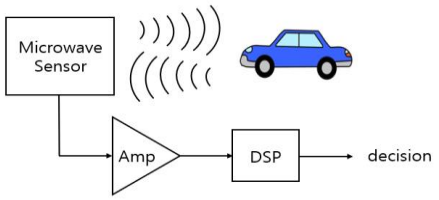


Fig. 1. Principle of CW radar

B. Frequency Modulated Continuous Waveform (FMCW) Radar Section title

The CW radar can only detect the speed of the target using the doppler frequency, so you must use the FMCW radar if you want to measure the distance between the target and the radar at the same time. Fig. 2 illustrates the principle of an FMCW radar. The FMCW radar linearly increases and decreases outgoing frequencies in a constant frequency range over time. Time and doppler frequency are calculated using the difference between the transmitted frequency and the received frequency (bit frequency), and the distance and the speed are calculated.

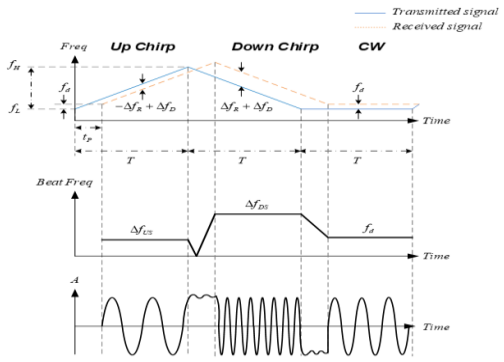


Fig. 2. Principle of FMCW radar

C. Linear Frequency Modulation (LFM) radar

Fig. 3 illustrates the principle of an LFM radar. The LFM radar is a radar for measuring the distance and speed to the

target by using a reflected wave that hits the target after sending out a pulse. It is mainly used to monitor targets that are very far away. While LFM radars are useful for long-range target detection, when overlapping transmission and reception signals occur, ambiguity occurs and short-range use is impossible.

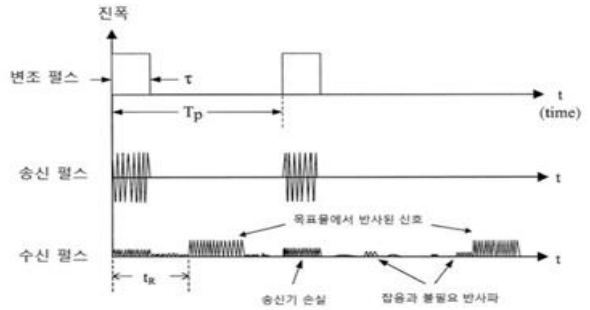


Fig.3. Principle of LFM radar

TABLE I. Comparison of characteristics of basic surveillance radar

Characteristics	CW	FMCW	LFM
Distance	Short distance	Short distance	Long distance
Distance / velocity	Velocity only	Distance / velocity	Distance / velocity
Architecture	Simple	Complication	Complication
Signal processing	Simple	Complication	Complication
Demand	Low	High	Low

III RF FRONT-END DESIGN

Fig. 4. is a block diagram of the transceiver structure of the proposed multi-mode radar. The transmitter uses a -20dBm baseband signal at 24 GHz through the RF mixer and uses DA (drive amplifier) and PA (power amplifier) to design the final output power of 15 dBm. The DA is designed with two paths, and the LFM mode is transmitted directly from the TX, and the LFM signal is generated and transmitted by the signal processor. In CW and FMCW mode, signals are generated from PLL and VCO in LO path. Mode is switched over DA and signal is transmitted over PA. The receiver receives the combined frequency of 24 GHz and the doppler frequency. The doppler frequency is about tens of hertz, so it is much smaller than 24 GHz. Therefore, the receiver of double conversion structure was used to use accurate doppler frequency. When the first 24GHz + F_d (doppler frequency) is received, it is converted to 1.25MHz + F_d through the down mixer, and another F_d frequency is obtained through the down mixer.

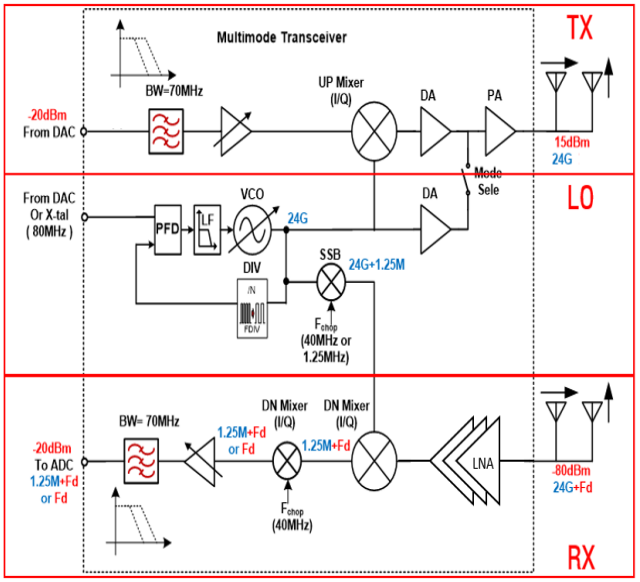
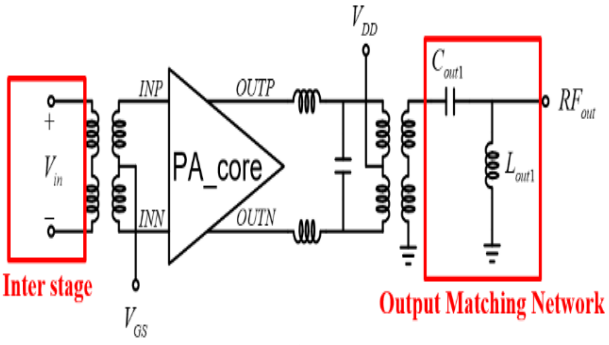


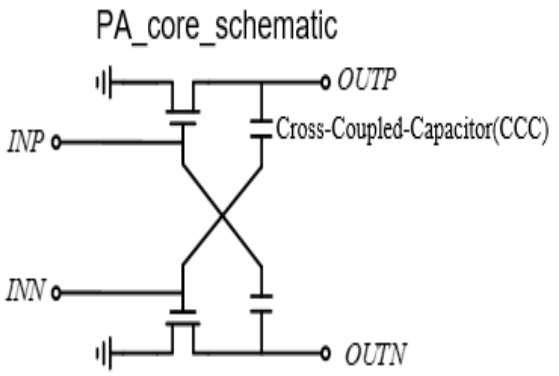
Fig. 4. Block Diagram of Multi-Mode Radar Transceiver Structure.

A. Power Amplifier (PA)

PA of TX was designed to increase the output power as high as possible. To secure sufficient headroom, a transformer was used on the output stage. The total current of PA stage was 100 mA and about 9dBm of the output power was obtained. Fig. 5 shows the circuit diagram and PA core of the PA, and Fig. 6 graphically shows the output power relative to the input power, resulting in OP1dB of approximately 9 dBm.



(a)



(b)

Fig. 5. (a) Schematic of PA, (b) Schematic of PA core

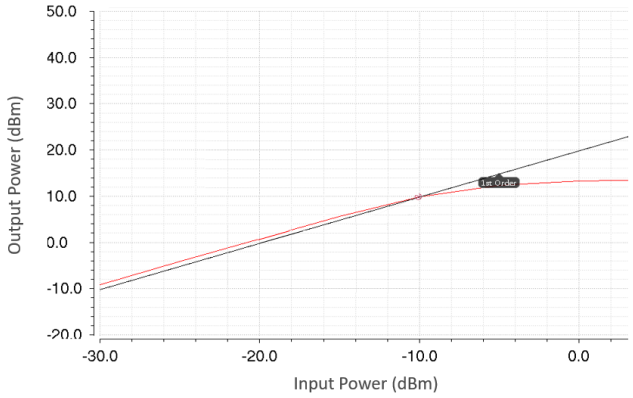


Fig 6. Simulation result of output power versus input power

B. Phase Locked Loop (PLL)

In LO path, frequency output waveforms in FMCW mode and CW mode are generated, and are the most important circuits in the transceiver. Fig.7 shows the full block diagram of the PLL, and Table II shows specification of the PLL. Multi-mode radar transmission and receiving integrated circuit is designed as a 1-poly 9-metal 65nm CMOS process. Due to the characteristic of the process, calibration through AFC (automatic frequency calibration) is required by inductor and variation of capacitance.

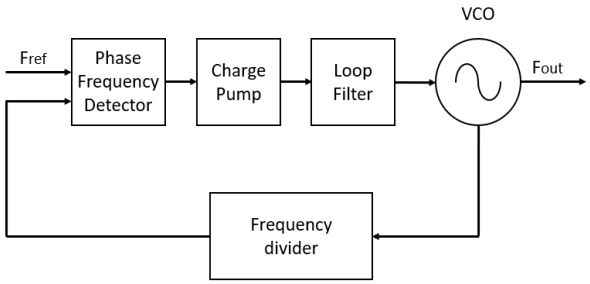


Fig. 7. Block diagram of PLL

TABLE II. Performance of PLL

Reference Clock	80 MHz
Loop Band Width	430 KHz (3rd order)
Sigma Delta Modulator	20bit 1-1-1 MASH type
Fout	24 GHz
Freq	610.35 Hz

Fig.8 shows a circuit diagram of the PFD (phase frequency detector) that makes up the PLL, receives a reference clock of 80 MHz, and delay is 7 to 10 percent of the reference frequency cycle. It is also designed to control delay.

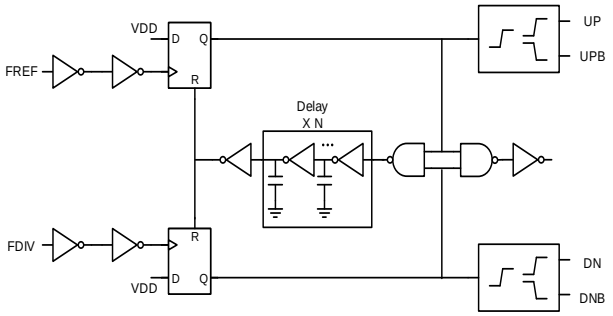


Fig. 8. Schematic of PFD

Fig.9 shows the circuit diagram of the divider that makes up the PLL. Because VCO frequency is too high to use frequency divider, divider2 was designed using Current Mode Latch (CML). The self-oscillation frequency is half of the input frequency. By applying three stages, 24GHz is divided into 3GHz.

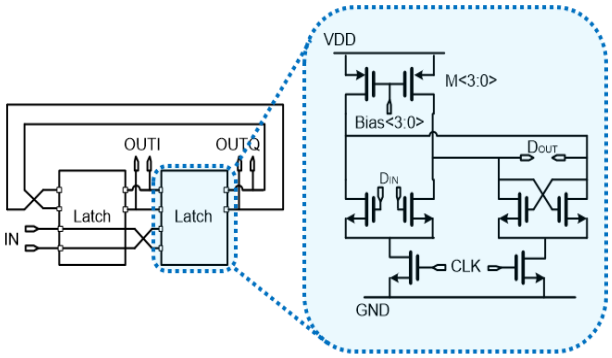


Fig. 9. Schematic of the divider

Fig.10 is a circuit of the loop filter in the PLL. 3 order loop filter is designed. The PLL is discrete system, but it is simulated with a linear model. Since stability and phase noise are trade-off relations, adjustable pole capacitance, zero resistance, and zero capacitance are applied to reduce errors in the measurement.

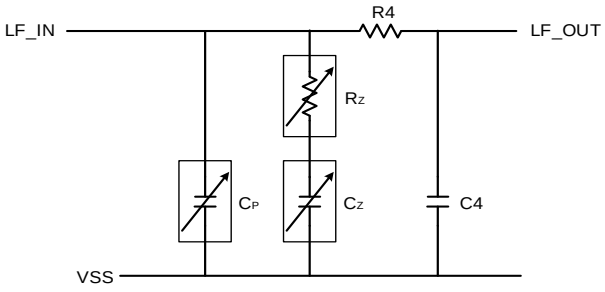


Fig. 10. Schematic of the loop filter

Fig.11 is the circuit of VCO (voltage control oscillator). The frequency range is from 23.5 GHz to 24.5 GHz. The capacitor is designed to be controlled by a combination of 3 bits. In order to improve phase noise, Switchable Triode Transistor Array (STTA) structure is used.

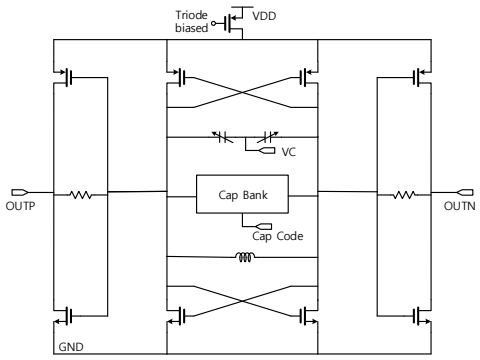


Fig. 11. Schematic of VCO

Fig.12 is a simulation result showing the output of VCO through discrete fourier transform and output frequency is 24GHz.

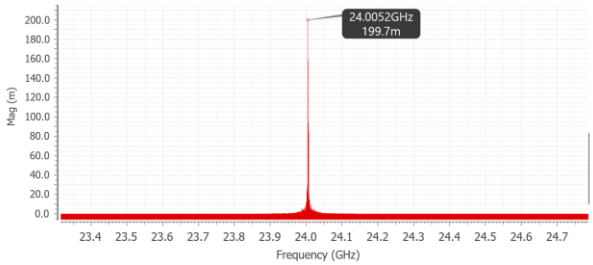


Fig 12. Simulation result of the VCO output

Fig.13 shows the simulation result of switching the VCO band by increasing the loop bandwidth by VCO Pre-Tuning and charge pump current boost. The frequency difference is 3.5 MHz and the locking time is approximately 0.588 us.

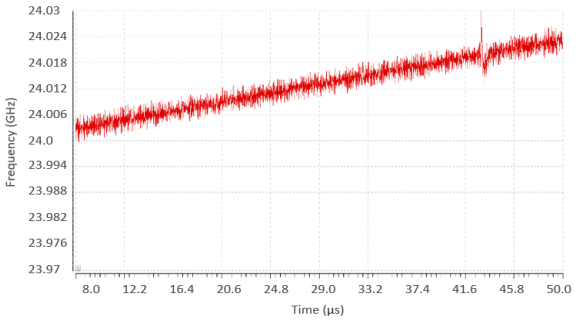


Fig. 13. Simulation result of band switching buy using pre-tuning & charge pump current boosting

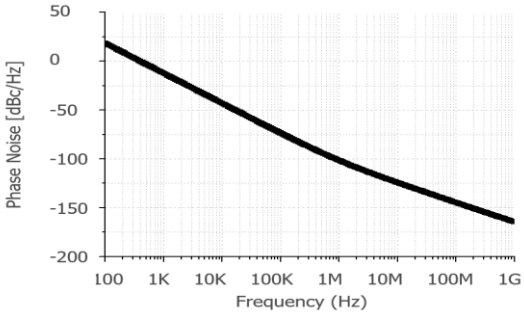


Fig. 14. Simulation result of phase noise of VCO

Fig.14 shows the simulation result of phase noise of VCO. It has -73.53 dBc/Hz at 100 kHz and -101.6 dBc/Hz at 1 MHz.

C. Receiver

RX is designed in an ICPM (image rejection chopping mode) structure to reduce the noise. Fig.15 shows the block diagram of receiver. The SNR (signal to noise ratio) is improved because this structure operates in the intermediate frequency band with low flicker noise. The ICPM structure can selectively receive the target signal by using image rejection. Also, it was designed to control gain and BW.

It allows DC offset cancellation and blocker rejection by feedback of down-converted frequency corresponding DC components. Therefore, it is designed to make it possible to determine if the measurement target is getting closer and further away.

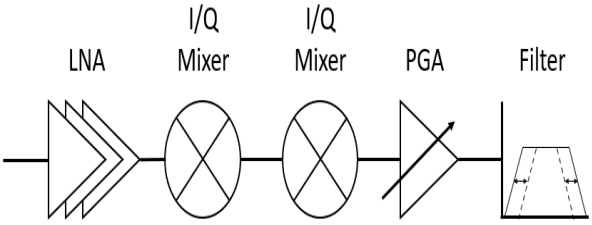


Fig. 15. Block diagram of receiver.

The LNA is designed to be 3-stage and Fig.16 shows the S-parameter simulation results. LNA performs 39.69 dB of S21, -42.17 dB of S11, and 5.34 dB of noise figure at 24.2GHz.

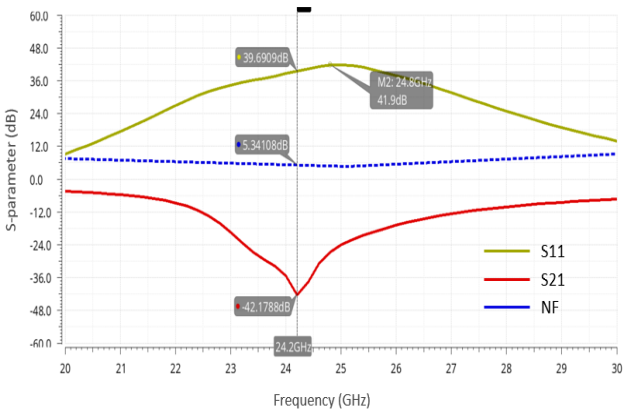


Fig. 16. Simulation result of LNA.

It is implemented as a TIA (transimpedance amplifier) in passive mixers and minimizes performance degradation with LC tuned LO buffer by increasing the gate bias. It is possible to change the transition gain by changing the resistance value of the TIA. Also, HPF using DCOC is designed to maintain constant input signal sensitivity according to distance. Fig.17 shows the simulation result of the base band of receiver.

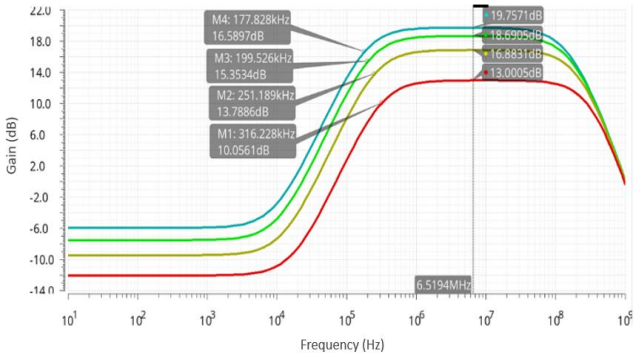


Fig. 17. Simulation result of base band of receiver.

IV. RESULTS AND DISCUSSION

In this paper, a new multi-mode radar transceiver is designed to detect targets at a distance and multiple targets using LFM, CW, and FMCW modes. The process is a 1-poly 9-metal 65nm CMOS and the design has been completed. Fig.18 shows layout of transceiver.

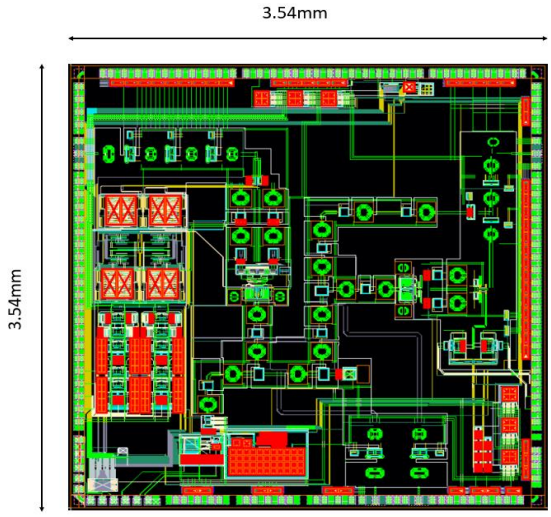


Fig. 18. Layout of transceiver.

TABLE II. Summary table of simulation results

Spec	Unit	TX	RX
Process (nm)	nm	65 CMOS	65 CMOS
Frequency (GHz)	GHz	24	24
NF@1MHz	dB	-	5
Gain	dB	23	66
IP1dB	dBm	-13.5	-55
OP1dB	dBm	6.5	10
DC Rejection	dB	-	35
LO Leakage Rejection	dB	37	-
BW	GHz	0.07	2
Supply Voltage	V	1.2	1.2
Current	mA	86	99

The transceiver for the CMOS multi-mode radar system was fabricated in a TSMC CMOS 65 nm process, and the total area is 3.54mm × 3.54mm. A 3.3 V supply voltage was used and the measurement was carried out after wire bonding the IC to the PCB.

V. CONCLUSION

It designed IC chips for multi-mode radar transceiver supporting LFM, FMCW, and CW modes, and has an operating frequency of 23.5 to 24.5 GHz. The transmitter, receiver, VCO and PLL are designed for multi-mode radar systems. Currently, PCBs using ROGERS substrates are being manufactured considering RF frequency characteristics.

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