Multi-level Waveform Generator with Delay Control for Low Distorted Class D Amplifiers

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***Abstract* – A multi-level waveform generator with delay control is proposed for improving total-harmonic distortion of class D amplifiers. The voltage-mode class D amplifier is a circuit that amplifies the output voltage at the load to be twice almost the power supply voltage by using an input driving signal. The conventional 3-level class D amplifier generates a lot of harmonics due to the switching operation, and the harmonics can only be removed by the frequency response characteristics of the load. A configuration of the class D amplifier that sets an intermediate voltage level to reduce the harmonics has been presented, but it is required to generate the driving waveform for this. The proposed waveform generator makes driving signals that can change the voltage applied to the amplifier load from three to five levels. The generated step time can be optimally set depending on the driving frequency by controlling the RC delay circuits in the edge detector of the proposed generator. The generator IC fabricated in the area of 840 µm × 640 µm using the TSMC 0.25 µm CMOS process shows 5-level driving waveforms converted the input pulse-width modulation signal of 200 kHz. The measurement results show that the intermediate step time can be adjusted to 0.48 µs by controlling the delay circuit of the proposed waveform generator.**

***Keywords*—Class D amplifier, Delay control, Low harmonic distortion, Multi-level waveform**

I. INTRODUCTION

Class D amplifiers, called H-bridge drivers, can drive high power signals to the load with high efficiency with control of switching transistors by input pulse width modulation (PWM) signals [1−3]. Because highly efficient and highly powered amplification can be achieved by using small-sized switching devices compared to the other amplifiers, class D amplifiers are widely used in small consumer electronic devices such as earphones, speakers, hearing aids, and wireless power transmitters [4−6].

The output signal to the load of the class D amplifier is conventionally implemented with 3-level voltage waveforms, which are high, low, and zero states to prevent the destruction of the switching transistors owing to simultaneously turning on of all switches on the supply-to-ground path [7−8]. The voltage waveform at the load is ideally a square wave owing to the switching operation driven by the PWM signal. The square wave shows that it contains a lot of harmonic signals that reduce signal quality and output efficiency, and the harmonics are generally reduced by the impedance characteristics of the load having band-pass or low-pass frequency responses. However, when the frequency response of the load has low frequency selectivity or low quality-factor, large harmonics cannot be sufficiently removed at the output. Total harmonic distortion (THD), which means the ratio of the sum of the overall powers of all harmonic signals to the power of the fundamental frequency, is a very important performance factor in radio communication systems, power systems, and audio systems [9]. The method of configuring additional voltage levels in the conventional 3-level class D amplifier has been studied to reduce THD at the output [10−13]. Previous studies reduce the generation of harmonics at the output by shaping the driving waveform using the intermediate voltage steps which are provided by additional switches in addition to the resonant load. However, the circuit configuration that generates the driving waveforms of the switches by using the PWM signal is complicated to design and implement, and series-configured switches which can increase the loss owing to the on-resistance are added to the current path [10−12]. A simple configuration using the parallel switches was proposed to the low-distorted class D amplifier, but the waveform generator to make specific waveforms for driving the switches were not presented [13].

In this paper, a waveform generator for a low-distorted class D amplifier is proposed to implement 5-level voltage output at the load. The proposed waveform generator is simply composed of edge detectors and combination logic circuits to generate driving waveforms from the input PWM signal. The time duration of the intermediate voltage step should be adjustable because the optimum time depends on the frequency of the input PWM signal. The time duration of the intermediate voltage step can be adjusted by controlling a 4-bit delay circuit implemented in the edge detector of the proposed generator. In Section II, the 5-level class D amplifier to be driven by the proposed waveform generator is presented in comparison with a conventional 3-level class D amplifier. Section III shows the circuit configuration and operation, and simulation results of the proposed waveform generator. Section IV provides measurement results and

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discussions of the generator implemented by TSMC 0.25 um CMOS process. Some concluding remarks are presented in Section V.

II. CONFIGURATION OF CLASS D AMPLIFIERS

The class D amplifier of the conventional H-bridge structure consists of two switch pairs which are received input signal A and B of the PWM signal generator as shown in Fig. 1(a). In the H-bridge operation, the input signal overlaps only the low state to prevent the destruction of the switching transistors owing to simultaneously turning on of all switches on the supply-to-ground path. Fig. 1(b) shows the timing chart of the three-phase operation which has the same pulse width by the input signal A and B. The output voltage of the load which has the three voltage levels can be obtained by turning two pairs of switches on and off alternately, which is useful to reduce THD at the output. However, the same pulse width of each level causes the mismatch of the desired waveform which has a similar sinusoidal signal with a low THD performance. In addition, the THD performance deteriorates further when the supply voltage is high.

Fig. 2(a) shows a proposed 5-level driver which is composed of six switches to advance THD performance maintaining stability. Each switch is controlled by the independent input signal of the proposed signal generator, two switches connected in parallel controlled by signals C and D are used to obtain the intermediate voltage level and control the pulse width of each level. In general, the voltage V_X is half of the supply voltage, when the input signal only A2 and C is on, the X path is generated where the output voltage of the load is 0.5VDD. Fig. 2(b) shows the timing chart of the five-phase operation in which each pulse width can be adjusted using the proposed signal generator. When the signal A1 and A2 are at high, the Y path is generated to obtain the voltage VDD until the signal C is high.

The output of the proposed 5-level driver has more output voltage resolution than the conventional 3-level class D amplifier. Because each voltage level of the 5-level driver is low compared to the 3-level driver in the same supply voltage, a 5-level driver with a low slew rate performance is suitable for the high-frequency condition. In addition, the THD performance is improved because the shape of the output voltage can be adjusted using an intermediate voltage level. Fig. 3 shows the simulated output spectrum of the 5-level driver compared with those of the 3-level driver at 100 Hz PWM input, the harmonic characteristics of the 5-level driver is improved by about 3 dB compared to the 3-level driver. The voltage of the 5-level and adjusting the pulse width of each level can be implemented using the proposed signal generator without a complicated structure of the driver. Table I summarizes the power ratio between the fundamental and total harmonic signals in the 3-level and 5-level drivers calculated from the simulation results in Fig. 3. The performance comparison in Table I shows that the harmonic distortion can be improved by the implementation of the 5-level driver.

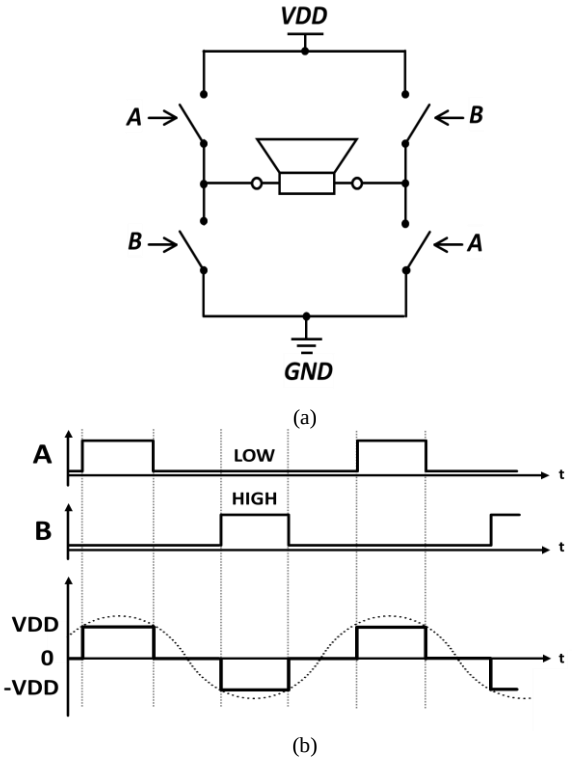


Fig. 1. Configuration of the 3-level class D amplifier; (a) Schematic of the conventional H-bridge structure (b) The timing chart of the output of the 3-level driver.

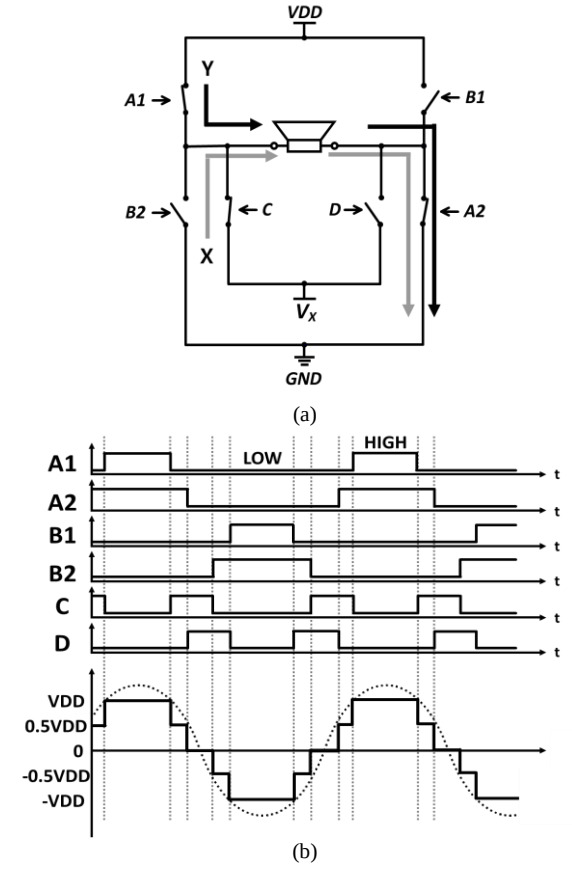


Fig. 2. Configuration of the 5-level class D amplifier; (a) Schematic of the proposed H-bridge structure (b) The timing chart of the output of the 5-level driver.

III. PROPOSED WAVEFORM GENERATOR FOR 5-LEVEL CLASS D AMPLIFIERS

The proposed multi-level waveform generator can drive multi-level outputs by generating a specific waveform that drives the switch of a class D amplifier, unlike other multi-level drive schemes that are complex to implement. The extended multi-level, 5-level is driven by adding the +Vx and −Vx node voltage levels between the edge of change in the conventional 3-level class D amplifier output steps. As shown Fig. 4, the proposed waveform generator consisting of edge detectors that detects the point of change in the signal and a combination logic circuit that switches the control signal of a class D amplifier by mixing the detector outputs. The proposed waveform generator operating with the PWM signal has ideal square waveform outputs as shown in Fig. 2(b). The edge detector in Fig. 5(a) can detect both the rising time and the falling time of the pulse waveform by using the logic device characteristics between the delayed signal by the internal delay circuit and the input signal. The total time constant (τ_{to}) in Fig. 5(b) is determined by the internal delay circuit consisting of a 4-stage RC circuit. The individual stage has the same time constant because the resistor and the capacitor are the same sizes. Extra delay is applied by the two inverters. The output signal (V_{Delay}) of the delay cell is utilized for comparison with the input signal (V_{IN}) using the logic gate. As shown in Fig. 5(b) When V_{IN} and V_{Delay} are in a high state at the same time, the AND gate detects the rising edge. Opposed to the rising edge detecting, the NOR gate outputs the falling time. The designed edge detectors can control total time constant delay with 16 resolutions by the 4-bit code of the internal delay circuit. The 0000-control code has a minimum delay and a maximum delay at 1111. The delay time, which determines the output pulse width by control code enables multi-level driving at different frequencies.

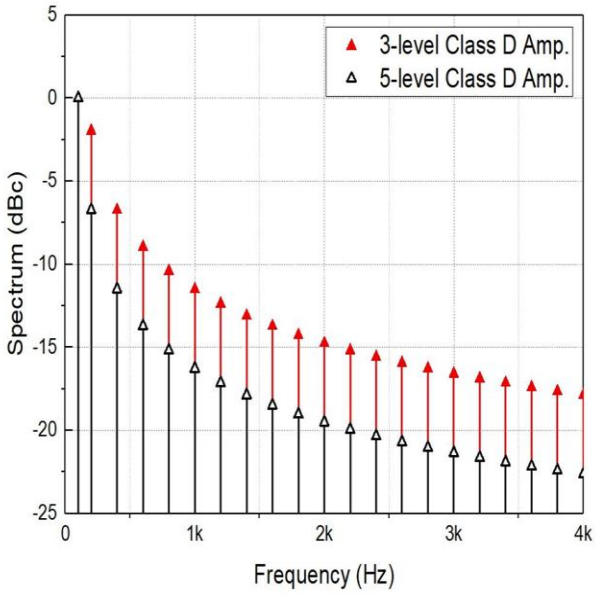


Fig. 3. The frequency spectrum of the 3-level and the 5-level class-D driver in response to a 100 Hz input.

TABLE I. Power ratio between the fundamental signals and total harmonics calculated from the simulation results in Fig. 3.

	3-Level Driver	5-Level Driver
Fundamental Signal [dBm]	30	31.761
Total Harmonics [dBm]	32.425	29.415
Ratio [%]	174.78	58.26

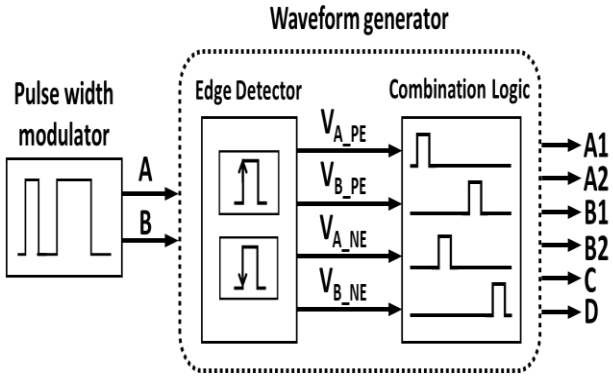
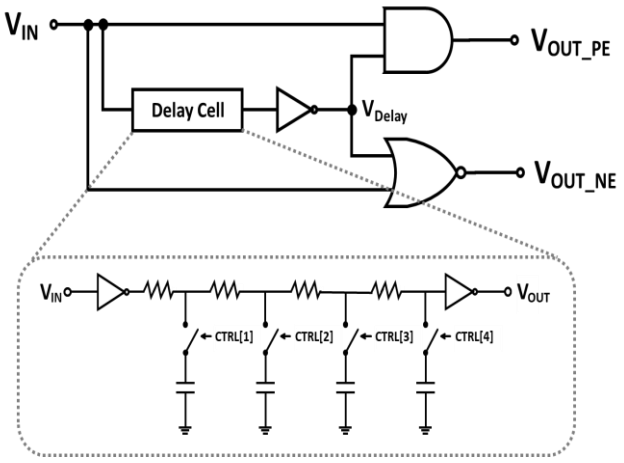
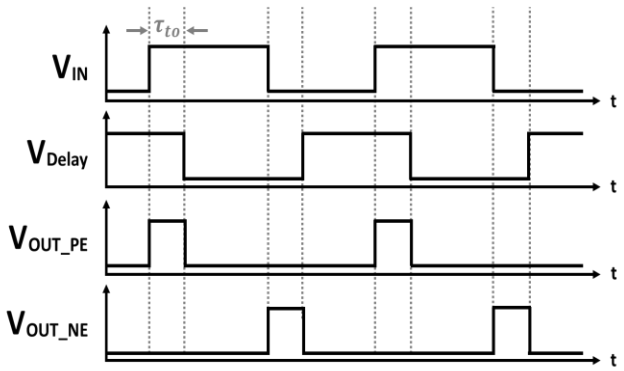


Fig. 4. Proposed waveform generator block diagram



(a)



(b)

Fig. 5. The Edge detector which detecting rising and falling edge from the input PWM signal; (a) circuits with integrated 4-bits RC delay cell (b) timing diagram.

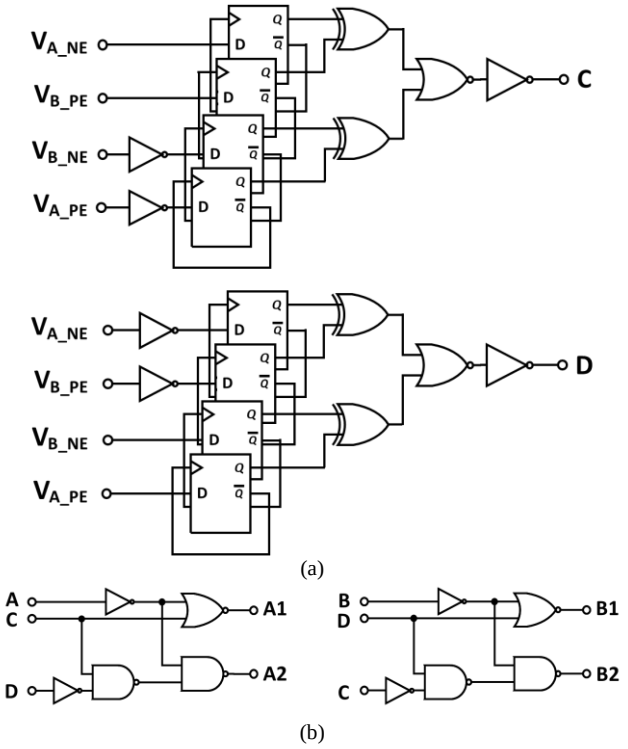


Fig. 6. Combination logic circuits; (a) with D flip-flops to generate C, D signals (b) modulates the pulse width to generate specific switching operation signals.

The combinational logic circuits that output the waveforms for individually operating the switches of the class D amplifier consists of a total of two steps. First, the logic circuits with D flip-flops in Fig. 6(a) combines the detector output signals with the rising and falling data of the PWM signal to generate the C and D pulse signals. The output waveform C is the signal from the falling edge of waveform generator input signal A to the rising edge of B. Unlike C, D is from the rise of A to the fall of B. The generated C and D are important signals to prevent overlap between switching signals so that no supply-to-ground current path occurs. Fig. 6(b) is logic circuits that modulates the pulse width by mixing C and D generated in the first step with the PWM output signals A, B. In this step, the two characteristics of the rising edge and falling edge of the input signal of the proposed waveform generator are separated and recombined into a waveform with one edge characteristic. For A1 and B1, the falling edge timing is the same as the original signals A and B, and the rising timing of A2 and B2 is the same as the original signal.

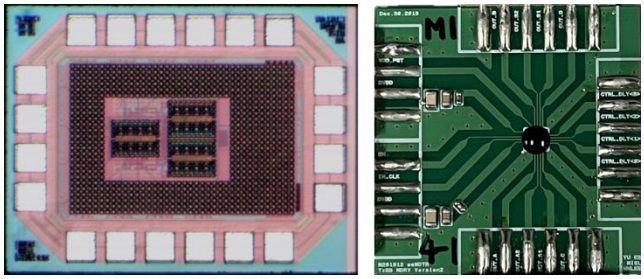


Fig. 7. (a) The die photograph (b) The printed circuit board (PCB) of the proposed waveform generator

IV. RESULTS AND DISCUSSIONS

The proposed waveform generator with size 840 μm × 640 μm is fabricated using TSMC 0.25 μm mixed-signal CMOS technology is shown in Fig. 7(a). The printed circuit board (PCB) for measuring the fabricated multi-level driver IC is shown in Fig. 7(b). The PCB with 1T thickness FR4 board is 3 cm × 2.9 cm.

The Digilent Analog Discovery 2 model which is manufactured by Analog Device is used to obtain the measurement results. The model is powered by a high-speed USB port and used by WaveForms software. The 5V power and enable signal are applied by using an external power supply and the clock signal with an amplitude of 5 V from the function generator is applied to the PCB. In the model which is consisted 16 digital input/output pins, the delay cell of the edge detector is controlled to 4 bits through the 4 digital input signal pins and the 8 outputs of the waveform generator are confirmed in real-time on the 8 digital output signal pins.

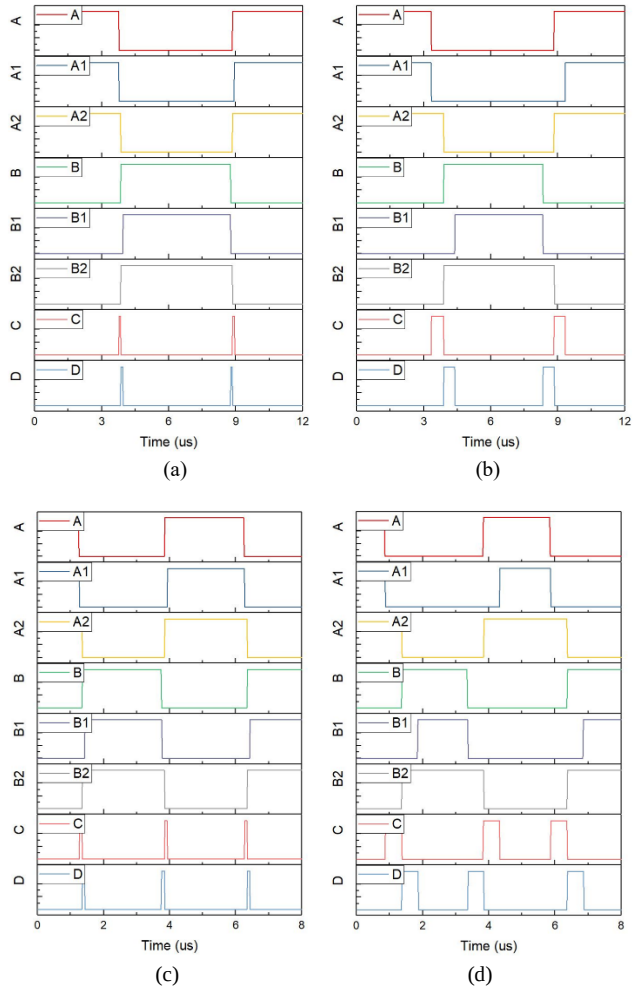


Fig. 8. The output signals of the proposed waveform generator on (a) 0000 (b) 1111 code at 100 kHz and on (c) 0000 (d) 1111 code at 200 kHz

Fig. 8 shows the measurement result of the proposed switch driving waveforms IC for the PWM signal generated according to the clock signal. The output signals with 0000 bit and 1111 bit at the clock signal of 100 kHz are presented

in Fig. 8(a), (b). The output signals as shown in Fig. 8(c), (d) include the measurement results on the maximum delay and the minimum delay at 200 kHz clock frequency. These results indicate that the delay time is up to 0.48 μs according to the control voltage. As a result of the measurement, it was confirmed that the proposed generator can be operated in a frequency range of 1 kHz to 230 kHz depending on the clock frequency and multi-level driving at different frequencies can be implemented by delay control code.

By adjusting the delay time until the output level state changes, the total harmonic distortion can be reduced, and the requirements of the output filter at the final output stage can be decreased. Also, the waveforms with low distortion characteristics for driving a class D amplifier can be obtained using the proposed switch driving waveform.

IV. CONCLUSION

A waveform generator for class D amplifiers is proposed to reduce the harmonic distortion at the output. The proposed generator consists of edge detectors and switching signal generation circuits implemented with D flip-flops and logic gates. A 4-bit controlled RC delay circuit in the edge detector adjusts the time duration in which the positive and negative edges are detected as a logic high. The time duration is determined to generate the intermediate voltage step in the 5-level class D amplifier depending on the frequency of the input PWM signal. All the waveforms to drive conventional 3-level and 5-level class D amplifiers can be simply obtained by the proposed generator. The proposed generator is fabricated in an area of 840 μm × 640 μm including signal pads by using TSMC 250nm mixed-signal CMOS process. The measurement results of the proposed generator show switch driving waveforms generated from the input PWM signal of 200 kHz for 3-level and 5-level class D amplifiers. It is demonstrated that the time duration at which the intermediate voltage step presents can be varied 0.48 μs by control the 4-bit codes.

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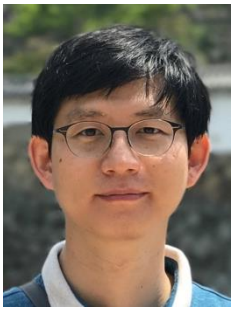

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