# Design of a 12 to 14.5 GHz Digitally-Controlled Oscillator for an Ultra-Low-Jitter PLL

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***Abstract* – A DCO was designed for an ultra-low-jitter digital sub-sampling PLL. To suppress the enormous amount of quantization noise, a very fine frequency resolution is critical. Also, the phase noise of an *LC* VCO itself is crucial for ultra-low-jitter applications. For high-performance *LC* VCO design, a basic insight into the oscillator is needed. The proposed DCO consists of a string-type RDAC, MASH 1-1 DSM, and CMOS-type cross-coupled *LC* VCO. The frequency resolution is significantly increased by using the DSM. The proportional path has a 17-bit resolution, while the integral path has an 18-bit resolution. The DSM operates at 400 MHz, and its quantization noise is canceled by the 2nd-order low-pass filter at the output of the DAC. By adopting 2nd-order noise shaping, the quantization noise at the PLL output is negligible. The DAC was designed with a string resistor topology for its design simplicity and relieved target specifications. The DCO has a 12 to 14.5 GHz frequency tuning range. The phase noise at a 1 MHz offset frequency is –109 dBc/Hz at a 14-GHz output. The average power consumption is 5.5 mW. The calculated FOM at a 1-MHz offset frequency is –184.5 dB.**

***Keywords*— Delta-Sigma Modulator (DSM), Digital-to-Analog Converters (DAC), Digitally-Controlled Oscillator (DCO), LC-VCO, Phase-Locked Loop, Phase noise, Sub-sampling**

## I. INTRODUCTION

As the communication industry has developed rapidly over the last few decades, research on communication circuits has received significant attention. From the perspective of commercialization, the most critical issue is how to achieve small-area and low-power designs while attaining the required performance. Recently, fabrication processes have been developed that are more suitable for digital designs with small-area and low-power to meet market requirements. Digital-based designs also have the advantage of their reconfigurability and ease of redesign according to process scales.

All-digital phase-locked-loops (ADPLL) have been intensively explored because of the above features. However, the quantization noise due to the limited frequency resolution of frequency discretization in digitally-controlled oscillators (DCO) can limit the performance of ADPLLs in terms of out-band phase noise [1]. To achieve a very fine frequency resolution, such that the quantization noise is lower than the phase noise of the oscillator, the size of the minimum adjustable switched capacitor must be smaller than several atto-Farads, which is limited by the process technology [1]. Recently, some research has attempted to minimize the effective adjustable switched capacitor by applying capacitive divider networks [2] or a C-2C switched-capacitor ladder [3]. However, both solutions are not robust to process variation because of their mismatches and parasitic. Another possible solution is to exploit the characteristics of delta-sigma modulators (DSMs), which are relatively insensitive to process variation. For an ultra-low-jitter digital PLL, quantization noise minimization is a critical issue. Therefore, designing a high-resolution DCO is very important. To raise the resolution of DCOs, several methods have been proposed [1]–[3].

Digitally-controlled oscillators (DCOs) or voltage-controlled oscillators (VCOs) are the most important components in PLLs that determine the overall performance of a PLL. Therefore, it is very important to design an appropriate oscillator for design purposes. *LC* oscillators usually occupy a huge silicon area; however, because of their superior figure-of-merit (FOM) due to their intrinsic frequency selectivity, they are widely adopted in high-performance RF applications. *LC* oscillators can be classified into Class-B, C, D, F, and so forth based on their conduction angle or harmonic characteristics. Efforts to improve phase noise and power efficiency have led to the introduction of new structures [4], [5]. Among them, Class-B architecture is the most commonly adopted because of its design simplicity and reliability.

In this paper, for design simplicity and robustness, a delta-sigma DAC-based DCO is presented.

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Manuscript Received Nov. 12, 2020, Revised Dec. 7, 2020, Accepted Dec. 8, 2020

## II. PROPOSED DIGITALLY-CONTROLLED OSCILLATOR FOR ULTRA-LOW-JITTER PLL

### *A. Design of Delta-Sigma DAC*

To sufficiently suppress quantization noise, a high-resolution delta-sigma DAC is required. The resolution of the DSM can be increased at the expense of power consumption, and the resolution of DAC can be increased at the expense of linearity. The resolution is differently set to the proportional path and the integral path of the digital PLL. In both paths, the resolution of the DSM is 12-bit. The proportional path has a 5-bit RDAC, and the integral path has a 6-bit RDAC. Because of noise shaping of the 2nd-order DSMs, a 2nd-order low pass filter is necessary [6]. The pole frequency of the proportional path is 100 MHz, and that of the integral path is 500 kHz. At the optimal pole frequencies, the quantization noise is negligible at the PLL output, and the filter area is minimal. The pole frequencies are also related to the operation frequency of the DSM, which is 400 MHz.

For the noise shaping, a 12-bit multi-stage noise-shaping (MASH) 1-1 DSM is used. Figure 1 shows the block model of the MASH 1-1 DSM. By cascading, second-order noise shaping is realized. For the RDACs, a simple string topology was used for a simple design. The RDAC linearity is not a critical issue in this application, so the linearity specification is somewhat relieved. Because the order of the DSM is two, we need 4 inputs (+1, 0, -1, -2) at each bit to make a fractional value. Therefore, for an n-bit RDAC, a total of $2^n$ + 4 resistors are needed for a second-order DSM. Figure 2 shows the schematics of the delta-sigma DAC and output low-pass filter with a digital loop filter (DLF). The resistance of the unit resistor of the DAC is 180 Ohm. The nominal high voltage of the DAC is 1.2 V so that the static power of the DAC is under 100 μW. Figure 3 shows schematics of the delta-sigma DAC, low-pass filters, and MUX with a digital loop filter (DLF). Unlike the design of the integral path, in the proportional path, the DAC is divided into the half, upper, and lower part. The upper part and lower part receive input separately, and the inputs are complementary. Therefore, two 2nd-order low-pass filters are needed. Here, $I_X$ denotes the decision signal from the bang-bang phase detector. It determines which voltage will be used for the control voltage, $V_{TUNE}$. The size of the resistors in the DAC is 145 Ohm. Likewise, the nominal maximum voltage of the DAC is 1.2 V. Therefore, the static power is 280 μW.

### *B. Design of LC* VCO

The design of high-performance *LC* VCOs is crucial because the performance of the oscillator determines the overall performance of a PLL. The following requirements must be met to achieve an ultra-low jitter digital PLL:

| | |
|---|---|
| Frequency tuning range | 12–14.5GHz |
| KVCO | 50 MHz/V for main loop, 500 MHz/V for axillary loop |
| Power | < 5 mW |
| FOM | -184 dB @ 1-MHz frequency offset |

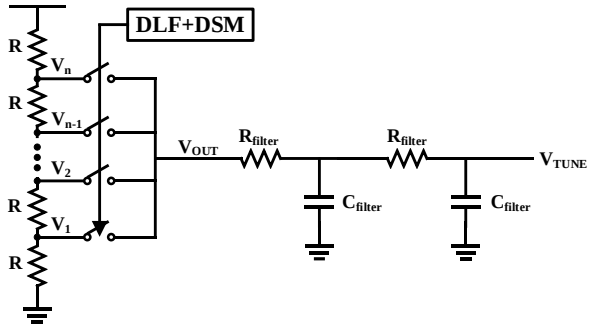


Fig. 2. Schematics of delta-sigma RDAC with 2nd order low pass filter and DLF used in integral path.

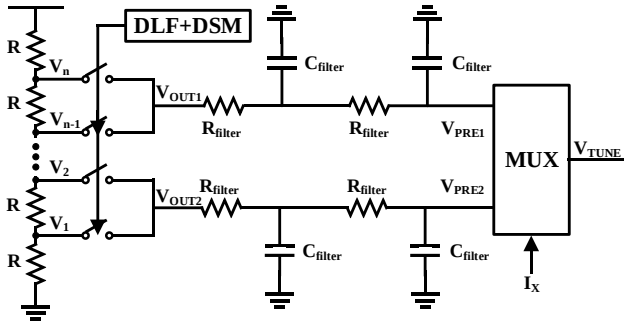


Fig. 3. Schematics of delta-sigma RDAC with 2nd order low pass filters, output MUX and DLF used in proportional path.

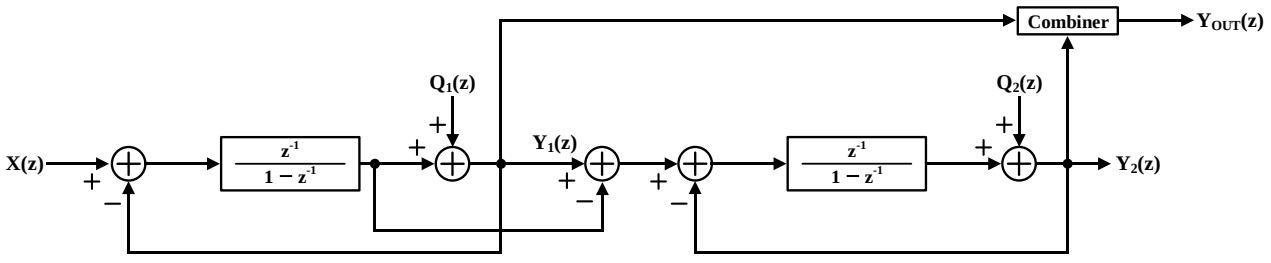


Fig. 1. Linear block model of MASH 1-1 DSM

Because the target frequency is high, the $g_m$ cell of the VCO should be a thin transistor to increase $g_m$ with the given parasitic capacitance. Also, a CMOS-type topology is chosen because, in an NMOS-type *LC* VCO with a thin

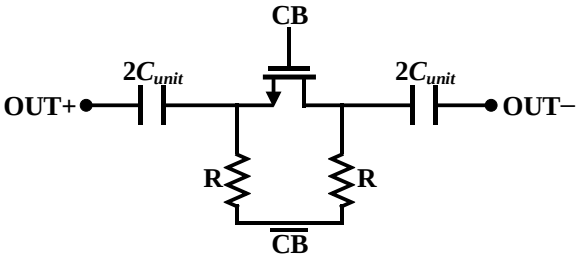


Fig. 4. Schematics of CBANK unit

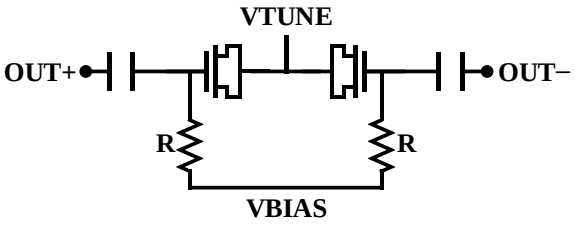


Fig. 5. Schematics of varactors in *LC* VCO

transistor, the gate oxide easily breaks. For superior phase-noise performance, an HVT device is used for the $g_m$ cell to prevent the transistors operating in the deep triode region.

The first step of design is the determination of the size of the inductor. The value of inductance is related to the oscillation frequency, frequency tuning range, phase-noise performance, and power consumption. Therefore, selecting the optimal inductance is a key step in the design of the VCO. In this design, 200 pH of an inductor is used, and its shape is calculated to have a maximum Q-factor. The calculated Q-factor is 30 at 14 GHz.

The next step is designing a capacitor bank (CBANK) for coarse frequency tuning. The total number of bits is 7, and the frequency resolution of coarse tuning becomes 20 MHz/bit; this induces a unit capacitance of about 2.5 fF. The 7-bit CBANK is binary-weighted. Figure 4 shows the schematics of the unit capacitor bank, where OUT+, OUT- are VCO outputs, $C_{unit}$ is the unit capacitor, R is the bias resistor, and CB is the enable signal. When CB is 1, the unit capacitors are seen to the tank. However, when CB is 0, the only parasitic capacitance of the transistor is seen to the tank. For distinguishable switching, R should be sufficiently large, and $R_{on}$ of the transistor should be small. Usually, the pole frequency of the inherent high-pass filter is 20 times larger than the oscillation frequency. As the W/L ratio of the transistor increases, the Q-factor of the CBANK increases as $R_{on}$ decreases. However, the parasitic capacitance increases, and the maximum oscillation frequency decreases. Therefore, finding the optimal point is important. The value of R is 100 kOhm, and the size of the transistor is 800 n/60n.

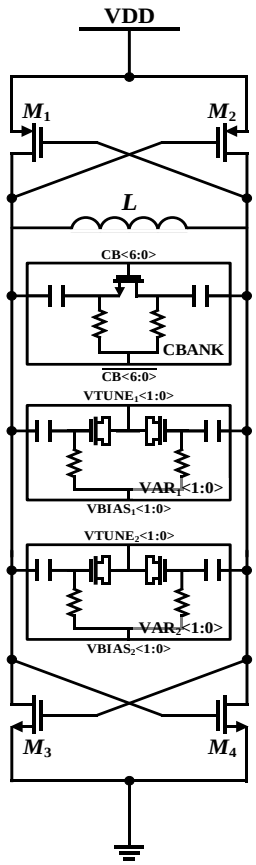


Fig. 6. Schematics of the *LC* VCO

Because the CBANK is binary-weighted, R becomes half, and the transistor size becomes double the bit increase.

Once the CBANK design is completed, the size of the varactors is determined to meet the given KVCO specification. Figure 5 shows the schematics of the varactors in the *LC* VCO. It consists of DC block capacitors, varactors, and bias resistors. Varactors are thick devices because the leakage current of thin devices is significant, which causes reference spurs in PLL. The DC block capacitors are 0.5 pF, and the resistors are 4.5 kOhm. For the main loop, to make the KVCO 50 MHz/V, the capacitance of the varactor is 22 to 28fF. In the same way, for the auxiliary loop, to make the KVCO 50 MHz/V, the capacitance of the varactor is 124 to 192 fF.

The gm cell size is directly related to the overall frequency, start-up, noise, and power of the VCO. The most important of these factors is the start-up. Usually, we set the start-up margin to be about 3 times larger than the Barkhausen criterion to ensure the oscillation of the VCO under PVT variations. After satisfying the start-up margin by changing the W/L ratio, the next step is to change the dimensions of the cell. A larger W·L value leads to a lower flicker noise corner, but it also decreases the frequency. Based on several simulations, the transistor dimension was fixed to 27 u/100n.

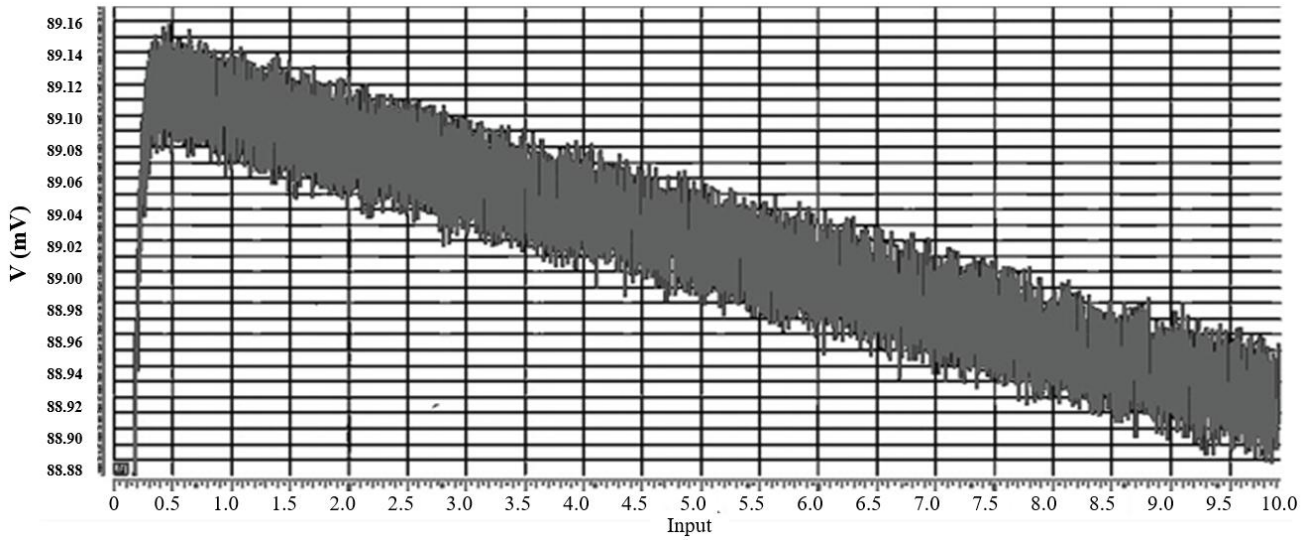


Fig. 7. Transient response of the out of DSM DAC and low pass filter.

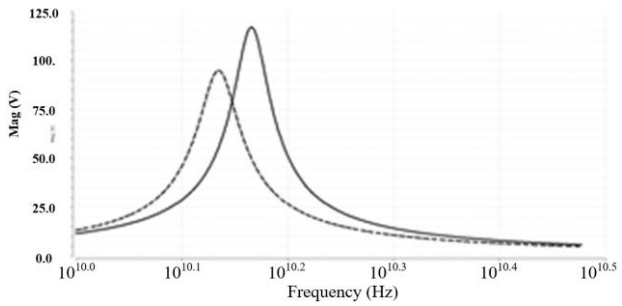


Fig. 8. Simulation results of the worst-case RP

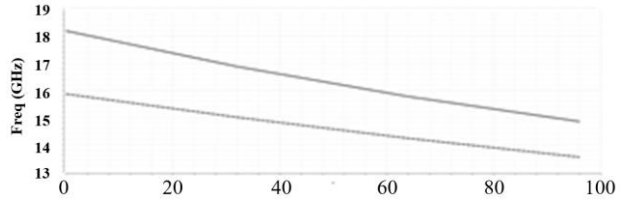


Fig. 9. Simulation results of frequency tuning range

The final version of the *LC* VCO (Fig. 6) consists of a CMOS-type gm cell, a spiral inductor, a 7-bit CBANK, two varactors ($VAR_1$) for the main loop with a 50-MHz/V KVCO, and two varactors ($VAR_2$) for the auxiliary loop with a 500-MHz/V KVCO.

## III. RESULTS AND DISCUSSION

Figure 7 shows the output transient result of the DSM DAC after the low-pass filter. As the input code of the DAC decreases, the output of the low-pass filter as well. Thanks to the DSM, the resolution of the DAC is significantly increased, and the low-pass filter filters out the high-frequency components. The remaining ripples are negligible at the output of the PLL.

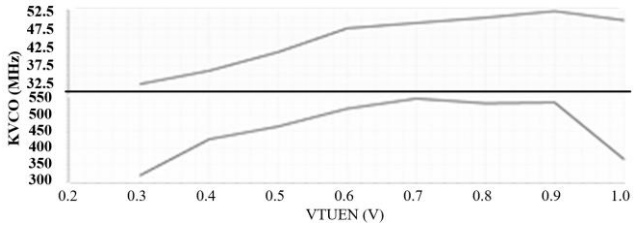


Fig. 10. Simulation results of KVCO of (up) main loop (down) auxiliary loop when VTUNE is changed from 0.2 to 1.0V

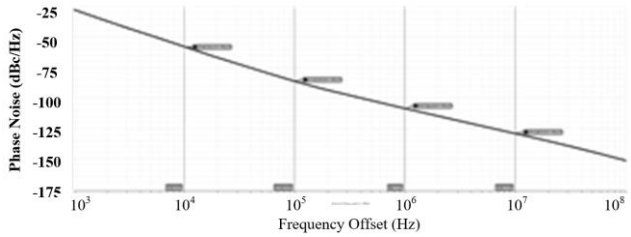


Fig. 11. Simulation results of the output phase noise @ 14.2GHz in schematic

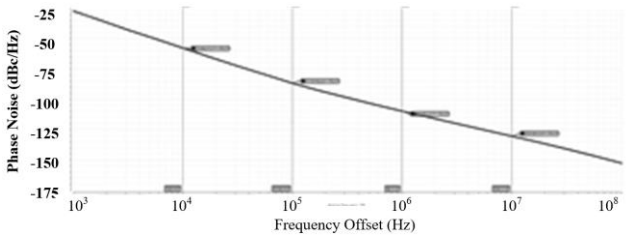


Fig. 12. Simulation results of the output phase noise @ 13.2GHz in PEX

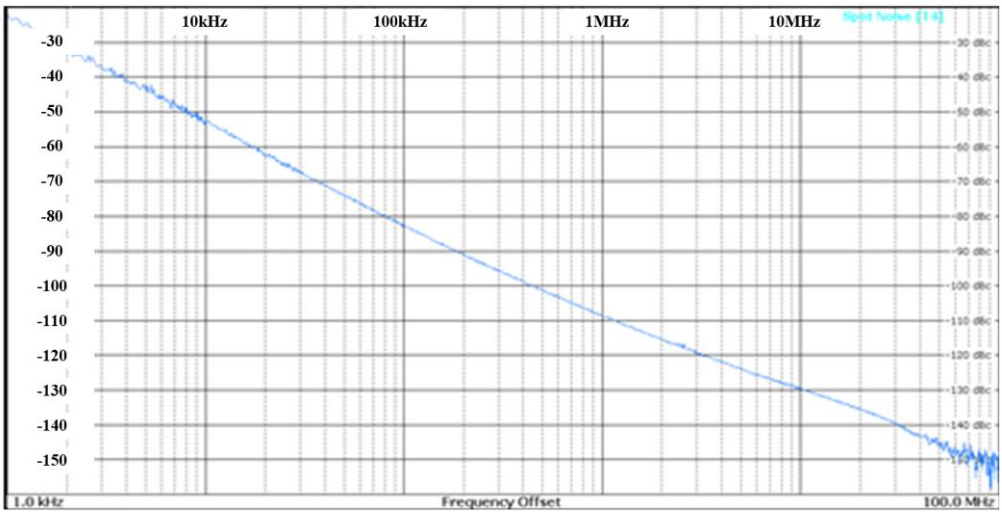


Fig. 13. Measured phase noise graph at 14GHz

Figure 8 shows the simulation results of the worst-case $R_P$. The solid line is the schematic simulation result, and the dashed line is the PEX simulation result. Because of the parasitic capacitance, in the PEX simulation, $R_P$ is reduced from 115 Ohm to 97 Ohm compared to that of the schematic simulation. Here, $g_m$ of the CMOS cross- coupled transistor is 30.5 mS. Therefore, in the schematic, the start-up margin is about 3, and in the PEX simulation, the start-up margin is nearly less than 3. In both cases, oscillation is guaranteed with sufficient a start-up margin.

Figure 9 shows the simulation results of the frequency tuning range. Likewise, the solid line is schematic, and the dashed line represents the PEX results. In the schematic, the frequency tuning range is 14 to 18.5 GHz. However, the frequency tuning range is still high in the PEX simulation result, 13.5 to 15.8 GHz. That is because the PEX results cannot count the parasitic inductance but capacitance. Also, dummy metal can decrease the oscillation frequency. Figure 10 shows the KVCO simulation results obtained at 14 GHz. As shown in the graph, both KVCOs of the main loop and the auxiliary loop meet the target specification, 52 MHz/V, and 550 MHz/V for each. Although is it slightly higher than the target, we can manage it with VBIAS. Figures 11 and 12 show the phase-noise results of schematic and PEX simulation. In both cases, the CBANK code is fixed to 127, which means that all of the capacitor units are on. The flicker noise corner is less than 500 kHz, which does not degrade the jitter performance of the PLL. At a 1-MHz frequency offset, the phase noise values are –108.8 dBc/Hz and –109.9dBc/Hz for schematic and PEX, respectively. The power consumption is 5.3 mW for both cases. The FOM of the VCO at a 1-MHz frequency offset is –184.8 dB and –184.9 dB for schematic and PEX, respectively, so the target FOM is satisfied in both cases.

In the measurements, the frequency was nearly 10% lower than the PEX results. This is the effect of parasitic inductance and dummy metal, which PEX does not consider. This amount of degradation is expected. The maximum frequency fell to 14.5 GHz from 15.8 GHz, and the minimum frequency fells to 12GHz from 13.5 GHz. Figure 13 shows the measured phase noise graph at 14 GHz.

The FOM of the VCO at a 1-MHz frequency offset was less than 184 dB when the phase noise was –109 dBc/Hz, and the power consumption was 5.5 mW. These measured results meet the design target specifications.

## IV. CONCLUSION

In this paper, the fundamentals of a DCO including a DAC, DSM, and VCO were presented, and the design of a low-phase-noise, high-resolution DCO was discussed. The DCO was designed for an ultra-low-jitter digital sub-sampling PLL. To suppress the enormous amount of quantization noise, a very fine frequency resolution is critical. Also, the phase noise of the *LC* VCO itself is crucial for ultra-low-jitter applications. For the high-performance *LC* VCO design, a basic insight into the oscillator is needed. The DCO consists of a string-type RDAC, a MASH 1-1 DSM, and a CMOS-type cross-coupled *LC* VCO. The frequency resolution is significantly increased by using the DSM. The proportional path has a 17-bit resolution, whereas the integral path has an 18-bit resolution. The DSM operates at 400 MHz, and its quantization noise is canceled by the $2^{nd}$-order low-pass filter at the output of the DAC. By adopting $2^{nd}$-order noise shaping, the quantization noise at the PLL output is negligible. The DAC was designed with a string resistor topology for design simplicity and relieved target specifications. The DCO has a 12 to 14.5 GHz frequency tuning range. The phase noise at a 1-MHz offset frequency is −109 dBC/Hz at a 14-GHz output. The average power consumption is 5.5 mW. The calculated FOM at a 1-MHz offset frequency is −184.5 dB.

## ACKNOWLEDGEMENT

This work was supported in part by the Industrial Technology Innovation Program of the Ministry of Trade, Industry & Energy (10080611), and in part by a National

Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) under grant NRF2020R1A2C2004260, and EDA tools were provided by IDEC, Korea.

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