A 6-Bit 2GS/s Sampling-Rate 27.8fJ/Conversion-Step 610-μm^2 Successive Approximation Register Time-to-Digital Converter

Youngwoo Kwon[1] and Hyungil Chae[a]
Department of Electrical and Electronics Engineering, Konkuk University
E-mail : youngwoo00@konkuk.ac.kr

***Abstract* - This paper proposes a small-area, low-power, and high-speed 6-bit SAR time-to-digital converter (TDC) for time-interleaved ADCs. The proposed architecture utilizes a selective delay tuning (SDT) cell to achieve a relatively large reference time step (T_{LSB}) of 4 ps. A T_{LSB} of 4 ps provides sufficient margin to ensure that the SAR TDC's performance remains dominant over the jitter from voltage-to-time converter (VTC) and TDC delay line thereby preventing SNDR degradation. Fabricated in a 28nm CMOS process, the proposed TDC occupies an active area of only 610 um^2. Proposed SAR TDC consumes 2.8mW from a 0.9V supply voltage. At a sampling rate of 2 GS/s, the design achieves an SNDR of approximately 36 dB. The proposed TDC demonstrates a compact area compared to prior arts and achieves a Nyquist FoM_W of 27.8 fJ/conv-step.**

***Keywords*— Analog-to-Digital Converter, Time-to-Digital Converter, Successive Approximation Register**

I. INTRODUCTION

High-speed data transmission and acquisition systems have driven increasing demand for high-speed (> 10 GS/s) , medium resolution (6~8 bits) Analog-to-Digital Converters (ADC). For this reason, the importance of Time-Interleaved (TI) ADCs has been increasing. In TI ADC architectures, the overall sampling rate increases proportionally with the number of slice ADCs, while the area also scales linearly. Although increasing the number of interleaving factor theoretically enables arbitrarily high sampling rates, non-idealities such as mismatch between slice ADCs, timing skew, and gain error become more pronounced as the number of slices increase. Therefore, minimizing the interleaving factor is critical for achieving high performance. Consequently, improving the speed and area efficiency of a single slice ADC is essential in TI ADC design.

a. Corresponding author; hichae@konkuk.ac.kr

Manuscript Received Mar. 25, 2026, Revised Jun. 15, 2026, Accepted Jun. 15, 2026
This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/4.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

Among various TI ADC implementations, voltage-domain ADCs such as Successive Approximation Register (SAR) ADCs and Charge-Injection (CI) SAR ADCs are widely adopted as slice ADCs. SAR ADCs are commonly used in TI ADC architectures due to their high linearity and excellent energy efficiency. However, achieving sampling rate beyond 1 GS/s at medium resolution remains challenging. In [1], a conventional SAR ADC is employed as a slice ADC, achieving a FoM_W of 47 fJ/conv-step. Nevertheless the sampling rate of a single slice ADC is limited to 875 MS/s, requiring more then ten slice ADCs to achieve an overall sampling rate exceeding 10 GS/s. To address this limitation, [2] improves the sampling rate of a single slice ADC to 1.15 GS/s by adopting loop unrolling. However, this approach requires multiple comparators, resulting in increased area per slice. In addition, comparator offset mismatch in TI ADC architectures can further degrade performance. Another voltage domain ADC, the CI SAR ADC, is also widely used due to its high speed and compact area [3]-[6]. The CI SAR ADC operates by sequentially discharging the sampling capacitor in a binary manner using multiple CI-cells. Since CI cells can be reused during conversion, the overall area can be significantly reduced compared to SAR ADCs. However, as the conversion progresses, the voltage on the sampling capacitor continuously decreases, which degrades linearity. Furthermore, similar to SAR ADCs, the sequential nature of the conversion limits the achievable sampling rate.

To overcome the speed limitations of conventional voltage domain ADCs, hybrid (voltage domain + time domain) ADCs and time-domain ADCs have been actively investigated. A hybrid ADC partitions the overall conversion process between the voltage domain and the time domain, where each domain resolves a portion of the total bits [7]-[9]. Typically, the MSBs are first converted in the voltage domain, and the residue voltage is then converted into the time domain input signal using a Voltage-to-Time Converter (VTC). The remaining LSBs are subsequently resolved by a TDC. Alternatively, a reverse approach can be employed, where the MSBs are first resolved in the time domain, followed by conversion into the voltage domain using a

Time-to-Voltage Converter (TVC), and the remaining LSBs are then processed in the voltage domain. However, in this case, the VTC, TVC, and SAR conversion must all be completed within a single clock cycle, which limits the achievable sampling rate compared to the former approach. By leveraging VTCs and TVCs, hybrid ADCs can perform voltage-domain and time-domain conversions in a pipelined manner, enabling higher speed compared to conventional voltage domain ADCs. However, when employed as slice ADC in TI ADC architectures, gain mismatch between the voltage and time domains must be calibrated for each slice, resulting in increased system complexity.

In contrast, time-domain ADCs convert the sampled input voltage into the time domain using a VTC and perform the entire conversion in the time domain [10]-[15]. Since no voltage domain conversion is involved, this approach enables very high speed operation. Among various time-domain ADC architectures, the SAR TDC achieves high speed by enabling pipelined operation across conversion stages. In addition, compared to TDC architectures such as flash-based TDC, it features a shorter conversion path, leading to lower power consumption and compact footprint. For these reasons, the time-domain ADC using SAR TDC architecture is well suited as a slice ADC in TI ADC systems.

This paper proposes a high-speed, low-power, and area-efficient ADC based on a SAR TDC architecture. The reference time step (T_{LSB}) is determined based on the ideal SNR requirement, and a selective delay tuning (SDT) cell is used to generate accurate binary scaled delay steps. By leveraging the inherent advantage of the SAR TDC architecture, all conversion stages are fully pipelined to achieve high conversion speed [15]. In addition, two redundant bits are introduced at the end of the LSB conversion stage to effectively mitigate accumulated decision errors of the time comparator and mismatch in the SDT cells, thereby improving overall conversion accuracy.

II. DESIGN METHODOLOGY

A. Proposed SAR TDC Architecture

Fig. 1 shows the overall architecture of the proposed SAR TDC. A 20-fF sampling capacitor is used for input signal sampling, and a 40-fF capacitor is employed at V_{VTC} node for the VTC operation. Since the input signal does not require a large input swing, a transmission gate is used for the input switch instead of a bootstrapped switch.

Fig. 2 shows the timing diagram of the proposed SAR TDC. Using the SH signal, the input signal is sampled on to $VTOP_P$ and $VTOP_N$. Afterward, when the VTC_EN signal goes high, the VTC operation begins. At the same time, $VTOP_P$ and $VTOP_N$ are discharged. During this process, when the voltages of $VTOP_P$ and $VTOP_N$ fall below the threshold voltage of the sensing inverter in the VTC, T_P and T_N signals which serve as the inputs to the TDC goes high thereby initiating the TDC operation. Since all stages of the TDC are pipelined in a loop-unrolling manner, the next input signal can be sampled immediately after the VTC operation is completed, enabling a high sampling rate of 2 GS/s.

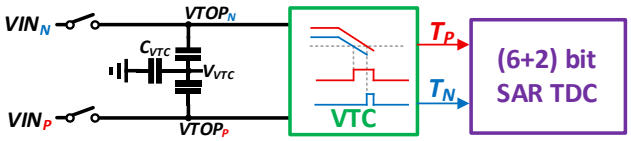

Fig. 1. Overall architecture of the proposed SAR TDC

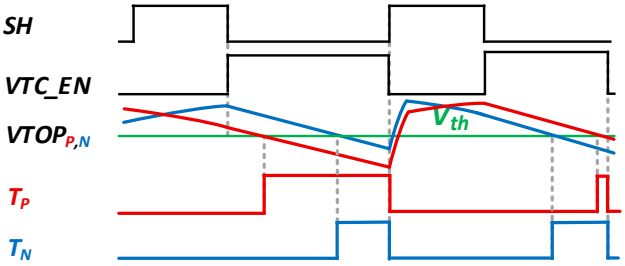

Fig. 2. Timing diagram of the proposed SAR TDC

$$SNR_{ideal} = \frac{2^N * T_{LSB}}{8 * \left((\sigma_{j,VTC})^2 + (\sigma_{j,TDC})^2 + \frac{T_{LSB}^2}{12} \right)} \quad (1)$$

B. Determination of the T_{LSB} in SAR TDC

Several factors degrade the SNDR of a SAR TDC, among which the most dominant ones are the jitters originating from the delay line and the VTC. As the conversion proceeds toward the LSB, the jitter from the delay line accumulates, which degrades the overall performance. The ideal SNR of the SAR TDC can be calculated as (1). T_{LSB} denotes the reference time step of the SAR TDC, while $\sigma_{j,VTC}$ and $\sigma_{j,TDC}$ represent the jitter originating from the VTC and the TDC delay line respectively. As can be observed from (1), in order to achieve the desired SNR in a SAR TDC, the jitters from the VTC and the delay line should be minimized, while T_{LSB} should be increased. In [8], the ideal SNR of a SAR TDC was calculated similar to (1), but $\sigma_{j,VTC}$ which occupies a similar portion as $\sigma_{j,TDC}$ was neglected in the calculation process. From simulation results, the measured $\sigma_{j,VTC}$ and $\sigma_{j,TDC}$ were 420 fs and 358 fs, respectively. In this work, for a 6-bit target SAR TDC, the calculated value of the T_{LSB} is 4.3 ps in order to achieve the ideal SNDR of 37.88 dB corresponding to a 6-bit resolution. However, increasing T_{LSB} proportionally increases the time-domain full-scale range, which in turn reduces the achievable sampling rate of the SAR TDC. Therefore, considering both speed and SNR, this work adopted 4-ps reference time step.

C. Circuit implementation

Fig. 3 illustrates the architecture of the VTC employed in this work [8]. Prior to the VTC operation, the bottom plates of the two sampling capacitors are precharged to V_{DD} by the VTC_ENb signal. Once the sampling is complete, the VTC_EN signal triggers the discharge of this bottom plate. Consequently, the voltages at nodes $VTOP_P$ and $VTOP_N$ decrease. When they fall below the sensing inverter's threshold voltage, the T_P and T_N signals go high, generating the time-pulse signals that serve as the input for the SAR TDC. Since the bottom plates of two sampling capacitors are connected and a single current source is used, mismatch

between current sources is eliminated, resulting in improved performance. To minimize the VTC conversion time for higher sampling rate, the input common-mode voltage was set near the threshold voltage of the sensing inverter.

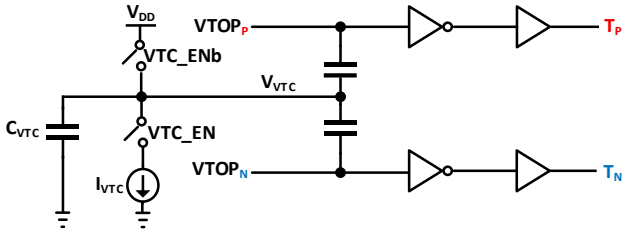

Fig. 3. VTC structure used for SAR TDC

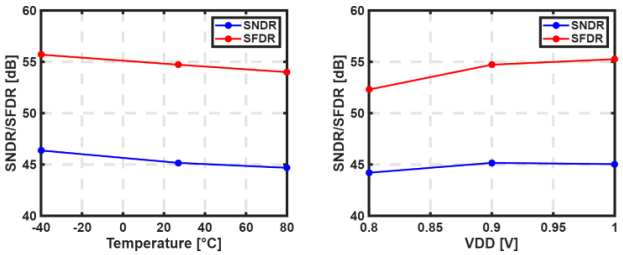

Fig. 4. Simulated SNDR/SFDR plot of VTC by sweeping supply voltage and temperature

Fig. 4 shows the simulated SNDR and SFDR of the VTC while sweeping temperature and supply voltage. The result shows stable performance of the VTC across varying temperature and supply voltage.

Fig. 5 illustrates the architecture of the (6+2) bit SAR TDC employed in this work [8], and Fig. 6 shows the SDT cell used in this work. The SDT cell changes the pull-down current at the MID node according to the time comparator′s decision result SelP,N, thereby making the desired delay. Compared to the traditional SAR TDC structure employing capacitors and MUXs, the SDT cell-based approach reduces the total transistor making the delay difference, thereby achieving a more compact area. A delay cell is inserted between the stages to prevent the time pulse signal from reaching the SDT cell input before the comparator′s decision result is fully resolved. The binary scaled delay is achieved by appropriately changing the size of the SDT cells. As shown in [14], two redundant bits are inserted at the end of the conversion line. These redundant bits serve to compensate for the accumulated errors within the TDC during the conversion process. For these bits, weights of 2-LSB and 1-LSB are employed. Since all steps of the SAR TDC are fully pipelined in the proposed architecture, only the sampling and VTC operation need to completed within a single phase. Therefore, it was possible to achieve high sampling rate of 2 GS/s. The variations in the SDT cell were compensated by employing redundant bits and digital foreground weight calibration.

The time comparator used for the decision in SAR TDC is shown in Fig. 7 [13]. It begins to operate asynchronously upon the input arrival, and a simple NOR gate is used to generate CLKDetect to catch the time comparator′s output. M5 and M6 are the input devices, and the earlier of TP and TN determines the regenerative latch (M1-4) output VP,N. The devices M7-10 are reset switches to prevent any glitch the following SR latch, which generates SelP,N signal used for the SDT cells. To enable pipeline operation, multiple flip-flops are connected in series, and all outputs are aligned using the CLK_{Detect} signal of the final stage.

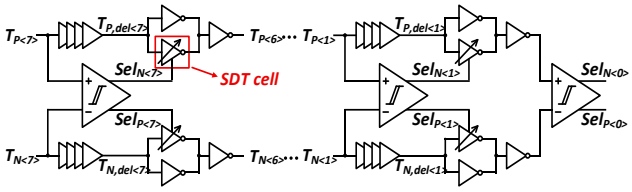

Fig. 5. Proposed (6+2) bit SAR TDC

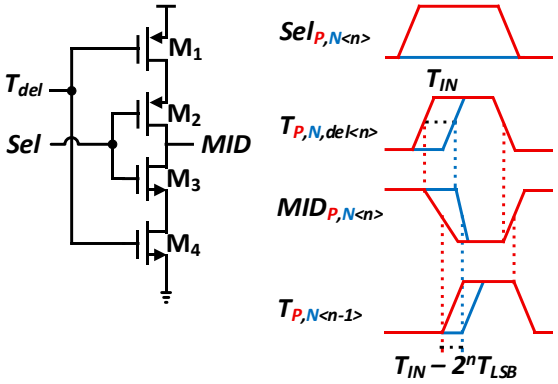

Fig. 6. SDT cell used for SAR TDC

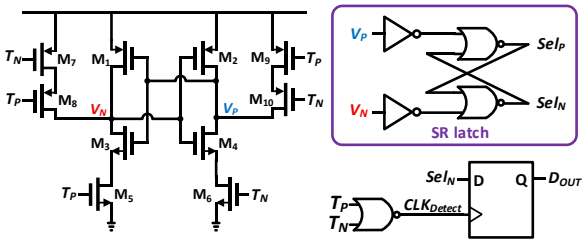

Fig. 7. Time comparator for SAR TDC

III. MEASUREMENT RESULTS

Proposed SAR TDC is fabricated with 28-nm CMOS process. The core area is 10.3 um by 61 um. Fig. 8 shows the die photo and core layout. The supply voltage of this ADC is 0.9 V, with a 0.56-V differential p-p input voltage range with an input V_{cm} of 0.7 V. The variation of the SDT cell is calibrated in the digital domain using digital foreground calibration. Fig. 9 shows the output power spectral density measured at a sampling rate of 2 GS/s with inputs of 297.7 MHz and 997.7 MHz. The maximum SNDR is measured to be 36.28/35.81 dB respectively, and the SFDR is 52.45/48.93 dB. Fig. 10 (left) shows the measured SNDR/SFDR while sweeping sampling frequency from 1.3 GHz to 2 GHz. Fig. 10 (right) shows the measured SNDR/SFDR while sweeping input frequency from 297.7 MHz to 997.7 MHz. Fig. 11 shows the measured DNL and INL, which are -0.38/0.31 LSB and -0.24/0.28 LSB respectively. Fig. 12 (left) shows the measured dynamic range, which is 36 dB. Fig. 12 (right) shows the power breakdown of the proposed SAR TDC. SAR TDC consumed the largest portion of the total power,

followed by the VTC+SW and DATA Align blocks. The total power consumption of the proposed SAR TDC was 2.8 m Wat sampling rate of 2 GS/s. TABLE I summarizes the performance of the proposed ADC and compares it with state-of-the-art for similar Time-domain ADCs and voltage domain ADC. Compared with other time-domain ADCs, the proposed ADC achieves a high speed-per-area performance than other time-domain ADCs, while maintaining a competitive FoM_W. Compared to voltage domain ADC, a much higher sampling rate is achieved.

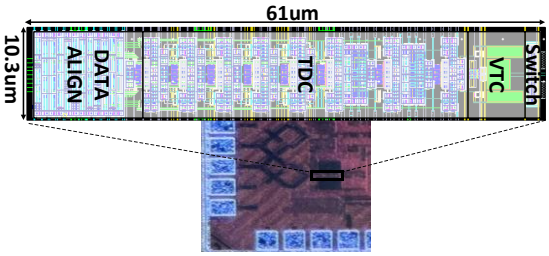

Fig. 8. Die photo and core layout of the proposed ADC

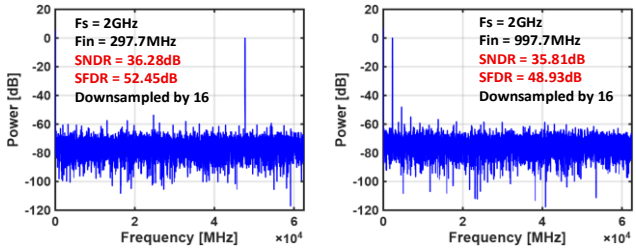

Fig. 9. Measured PSD at low input (left) and Nyquist input (right)

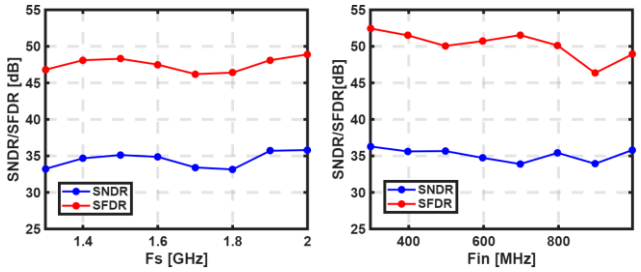

Fig. 10. Measured SNDR/SFDR vs sampling frequency (left), vs input frequency (right)

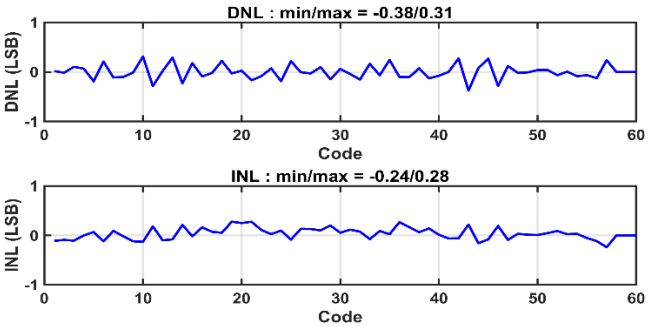

Fig. 11. Measured INL/DNL

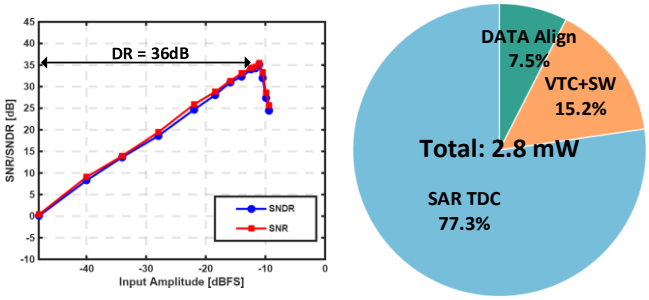

Fig. 12. DR and Power breakdown

IV. CONCLUSION

This paper presents a compact area and high-speed SAR TDC. The proposed ADC utilizes a SAR TDC architecture and achieves lower power consumption and smaller area compared to other time-domain ADCs. In addition, the dominant factor that degrade the SNDR of a SAR TDC, namely the jitter from the VTC and the jitter from the TDC delay line, are analyzed to determine a relatively large 4-ps reference time step. Furthermore, 2-bit redundant bits are inserted after the 6-bit SAR TDC to compensate for the SDT cell mismatch and decision errors from the time comparator. As a result, the proposed 6-bit target ADC achieves an SNDR of 35.81 dB with a Nyquist input, resulting in a competitive Walden FoM of 27.8 fJ/conv-step. Moreover, very small area of 610 um^2 makes this design suitable for slice ADC in TI ADCs.

TABLE I. Performance Summary and Comparison

	This Work	[14]	[11]	[12]	[10]	[2]
Architecture	**SAR TDC**	SAR TDC	SAR TDC	Interpolation TDC	GRO based TDC	SAR ADC
Technology[nm]	**28**	4	14	28	28	28
Supply [V]	**1**	0.9/0.75	0.8	1	1	1.1
# Channels	**1**	4	1	4	1	4
Sub-channel Fs [GS/s]	**2**	4	5	2.5	2	1.125
Resolution [bits]	**6**	10	8	8	7	7
SNDR @Nyq [dB]	**35.81**	44.5	40.8	40.1	36.85	39.72
Power [mW]	**2.8**	94.2	7.4	23.2	3.65	6.56
Sub-Channel Area [um^2]	**610**	2000	1425	23750*	4000	7290*
FoM_w [fJ/conv-step]	**27.8**	42.9	16.6	61.5	31.4	18.5
$FoM_{schreier}$[dB]	**151.4**	153.8	156.1	150	151.2	155.07

*estimated

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

REFERENCES

[1] A. S. Yonar et al., "An 8-bit 56GS/s 64x Time-Interleaved ADC with Bootstrapped Sampler and Class-

AB Buffer in 4nm CMOS," 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2022, pp. 168-169, doi: 10.1109/VLSITechnologyandCir46769.2022.9830308.

[2] Y. -H. Wang and S. -J. Chang, "A 7b 4.5GS/s 4× Interleaved SAR ADC with Fully On-Chip Background Timing Skew Calibration," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 16-18, doi: 10.1109/ISSCC42615.2023.10067573.

[3] K. D. Choo, J. Bell and M. P. Flynn, "27.3 Area-efficient 1GS/s 6b SAR ADC with charge-injection-cell-based DAC," *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2016, pp. 460-461, doi: 10.1109/ISSCC.2016.7418106.

[4] C. -H. Kye and K. Choo, "A 0.000261 mm2 Single-Channel 1 GS/s 8-Bit 3-Stage Capacitor Array-Assisted Charge-Injection DAC-Based SAR ADC in 28 nm CMOS," *2023 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Haikou, China, 2023, pp. 1-3, doi: 10.1109/A-SSCC58667.2023.10347948.

[5] J. Park, J. Park, S. Song and H. Chae, "A 17-fJ/conv-step FoMw and 259-um2 7-Bit C-CIDAC SAR ADC," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 11, pp. 1535-1539, Nov. 2025, doi: 10.1109/TCSII.2025.3581255.

[6] J. Kim, G. Cho and J. Kim, "A 7GHz ERBW 1.1GS/s 6-bit PVT Tolerant Asynchronous CI-SAR with only 8.5fF Input Capacitance," *2023 IEEE Custom Integrated Circuits Conference (CICC)*, San Antonio, TX, USA, 2023, pp. 1-2, doi: 10.1109/CICC57935.2023.10121269.

[7] A. Whitcombe *et al*., "22.3 A 76mW 40GS/s 7b Time-Interleaved Hybrid Voltage/Time-Domain ADC with Common-Mode Input Tracking," *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2024, pp. 392-394, doi: 10.1109/ISSCC49657.2024.10454355.

[8] A. Whitcombe *et al*., "A 6.0mW 3.8GS/s 7b VTC/TDC-Assisted Interleaved SAR ADC with 13GHz ERBW," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, Honolulu, HI, USA, 2022, pp. 170-171, doi: 10.1109/VLSITechnologyandCir46769.2022.9830329.

[9] H. Liang *et al*., "A 32GS/s 8b 16× Time-Interleaved Hybrid ADC with Self-Detection Offset Calibration, DLL-Based TLSB PVT Variation Calibration and VTC Gain Self-Tracking," *2025 IEEE Custom Integrated Circuits Conference (CICC)*, Boston, MA, USA, 2025, pp. 1-3, doi: 10.1109/CICC63670.2025.10983486.

[10] C. Zhang, J. Wei, Y. Chen, M. Liu and Y. Yang, "A 0.004-mm2 3.65-mW 7-Bit 2-GS/s Single-Channel GRO-Based Time-Domain ADC Incorporating Dead-Zone Elimination and On-Chip Folding-Offset Calibration in 28-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 11, pp. 3179-3193, Nov. 2023, doi: 10.1109/JSSC.2023.3282412.

[11] J. Liu, M. Hassanpourghadi and M. S. -W. Chen, "A 10-GS/s 8-bit 2850-μm2 Two-Step Time-Domain ADC With Speed and Efficiency Enhanced by the Delay-Tracking Pipelined-SAR TDC," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3757-3767, Dec. 2022, doi: 10.1109/JSSC.2022.3196924.

[12] M. Zhang, Y. Zhu, C. -H. Chan and R. P. Martins, "16.2 A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input," *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2020, pp. 252-254, doi: 10.1109/ISSCC19947.2020.9062986.

[13] Q. Chen, C. C. Boon, Q. Liu and Y. Liang, "A Single-Channel Voltage-Scalable 8-GS/s 8-b >37.5-dB SNDR Time-Domain ADC With Asynchronous Pipeline Successive Approximation in 28-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1610-1622, June 2023, doi: 10.1109/JSSC.2022.3230697.

[14] J. Liu, A. Shabra, S. Ho, G. Manganaro and M. Shuo-Wei Chen, "A 16GS/s 10b Time-domain ADC using Pipelined-SAR TDC with Delay Variability Compensation and Background Calibration Achieving 153.8dB FoM in 4nm CMOS," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2, doi: 10.1109/VLSITechnologyandCir46783.2024.10631373.

[15] H. Chung, H. Ishikuro and T. Kuroda, "A 10-Bit 80-MS/s Decision-Select Successive Approximation TDC in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 5, pp. 1232-1241, May 2012, doi: 10.1109/JSSC.2012.2184640.

Youngwoo Kwon received the B.S. degree in electrical engineering from Konkuk University, Seoul, Korea, in 2024 and is currently working toward the M.S. degree in electrical engineering at Konkuk University.

His research during M.S. course has focused on analog to digital converter.

Hyungil Chae received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2004 and the M.S degree in electrical engineering from University of Michigan, Ann Arbor, MI in 2009 and PH.D. in electrical engineering from University of Michigan, Ann Arbor, MI, in 2013