# An mm-Wave Wilkinson Combiner with Stacked Coupling and Capacitive Loading Technique

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***Abstract* - This paper introduces a small Wilkinson power combiner (WPC) created in a 0.18 μm CMOS process for use in millimeter-wave systems. The suggested combiner substitutes typical λ/4 microstrip arms with stacked coupled transmission-line segments, which are made on the uppermost metal pair (M5/M6). This allows for significant vertical coupling and field confinement, which raises the effective phase constant and decreases the physical arm length. Furthermore, distributed capacitive loading is added along the arms to create a slow-wave effect and adjust the arm susceptance for better input matching. A small trim capacitor at the combining node also corrects for any remaining pad/transition reactance. Measurements taken around 60 GHz show an insertion loss of 0.6 dB, a return loss of -19 dB, and an isolation of -36 dB within a small area of 0.28 mm$^2$. In comparison to current CMOS combiners, the presented method strikes a good balance between size reduction and electrical performance, delivering a CMOS-compatible, low loss, and high isolation option ideal for compact millimeter-wave phased-array and highly integrated front-end systems.**

***Keywords*— Wilkinson power combiner, stacked coupling, capacitive loading, CMOS, millimeter-wave.**

## I. INTRODUCTION

Wilkinson power divider/combiner (WPD) remains a simple building block for RF and millimeter-wave systems because it can offer good input matching with high port-to-port isolation along with the required power split. The conventional two λ/4 transmission-line-section implementation in integrated CMOS, however, pays dearly in terms of chip area and non-trivial loss in back-end metals, a cost that increases as phased-array transceivers move towards dense system-on-chip integration. In order to treat footprint and loss simultaneously, several miniaturized methods have been explored in the literature [1]. For starters,

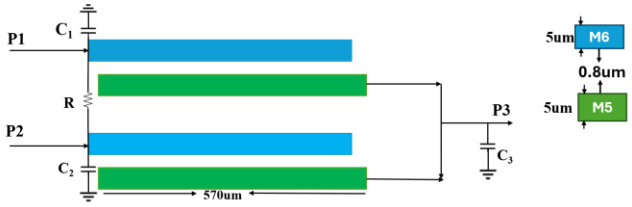


Fig.1. Proposed design of stacked couple lines and capacitive loading

"folded" (typically two-stage) Wilkinson topologies miniaturize electrical length by taking sections over multiple layers, roughly halving footprint with respect to a typical two-stage realization without sacrificing wideband performance in the mid millimeter-wave range [1]. Second, silicon IPD technology's periodically synthesized transmission lines provide a small wideband transformation network with high isolation and matching of use where area is at a premium and low-parasitic passives are available [2]. Third, stub-loaded raised-CPW structures take advantage of slow-wave effects to decrease the effective electrical length and achieve high-impedance segments on silicon; this makes aggressive on-chip miniaturization at about 60–67 GHz possible with realistic matching and isolation in CMOS [3]. At higher bands, silicon/IPD demonstrations at W-band level have been reported to have -1 dB-class insertion loss with useful isolation in small cores [4], and III–V IPD platforms have enabled low-loss, small, dual-band 28/60 GHz dividers for multi-standard front ends [5]. Although all these advances, the majority of compact solutions still rely on long EM-tuned coupled sections or large slow-wave loads that add loss; some of them are non-CMOS technologies, which are more challenging for co-integration with power amplifiers and transceivers. This prompts Wilkinson architecture that simultaneously meets a genuinely small silicon area, low insertion loss and successful isolation over millimeter-wave bandwidths without recourse to ungainly branches or very lossy coupling networks. In the current paper, we attempt that aim by combining stacked (broadside) coupled lines and distributed capacitive loading in 0.18 μm CMOS to reduce the physical path needed, confine fields between successive metals, and complete the impedance

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synthesis for matching and isolation thereby targeting sub-dB-class insertion loss, high isolation, and balanced outputs within a form factor suitable to phased-array and PA-combining applications, based on miniaturization and performance trends depicted in you [6]-[7].

## II. DESIGN METHODOLOGY

The proposed Wilkinson power combiner, depicted in Fig. 1 is built utilizing 0.18 µm CMOS technology. It uses the uppermost metal pair (M5–M6) to make the most of conductor thickness, lessen ohmic loss, and enhance electromagnetic field confinement. For each quarter-wave arm, a three-dimensional stacked (broadside) coupled-line configuration is used instead of a standard single microstrip line. The two metal traces are vertically arranged with a space of roughly 0.8 µm between them, while the line width is held at 5 µm to preserve consistent impedance control and low series resistance. In comparison to edge-coupled lines, the broadside setup generates considerably greater magnetic and electric coupling because of the diminished vertical separation and overlapping field distribution. This improved coupling raises the effective propagation constant and permits the necessary electrical length to be attained with a considerably shorter physical line, which contributes directly to a decrease in chip area and lower integrated attenuation. To additionally improve broadband matching and miniaturization, the design includes three distributed capacitors. Two matching shunt capacitors, $C_1$ and $C_2$, each having a value of 24.1 fF, are positioned symmetrically along the two input branches. These capacitors deliberately create a slow-wave effect by raising the effective per-unit-length capacitance

$$C'_{\text{eff}} \approx C' + \frac{C_1+C_2}{l_{\text{arm}}} \quad (1)$$

of the transmission lines, thus boosting the phase constant without lengthening the physical size.

$$\beta = \omega\sqrt{L'C'_{\text{eff}}} \quad (2)$$

Consequently, the necessary quarter-wave phase shift at the intended millimeter-wave frequency can be achieved using a small metal length.

Producing a slow-wave factor is as

$$S = \frac{\beta_{\text{loaded}}}{\beta_{\text{unloaded}}} > 1 \quad (3)$$

and therefore reducing the required physical quarter-wave length as

$$l_{\text{loaded}} = \frac{l_0}{S} \quad (4)$$

In this work, the slow-wave behavior is validated by DTA/EM extraction

$$S_{\text{DTA}} = \frac{\beta_{\text{loaded}}}{\beta_{\text{unloaded}}} \quad (5)$$

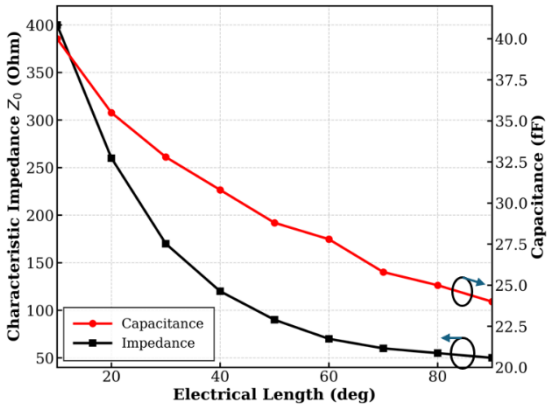


Fig. 2. Characteristic impedance and loading capacitance versus electrical length of the modified transmission line at 60 GHz.

while keeping a reasonable characteristic impedance. In contrast to typical miniaturization methods[8]-[10] that depend on very narrow or high-impedance lines above 100 Ω, the presented stacked design keeps a workable impedance near 50 Ω. This enhances manufacturing stability, lowers sensitivity to lithography changes, and reduces conductor loss. The distributed loading also offsets remaining inductive parasitics from vias, metal transitions, and pad interfaces, improving return loss across a larger frequency range. A third adjustment capacitor, $C_3$, with a value of 24.1 fF, is positioned at the combining point. This capacitor precisely adjusts the output susceptance and counteracts the concentrated parasitic reactance related to the junction discontinuity and output pad. By offsetting the remaining capacitive and inductive elements, $C_3$ improves the input matching response and stabilizes the phase balance between the two branches. This correction enhances wideband impedance matching and lessens phase variation throughout the operating range, which is essential for phased array and beamforming uses where uniformity in amplitude and phase directly impacts array effectiveness. High isolation between the two input ports is achieved using a polysilicon isolation resistor connected between the arms in the conventional Wilkinson setup. The resistor's shape is carefully designed to guarantee a precise resistance level, minimal unwanted capacitance, and consistent temperature performance at millimeter-wave frequencies. When odd-mode signals are applied, the resistor soaks up the varying power resulting from input differences or unevenness, which stops signal escape between ports and keeps them separate. In even-mode operation, ideally no current flows through the resistor, so it doesn't add to signal weakening. This system makes sure the ports stay well-isolated from each other, while also keeping the extra signal loss low along the main path. The combination of layered linking and capacitive load offers two benefits at once. Firstly, the powerful vertical linking boosts the effective inductive interaction between the lines, increasing the phase constant and cutting down on the required physical length. Secondly, the capacitive load further improves the slow-wave effect without greatly increasing dielectric loss, since most of the electromagnetic field stays within the upper metal layers instead of going into the lossy silicon base. The diminished electrical path also

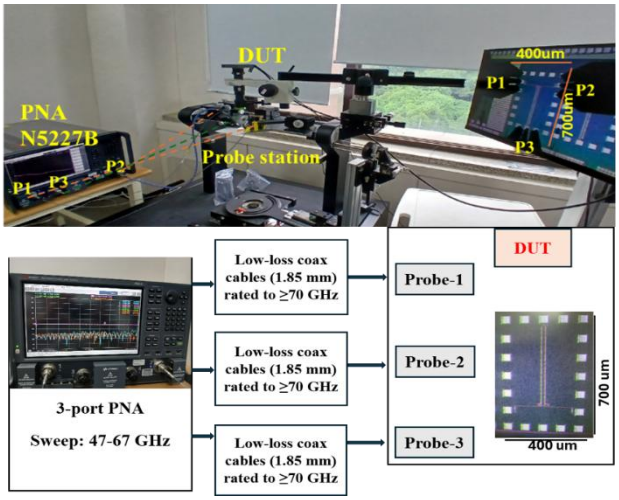


Fig.3. Measurement setup

lessens overall conductor and dielectric weakening. Taken together, these results allow for small layout sizes while keeping signal loss low and impedance matching broad [11]-[14]. Fig. 2 illustrates the trade-off between physical electrical length, characteristic impedance, and required loading capacitance. As the physical length decreases, a larger effective capacitance is required to maintain the same electrical phase. However, the proposed stacked configuration allows this capacitance to be realized using moderate capacitor values (24.1 fF) and practical line impedances around 50 Ω, avoiding unrealistic geometries. This balanced approach maintains manufacturability while delivering strong miniaturization and stable RF performance. In summary, the presented Wilkinson combiner attains a small size using stacked broadside coupling and slow-wave capacitive loading, obtains wideband matching with distributed and trimming capacitance, and achieves significant isolation via a precisely tuned thin-film resistor. Employing thick top metals and managed electromagnetic confinement reduces conductor and substrate losses, leading to minimal additional attenuation despite a substantial decrease in area. These attributes render the suggested configuration appropriate for highly integrated millimeter-wave front-ends and future 5G/6G beamforming systems [15]-[18].

## III. RESULTS & DISCUSSION

The fabricated Wilkinson power combiner was measured as shown in Fig. 3 using an Agilent PNA-X N5247B vector network analyzer (VNA) in conjunction with a Cascade Microtech ground-signal-ground (GSG) probe station. Three GSG probes were employed to contact the input and output ports, enabling full two-port and three-port S-parameter characterization. On-wafer calibration was performed up to the probe tips to ensure accurate de-embedding of pad parasitic and interconnect effects. All measurements were carried out at 60 GHz under standard laboratory conditions. The proposed Wilkinson power combiner was fabricated in a standard 0.18 μm CMOS process and characterized at 60 GHz. The measured results demonstrate an insertion loss of

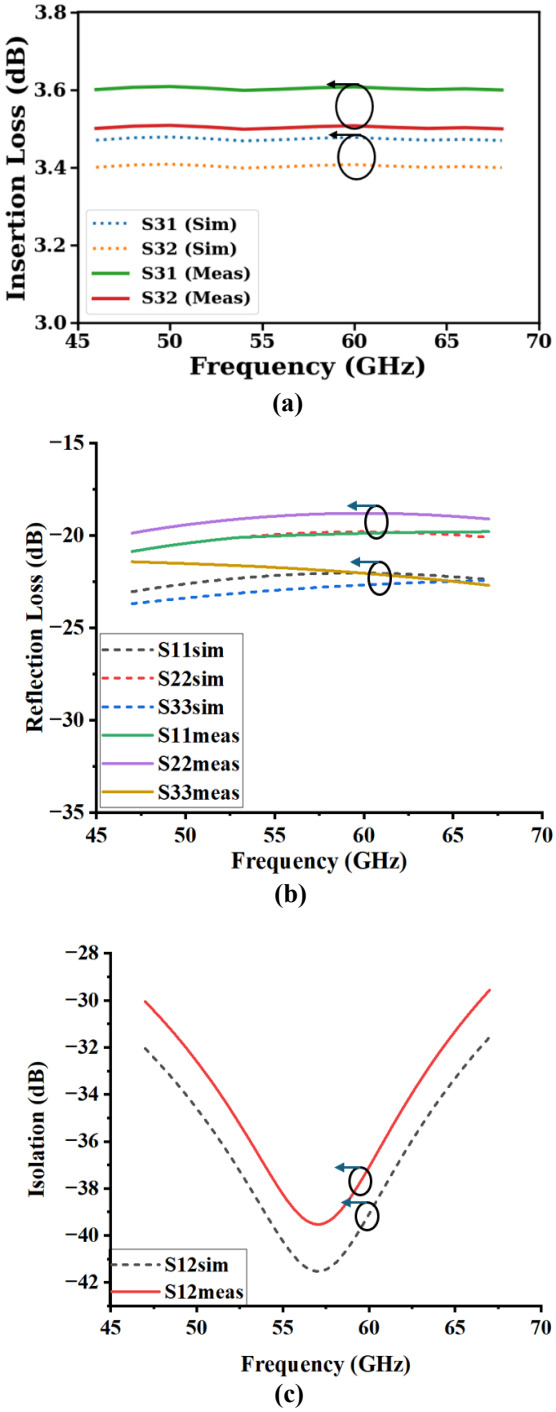


Fig. 4. Simulation and measurement results (a) Insertion loss, (b) Reflection loss and (c) Isolation

0.6 dB, return loss better than -19 dB, and isolation exceeding -36 dB, The total chip area is only (400 μm X 700 μm) 0.28 mm$^2$, which represents a 83 % reduction compared to conventional CMOS Wilkinson dividers [14] whose dimension is 0.8 mm X 2.1 mm. As shown in Fig. 4 The measured S-parameters confirm excellent agreement with simulations, validating the effectiveness of the stacked coupling and capacitive loading technique. Furthermore, the

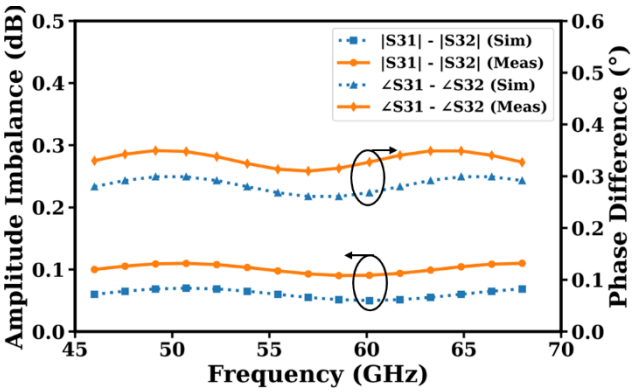


Fig. 5. Amplitude imbalance and phase difference

validation process for system performance involves comparing it against the Wilkinson power divider [19] which uses folded inductors as described in the reference. The design features a tiny footprint which measures 0.0361 mm$^2$ and works between 15-55 GHz, but it produces higher insertion loss values between 3.5 and 4.17 dB. The device provides isolation levels which reach only above 10 dB while it maintains signal amplitude imbalance below 0.2 dB and phase difference under 3°. The proposed design demonstrates better RF performance than the previous design because it decreases insertion loss by about 0.6 dB and it improves isolation by more than 25 dB. The design also delivers superior signal stability regarding both amplitude and phase characteristics; amplitude imbalance is under 0.1 dB and phase imbalance is under 0.3 ° shown in Fig. 5 The general consistency between simulation and measurement validates the substantial symmetry of the suggested structure. The remarkably minor amplitude and phase imbalance indicate that the stacked coupled-line arrangement and distributed capacitive loading successfully maintain equal power division and phase uniformity among the output ports. This level of performance is essential for Millimeter-wave phased array and beamforming applications, as even slight discrepancies can diminish array efficiency and beam precision.

## IV. CONCLUSION

A small Wilkinson power combiner, utilizing stacked (broadside) coupled transmission lines with distributed capacitive loading, has been created using a 0.18 µm CMOS process. By using strong vertical coupling on the M5/M6 metal pairing, the suggested design boosts the effective phase constant and permits a shorter quarter-wave transformation, while keeping conductor loss minimal by using wide top-metal traces. Furthermore, the incorporated capacitors adjust the arm susceptance and offset remaining parasitics, leading to enhanced broadband matching and consistent combining performance within a considerably smaller chip area. Measurements show an insertion loss of 0.6 dB, a return loss of -19 dB, and an isolation of -36 dB, accomplished in a small active-array-suitable area of 0.28 mm$^2$. In comparison to current advanced CMOS combiners, the presented design provides a good balance between size reduction and electrical performance, notably regarding isolation and area efficiency, while preserving complete CMOS process compatibility without the need for external IPD technologies. These findings prove that stacked coupling and capacitive slow-wave loading are useful, scalable design methods for future millimeter-wave integrated front-ends, where dense phased-array integration needs low-loss, well-matched, and highly isolated passive combining networks in the smallest silicon area possible.

TABLE I. Comparison Table with Existing Technology

| Specification | This Work | Ref [1] | Ref [2] | Ref [3] |
|---|---|---|---|---|
| Frequency (GHz) | 47-67 | 30 | 15-40 | 60 |
| Topology | Stacked coupling + capacitive loading | Folded using CPW | Periodic CCS* | Stub loaded CPW** |
| Technology | 0.18 µm CMOS | GaAs HBT | IPD | 90 nm CMOS |
| Insertion loss (dB) | <0.6 | <2 | <1.2 | <2.3 |
| Isolation (dB) | >30 | >15 | >12 | >13 |
| Area (mm$^2$) | 0.28 | 0.45 | 0.28 | 0.3 |

CCS= complementary conducting strip*: CPW=coplanar waveguide**

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