

Dynamic Multiplexer-Driven Level Shifter with High Common-Mode Transient Immunity and Sub-ns Transfer Delay for GaN Gate Drivers

Heechan Ahn, Jeongjin Roh

Department of Electronic Engineering, Hanyang University
E-mail : notch2@hanyang.ac.kr

Abstract - High-speed GaN gate drivers in half-bridge setups generate extreme voltage slew rates at the floating high-side node, compromising traditional level shifter reliability. Pulse-triggered designs face fundamental trade-offs between transfer delay reduction and common-mode transient immunity (CMTI) enhancement. This paper proposes a dynamic MUX-driven level shifter that senses internal latch nodes and high-side switch status to adaptively reconfigure current paths. During signal propagation, it enhances latch drive for accelerated transfer; during high-CMTI noise intervals, it maintains differential current balance to reject disturbances. Fabricated in 180 nm BCD process, the circuit achieves 886 ps delay and 200 V/ns CMTI, outperforming traditional PTAC designs for GaN applications.

Keywords—GaN, Level shifter, Common-mode transient immunity, Transfer delay, Gate driver

I. INTRODUCTION

In recent years, wide-bandgap (WBG) semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) have emerged as key candidates to replace traditional silicon-based power devices in power conversion systems. Their superior material properties, including low on-resistance, low junction capacitance, and high-temperature operation capability, enable significant performance improvements in both switching frequency and overall system efficiency [1], [2].

However, the high switching speed of these devices introduces a critical challenge in gate driver design: severe common-mode transient noise. As illustrated in the half-bridge topology in Fig. 1, GaN power devices are exclusively implemented as N-channel HEMTs due to material physics constraints, with no viable P-channel

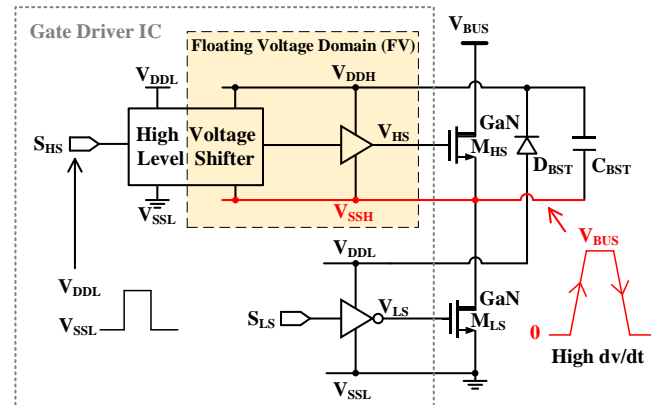


Fig. 1. Block diagram of Half bridge GaN Gate Driver

counterpart. Consequently, both the high-side (M_{HS}) and low-side (M_{LS}) switches must be N-channel devices. To turn on the high-side switch, its gate voltage must exceed its source voltage (V_{SSH}), which swings between 0 and V_{BUS} . This necessitates a floating gate drive supply, typically implemented with a bootstrap circuit and a high-voltage level shifter for signal transmission.

When the low-side switch (M_{LS}) turns off and the high-side switch (M_{HS}) turns on, V_{SSH} rises sharply from 0 to V_{BUS} , inducing a large dv/dt event. This noise can corrupt the logic state of the level shifter, resulting in erroneous outputs. Therefore, developing robust dv/dt mitigation techniques is essential for reliable gate driver operation [3], [4], [5].

$$V_{DDH} = V_{SSH} + C_{BST} \quad (1)$$

Fig. 2. (a) shows the schematic of a traditional PTAC level shifter consisting of low-voltage (LV) and floating-voltage (FV) domains. In the LV domain, a pulse generator converts the rising edge of the input signal into a short pulse to minimize power consumption. High-voltage MOSFETs $NLDM_1$ and $NLDM_4$ reside in the LV domain and serve as interface transistors between the LV and FV domains. NMOS and PMOS transistors in the FV domain are of equal size and operate as current mirrors, replicating the current signal from the $NLDMOS$ into the FV domain.

To analyze the rising edge operation, this period is defined as the signal phase. During the signal phase, the pulse generator applies a short pulse to the gate of $NLDM_1$. Assuming the initial state of the inverter latch is $V_X = \text{High}$ and $V_Y = \text{Low}$, PM_3 and NM_3 replicate the current from PM_1 , pulling down V_X and pulling up V_Y , respectively.

a. Corresponding author; jroh@hanyang.ac.kr

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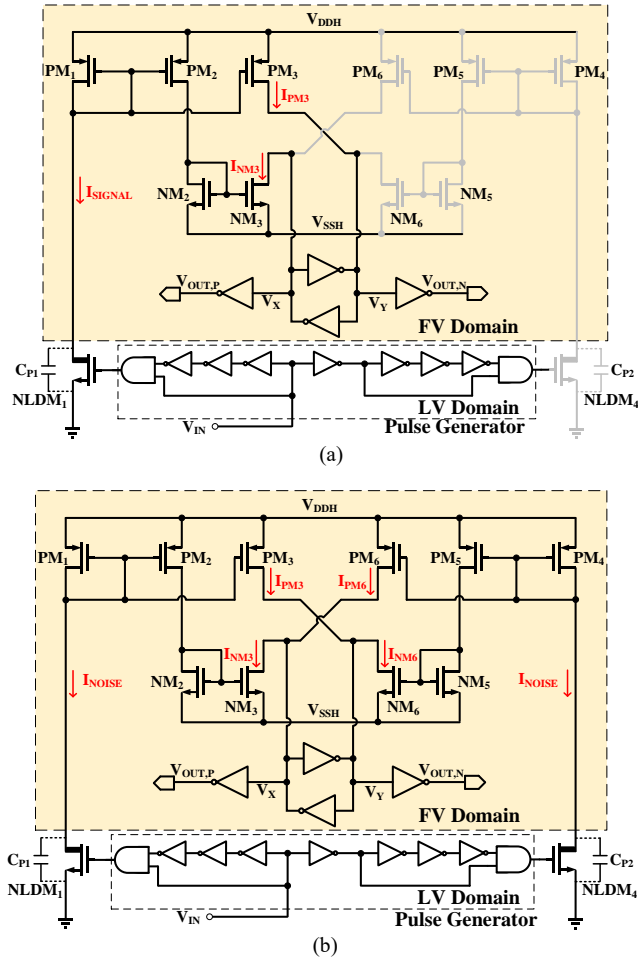


Fig. 2. Schematic of traditional high voltage level shifter under (a) signal phase (b) common-mode transient phase

Consequently, the output signal $V_{OUT,P}$ transitions from Low to High, and the high-side switch M_{HS} turns on completely, causing V_{SSH} to rise to V_{BUS} . The discharge speed of the V_X node can be improved by increasing the pull-down current I_{NM3} and decreasing the pull-up current of the latch. The increase in I_{NM3} is achieved by enlarging the size of $NLDM_1$ and increasing the current mirror ratio in the FV domain, while the pull-up current is reduced by decreasing the inverter size within the latch. Through transistor sizing, transfer delay can be minimized.

In the FV domain, V_{DDH} is supplied by an external bootstrap structure. When M_{HS} turns on and the floating ground (V_{SSH}) rises sharply, V_{DDH} also rises steeply. This simultaneously increases the drain voltage of $NLDM_1$ and $NLDM_4$, generating a noise current I_{NOISE} as shown in Fig. 2(b). This period is defined as the common-mode transient phase.

$$I_{NOISE} = C_{P1} \cdot \frac{dv}{dt} \quad (2)$$

If the circuit were perfectly symmetric, PM_3 , PM_6 , NM_3 , and NM_6 would replicate identical noise current I_{NOISE} , and due to the cross-coupling structure, this noise current would be canceled at the V_X and V_Y nodes with no adverse effect.

However, even symmetrically designed circuits suffer from inevitable process-induced mismatch in electrical performance. Mismatch between $NLDM_1$ and $NLDM_4$

generates slightly different noise currents I_{NOISE} during the common-mode transient phase. Transistors in the FV domain experience current mirror mismatch, resulting in incomplete cancellation of noise current, with residual current flowing into the V_X and V_Y nodes. Fortunately, if the latch is sufficiently large, the uncompensated noise current is absorbed by the latch. However, larger noise currents require larger latches to absorb the residual current.

Based on this analysis, to generate less I_{NOISE} during the common-mode transient phase, the sizes of $NLDM_1$ and $NLDM_4$ should be minimized; conversely, to maintain high CMTI, the latch must be enlarged [6], [7].

As shown in the foregoing analysis, the design requirements for achieving low transfer delay and high CMTI immunity are fundamentally contradictory.

Minimizing delay during the signal phase requires large coupling transistors and a small latch. Conversely, maximizing CMTI immunity during the common-mode transient phase demands small coupling transistors and a large latch. This inherent trade-off in traditional level shifter architectures makes it impossible to simultaneously optimize both performance metrics. Therefore, this work proposes a novel architecture designed to resolve this conflict.

II. DESIGN METHODOLOGY

A. Proposed Adaptive Control Level Shifter

To overcome the fundamental trade-off between transfer delay and CMTI immunity inherent in traditional PTAC level shifters, this paper proposes a MUX-driven adaptive level shifter as depicted in Fig. 3. The proposed circuit extends the traditional PTAC architecture by incorporating two 2:1 MUXes and critical current-control transistors in the floating-voltage (FV) domain. These additional circuits sense the state of internal node voltages (V_X , V_Y) and the high-side switch gate voltage (V_{HS}), and dynamically control circuit operation to adaptively optimize performance during both the signal and common-mode transient phases.

B. Signal phase operation

During the signal phase when input signal (V_{IN}) is applied, the circuit operates to minimize transfer delay. As shown in Fig. 3(a), when the rising edge of the input signal generates a signal current (I_{SIGNAL}) through the pulse generator, PM_3 , PM_4 , NM_3 , and NM_4 replicate the current from PM_1 . The initial state has $V_X = \text{High}$ and $V_Y = \text{Low}$. During the signal phase, V_{HS} remains Low, so the MUX outputs are $V_A = V_Y$ (High) and $V_B = V_X$ (Low). Consequently, only PM_5 and NM_5 among the four MUX-controlled MOSFETs (PM_5 , NM_5 , PM_{10} , NM_{10}) turn on, creating an additional current path to drive the inverter latch.

This acceleration effect enables the latch to transition much faster than in traditional structures, thereby reducing overall transfer delay.

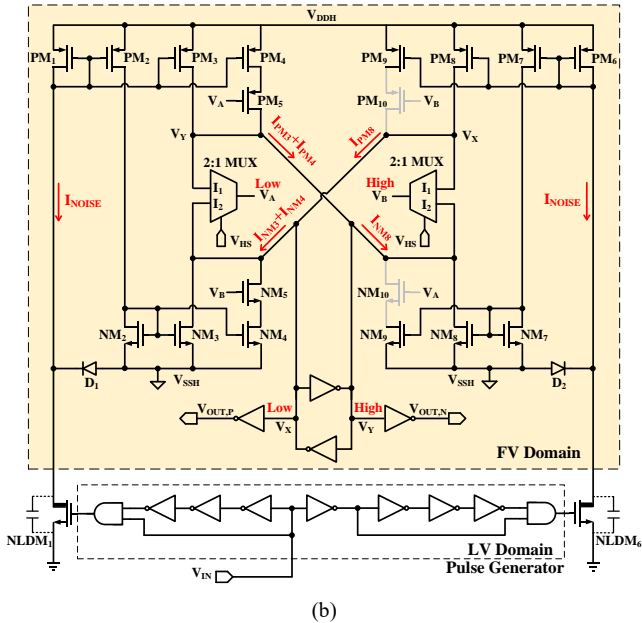
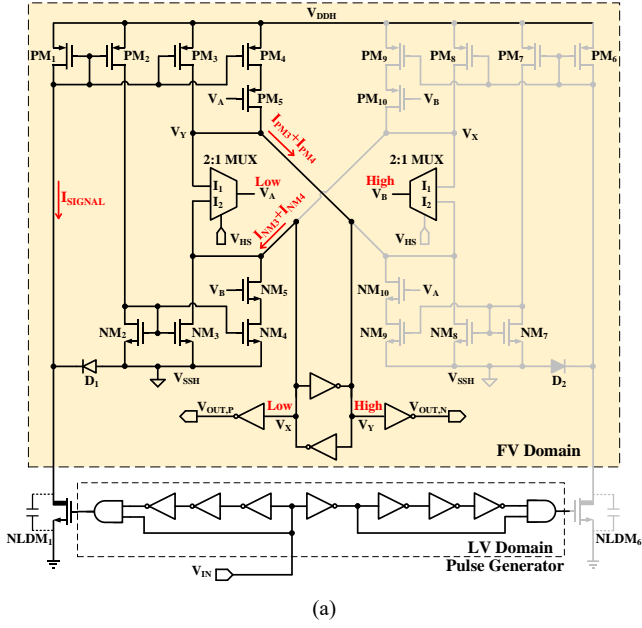


Fig. 3. Schematic of proposed high voltage level shifter under (a) signal phase (b) common-mode transient phase

C. Common-mode transient phase operation

Following the signal phase, when the level shifter's High output is delivered to the high-side switch M_{HS} , the half-bridge configuration causes V_{SSH} to rise rapidly, generating common-mode transient noise current I_{NOISE} . As shown in Fig. 3(b), during the common-mode transient phase, internal node voltages are $V_X = \text{Low}$ and $V_Y = \text{High}$, with the high-side GaN switch M_{HS} turned on, so $V_{HS} = \text{High}$. Consequently, the MUX outputs transition to $V_A = V_X$ and $V_B = V_Y$, maintaining Low and High values, respectively. The current flowing into the V_X and V_Y nodes is expressed by the following equation.

$$I_X = I_{PM8} - I_{NM3} - I_{NM4} \quad (3)$$

$$I_Y = I_{PM3} + I_{PM4} - I_{NM8} \quad (4)$$

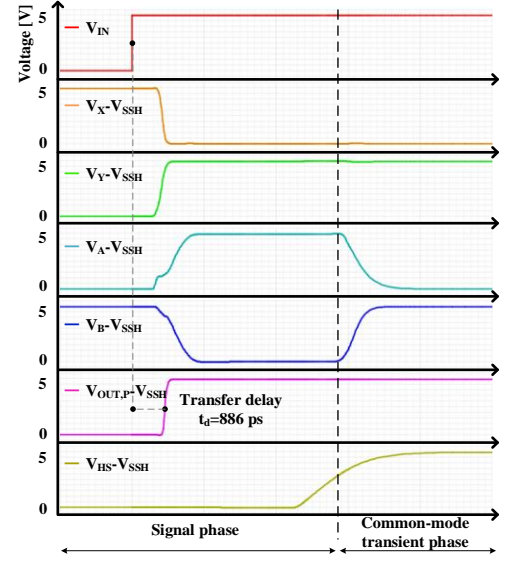


Fig. 4. Simulated transient waveforms of the proposed level shifter

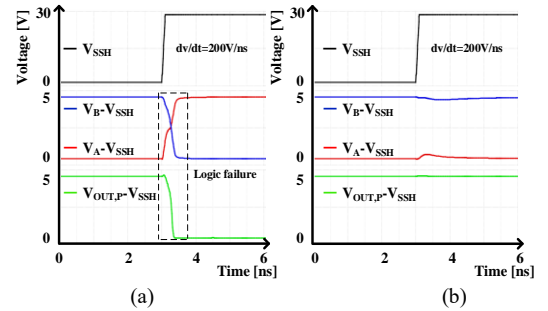


Fig. 5. Post-layout CMTI simulation results of (a) traditional level shifter (b) proposed level shifter

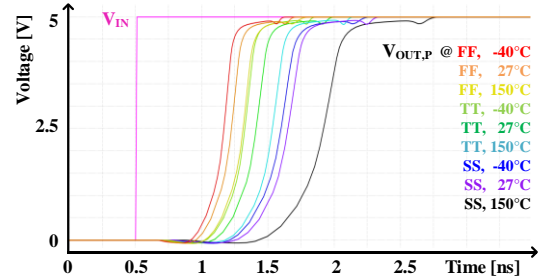


Fig. 6. Corner simulation result of proposed level shifter

Current flowing into the V_X and V_Y nodes is replicated by current mirrors reflecting I_{NOISE} . During the common-mode transient phase, the V_X node remains pulled down and the V_Y node remains pulled up, ensuring that no logic errors occur even under severe common-mode transient conditions.

Fig. 4 shows the transient simulation waveforms of the proposed level shifter. When the input PWM signal V_{IN} is applied, the MUX-driven controller pulls down the V_X node and pulls up the V_Y node during the signal phase using an additional current path incorporated to improve transfer delay. As V_{HS} subsequently rises and the circuit enters the common-mode transient phase, V_{SSH} increases and I_{NOISE} . However, the MUX-driven control cancels the malfunction-inducing noise current, maintaining V_X at a low level and V_Y

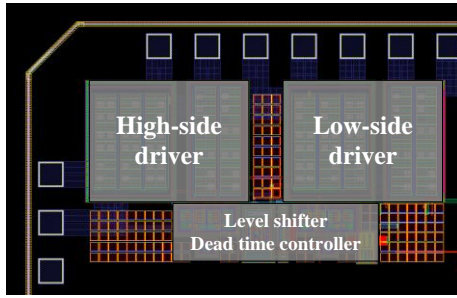


Fig. 7. Chip layout

at a high level. In this condition, the reported transfer delay of 886 ps represents the propagation delay from the 50% crossing of the low-voltage input PWM signal V_{IN} to the 50% crossing of the level-shifted output $V_{OUT,P}$ in the high-voltage domain. The delay was evaluated under the load condition of 1fF load capacitor.

Fig. 5 presents the Post-layout CMTI simulation results. The CMTI is evaluated by ramping the V_{SSH} voltage at 200 V/ns in simulation and then monitoring the output signal of the level shifter. The traditional structure fails to sufficiently suppress the I_{NOISE} current, resulting in logic errors during the common-mode transient phase. In contrast, as shown in Fig. 5 (b), the proposed structure successfully cancels I_{NOISE} , preventing unintended inverter latch switching and eliminating malfunction even under severe common-mode transient conditions. Consequently, the proposed architecture achieves high CMTI robustness by eliminating the possibility of logic failure caused by process-induced mismatch or asymmetric layout commonly observed in traditional structures.

Fig. 6 shows the corner-simulation results of the proposed level shifter under nine PVT conditions, including TT, FF, and SS corners at 27 °C, -40 °C, and 150 °C. In all simulated cases, the proposed level shifter maintained correct output transitions without logic failure. The propagation delay was 886 ps at the nominal TT corner and increased to 1.36 ns in the worst-case condition of SS at 150 °C, confirming robust operation against process and temperature variations.

Thus, the proposed Dynamic MUX-driven adaptive level shifter senses the circuit's internal state in real time and dynamically reconfigures current paths through the MUX, successfully resolving the trade-off between transfer delay and noise immunity—a fundamental limitation of existing technologies.

III. SIMULATION RESULTS AND DISCUSSIONS

The proposed level shifter and gate driver were implemented in DB Hitek's 180 nm 30 V BCDMOS process using 5 V SVT CMOS and 30 V LDMOS devices, as shown in Fig. 7. Post-layout simulation results show that the proposed circuit operates robustly under common-mode transients of up to 200 V/ns at V_{SSH} and achieves a transfer delay of 886 ps. In addition, under nominal conditions, the energy per transition, E_T , drawn from the FV-domain and LV-domain supplies was 70.97 pJ and 6.18 pJ, respectively, resulting in a total energy per transition of 77.15 pJ. Under the same conditions, the conventional PTAC structure exhibited logic malfunction at 200 V/ns, whereas the proposed MUX-driven structure maintained stable latch operation without spurious switching. These results demonstrate that the proposed

adaptive MUX control effectively mitigates the tradeoff between transfer delay and CMTI discussed in Section II. Furthermore, Table I compares the proposed structure with previously reported level shifters in terms of process, supply voltage, energy per transition, delay, and CMTI.

TABLE I. Comparison with Previous Work

	[8] (simulated)	[9] (simulated)	This work (simulated)
Process	0.5 μ m HVC MOS	0.35 μ m HVC MOS	180 nm BCDMOS
V_{DDH} [V]	25	10	30
E_T [pJ]	50	10	77.15
t_d [ps]	1700	1260	886
CMTI [V/ns]	-	200	200

IV. CONCLUSION

This paper presented a MUX-based adaptive level shifter to address the trade-off between transfer delay and CMTI in GaN gate drivers. By dynamically controlling current paths based on node voltages and phases, the design achieves fast response during the signal phase and strong noise immunity during the common-mode transient phase. Simulation results demonstrated improved delay and CMTI up to 200 V/ns compared to traditional designs. This work offers a practical solution for reliable high-speed gate drivers with wide-bandgap semiconductors.

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Heechan Ahn received the B.S. degree in electronic engineering from Hanyang University, Ansan, Korea, in 2024. He is currently working toward the M.S. degree in electronic engineering at Hanyang University, Ansan, Korea. His current research interests include integrated power managements ICs design and high-performance DC-DC Converter design.



Jeongjin Roh (Senior Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1990, the M.S. degree in electrical engineering from Pennsylvania State University, in 1998, and the Ph.D. degree in computer engineering from The University of Texas at Austin, in 2001. From 1990 to 1996, he was as a Senior Circuit Designer for mixed-signal products with Samsung Electronics, Giheung, South Korea.

From 2000 to 2001, he was a Senior Analog Designer for delta-sigma data converters with Intel Corporation, Austin, TX, USA. He joined the Faculty of Hanyang University, Ansan, South Korea, in 2001. His research interests include power management circuits and oversampled delta-sigma converters.