A GaN Gate Driver with Integrated Protection Circuit

Myeong-Ho Kim[1], Min-Sik Kim[2], Jong-Hun Kim[1], Seung-Ju Lee[1], Mun-Jung Cho[2], Eun-Jae Ko[1], Chan-Hyung Lee[3], Hyun-Tak Jeon[4] and Se-Un Shin[a]
[1]Graduate School of Semiconductor Technology, Pohang University of Science and Technology
[2, a]Department of Electrical Engineering, Pohang University of Science and Technology
[3]Department of Electronic Engineering, Sogang University
[4]School of Semiconductor Engineering, Chungbuk National University
E-mail: [1]mhkim98@postech.ac.kr

***Abstract* - This paper proposes a gate driver IC with integrated protection circuits to enhance reliability in high-speed power conversion systems. Although GaN power devices are widely adopted to achieve high power density and high conversion efficiency, their relatively immature technology and limited robustness necessitate the use of dedicated protection circuits.**

The proposed gate driver employs a separated output buffer structure to prevent short-circuit current during switching transitions and allows independent adjustment of turn-on and turn-off times through external gate resistors. In addition, a low-power hysteretic under voltage lock-out (UVLO) circuit is incorporated to ensure stable operation during power-up and power-down processes while minimizing static current consumption. To suppress false triggering caused by switching noise, a leading edge blanking technique is applied in the over-current protection (OCP) scheme. Furthermore, a fault reset time–based protection mechanism is introduced to mitigate fault chattering resulting from repetitive over-current events.

***Keywords*—Gate driver, protection circuit, UVLO, GaN**

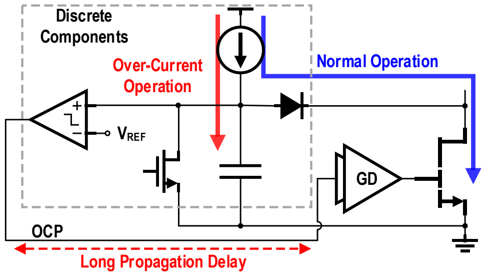

Fig. 1. Schematic of desaturation circuit

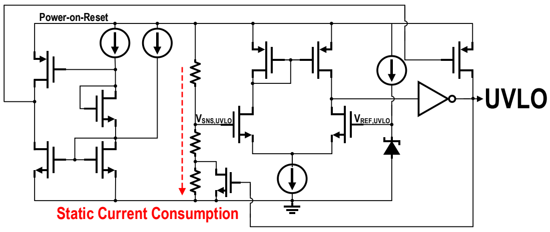

Fig. 2. Schematic of conventional UVLO circuit

I. INTRODUCTION

High power density and high conversion efficiency have become key design objectives in modern power electronic systems. To achieve these goals, technologies have evolved toward increasing switching frequency and minimizing the size of passive components, and GaN (gallium nitride) power devices have attracted significant attention as enabling devices. Owing to their low on-resistance and small parasitic capacitances, GaN devices enable much faster switching operation than conventional Si-based power devices, thereby achieving both reduced switching losses and system miniaturization [1], [2].

However, GaN power devices inherently suffer from reliability challenges. The high switching speed results in steep dv/dt and di/dt, which easily induce transient phenomena such as over-voltage, over-current, and ringing. In addition, GaN devices generally exhibit smaller allowable over-current margins and limited short-circuit capability compared to Si devices. As a result, delayed protection action can directly lead to device failure [3]–[5]. Therefore, fast and reliable protection circuits are indispensable in GaN-based power conversion systems.

For OCP, desaturation-based protection schemes have been widely adopted in previous studies [6]–[8]. However, as illustrated in Fig. 1, these approaches require additional high-voltage diodes to withstand the sensing voltage and rely on discrete components to process the protection signal and feed it back to the gate driver. Consequently, the overall circuit complexity is increased, and additional propagation delay is introduced before the power device is effectively shut down.

Meanwhile, under-voltage lockout (UVLO) circuits are also essential to protect the gate driver and power device under abnormal supply voltage conditions. As illustrated in Fig. 2, UVLO circuits in prior works were commonly implemented using resistor dividers to sense the supply voltage and to realize hysteresis characteristics [9]. However, such structures suffer from continuous static current consumption during normal operation. Increasing the

a. Corresponding author; seuns@postech.ac.kr

Manuscript Received Dec. 27, 2025, Revised May 30, 2026, Accepted Jun. 1, 2026

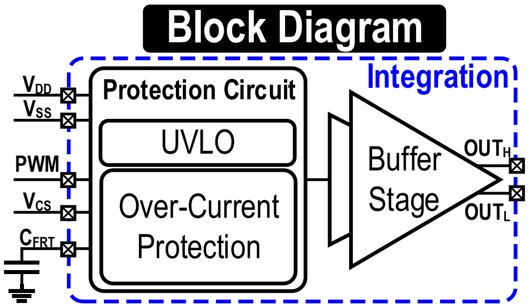

Fig. 3. Block Diagram of proposed gate driver IC

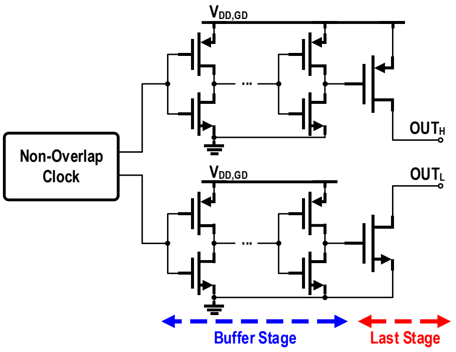

Fig. 4. Schematic of buffer stage

resistance values to reduce power consumption often results in larger chip area and associated design trade-offs.

To overcome these limitations, this work proposes a gate driver circuit with integrated protection functions. As shown in Fig. 3, the proposed design integrates the protection circuits—including a low-power hysteretic UVLO and OCP circuit—together with a separated output buffer stage within a single gate driver architecture to enhance switching reliability. The separated output buffer structure improves switching robustness, while the low-power hysteretic UVLO ensures stable operation during power-up and power-down transients. In addition, a leading-edge blanking technique is adopted to suppress false over-current triggering caused by switching noise, and a fault reset time–based protection mechanism is introduced to prevent repetitive over-current tripping. The feasibility and effectiveness of the proposed gate driver circuit have been validated through simulations using Cadence™ Virtuoso.

II. DESIGN METHODOLOGY

A. Buffer Stage

Fig. 4 shows the buffer stage architecture of the gate driver used in this work. Since the final output stage of the buffer directly drives the gate of the power device, the transistor widths are determined based on the required source and sink current capabilities. In general, the required sink capability during turn-off is larger than the source capability during turn-on, and thus the sink current is typically designed to be approximately 1.5–2 times larger than the source current. This asymmetric design is particularly important to rapidly discharge the gate charge during turn-off, thereby suppressing dv/dt-induced false turn-on caused by the Miller effect in high-speed switching environments. In addition, the carrier mobility of PMOS devices is approximately 2–3 times lower than that of NMOS devices. Considering these characteristics, the width ratio of the final output stage is set to $(W/L)_P:(W/L)_N = 2.5:2$ in this design.

As shown in the schematic, the final output stage is not implemented as a conventional CMOS buffer with the drains of the PMOS and NMOS tied together; instead, the two devices are separated. This is because very large transient currents can flow when the final stage drives the gate of the power device. If a conventional inverter structure were used, simultaneous conduction of the PMOS and NMOS during switching transitions could result in large short-circuit currents, leading to increased power consumption and degraded reliability.

Furthermore, by adopting a separated output stage structure, the turn-on and turn-off times can be independently adjusted using external gate resistors. This provides additional design flexibility at the system level, allowing optimization of switching losses, EMI, and ringing. As illustrated in Fig. 4, when an input signal is applied, a non-overlap clock circuit generates complementary control signals for the PMOS and NMOS, thereby preventing short-circuit current and ensuring stable operation of the buffer stage.

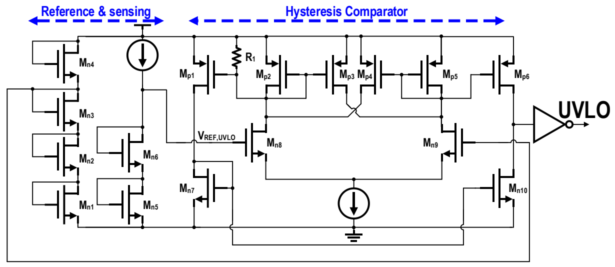

Fig. 5. Schematic of UVLO circuit

B. UVLO

Fig. 5 shows the UVLO circuit employed in this work. The reference voltage is generated using diode-connected NMOS transistors connected in series, while the supply voltage is sensed using a MOS-based resistive sensing network instead of a conventional passive resistor divider. Unlike traditional UVLO implementations that rely on resistor networks for both voltage sensing and hysteresis generation—resulting in continuous static current consumption—the proposed design adopts a hysteresis comparator structure to realize the hysteresis characteristic with minimal additional static current. This approach effectively reduces power consumption while ensuring stable UVLO operation.

Hysteresis is required in UVLO circuits to prevent repetitive toggling of the comparator output when the supply voltage slowly rises near the threshold or fluctuates due to noise. Such chattering behavior can lead to unstable operation of the gate driver and consequently degrade the reliability of the power device. Therefore, providing a clear separation between the turn-on and turn-off threshold

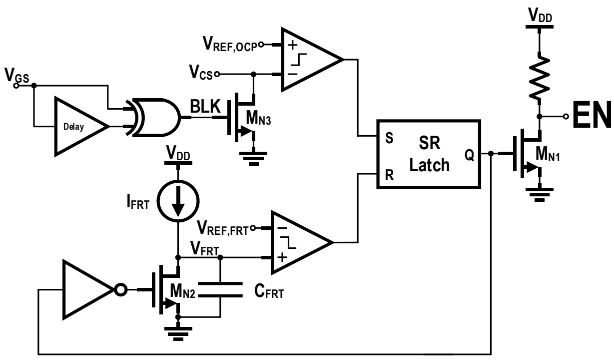

Fig. 6. Schematic of OCP circuit

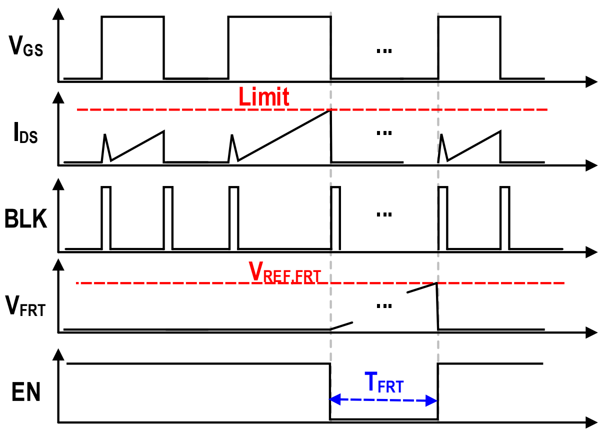

Fig. 7. Timing diagram of protection circuit

voltages through hysteresis is essential to ensure stable UVLO operation.

Meanwhile, the hysteresis comparator used in this design incorporates a feature that differentiates it from conventional structures. As shown in Fig. 5, a resistor is inserted at the gate of the PMOS transistor located on the left side of the circuit, so that the initial operating state of the comparator is well defined even when the supply voltage is very low. During the initial power-up phase, internal nodes may remain floating, which can prevent proper comparator operation; in this case, the inserted resistor initializes the gate voltage to a defined level.

As a result, the UVLO output remains reliably disabled until the supply voltage rises sufficiently, ensuring that the gate signal is stably blocked even in the low-voltage region. Consequently, the proposed UVLO circuit guarantees predictable and stable operation throughout the entire power-up and power-down processes.

C. Over-Current Protection

Fig. 6 shows the OCP circuit employed in this work. A current-sensing scheme is used for over-current detection; however, a major challenge arises from the large switching noise generated during the turn-on and turn-off transitions of the power device. Such noise can cause the comparator to malfunction and result in false triggering, even in the absence of a true over-current condition.

To mitigate this issue, a leading edge blanking time is introduced in the proposed design. As shown in Fig. 6, a leading edge blanking interval of approximately 200 ns is applied during the switching transitions of the power device based on the gate signal. During this interval, an nMOS switch is activated to block the input of the comparator, thereby effectively suppressing false triggering caused by switching noise.

Over-current conditions are typically caused by output short circuits or inductor saturation. When an over-current event forces the power device to turn off and the device is immediately turned on again in the next PWM cycle, switching may occur before the current has sufficiently decayed. This can lead to repeated detection of the same over-current condition, resulting in fault chattering. Such repetitive behavior imposes cumulative thermal stress on both the power device and the gate driver, significantly degrading system reliability.

To address this problem, a fault reset time is incorporated in the proposed OCP scheme. When an over-current is detected, the input signal is blocked to turn off the power device, and reactivation is allowed only after a predefined fault reset time has elapsed.

Fig. 7 shows the timing diagram of the protection circuit. When an over-current event occurs, the comparator output is driven high, activating the SET input of the SR latch. As a result, M_{N1} is turned on, pulling the EN signal low and disabling the gate drive signal. Simultaneously, the output of the SR latch turns off M_{N2} through an inverter, allowing the current I_{FRT} to charge the capacitor C_{FRT}. When the voltage across C_{FRT} exceeds the reference voltage $V_{REF,FRT}$, the comparator output transitions high, resetting the SR latch. Consequently, the EN signal returns high and normal operation is resumed.

The fault reset time (FRT) is defined as

$$T_{FRT} = \frac{C_{FRT} \cdot V_{FRT}}{I_{FRT}} \quad (1)$$

By selecting the external capacitor C_{FRT}, the fault reset time can be programmably adjusted, providing flexibility to tailor the protection duration according to system requirements.

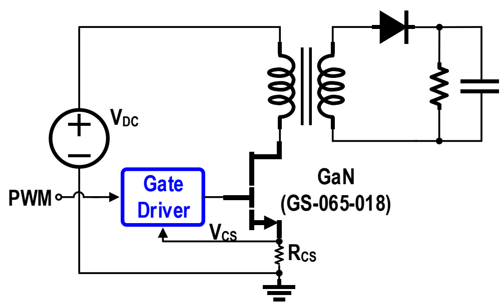

Fig. 8. Flyback converter for simulation setup

TABLE I. Comparison Table with Prior Works

	Protection /UVLO Method	UVLO Static Power / Current	OCP Response Time	Propagation Delay
[6] Y. Wu et al., TPEL 2024	Gate-voltage-controlled short-circuit current limiting	N/A	90 ns	Not reported
[7] Z. Wang et al., TIE 2014	SSCB, DESAT, and dynamic fault-current evaluation protection	N/A	100 ns	40 ns
[8] D.-P. Sadik et al., TIE 2016	Integrated short-circuit protection driver	N/A	180 ns	180 ns
[9] K. Song et al., APEC 2017	Hysteretic UVLO with POR for HVIC	411 μW @ V_{DD} = 15 V	N/A	N/A
This Work	Proposed GaN gate driver IC with hysteretic UVLO and OCP	143 μW @ V_{DD} = 6.5 V	30 ns	16 ns

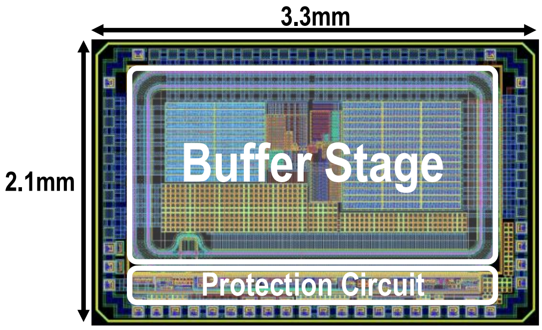

Fig. 9. Layout design of the proposed gate driver

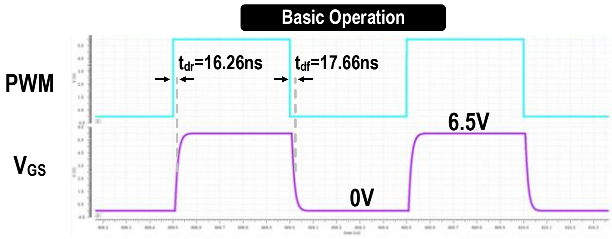

Fig. 10. Simulation results of basic operation

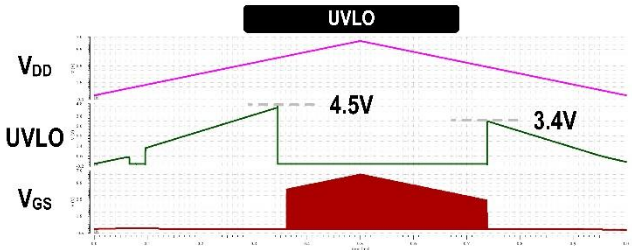

Fig. 11. Simulation results of UVLO

D. Performance Comparison

To quantitatively evaluate the proposed gate driver IC, a comparison with previously reported protection and UVLO circuits is summarized in Table I. Key metrics, including UVLO static power consumption, OCP response time, and propagation delay, are compared.

As shown in Table I, the proposed design achieves lower UVLO static power consumption (143 μW @ 6.5 V), a fast OCP response time of 30 ns, and a short propagation delay of 16 ns. These results demonstrate that the proposed gate driver effectively combines low-power operation and fast protection capability for high-speed GaN switching applications.

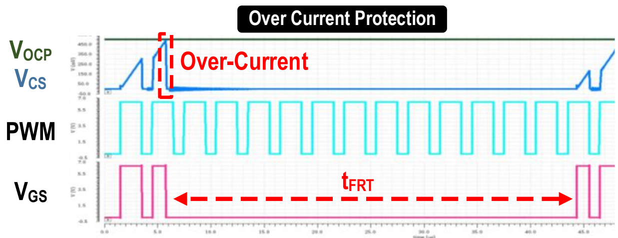

Fig. 12. Simulation results of OCP

III. RESULTS AND DISCUSSIONS

To verify the proposed design, simulations were performed using a flyback converter configured as shown in Fig. 8. The input voltage was set to 380 V, and the transformer turn ratio was configured to 5:1. A GaN power device (GS-065-018) was used as the switching device. The current was sensed by inserting a shunt resistor at the source side of the GaN device.

The current was sensed by inserting a shunt resistor at the source side of the GaN device. In this work, the value of the current sensing resistor (R_{CS}) was selected as 40 mΩ. Since commercially available 650 V GaN power devices typically exhibit an on-resistance of approximately 100–200 mΩ, the selected R_{CS} value is sufficiently smaller than the intrinsic on-resistance of the power device. Therefore, the additional conduction loss caused by R_{CS} is expected to have a limited impact on the overall system efficiency while enabling reliable over-current detection.

Fig. 9 shows the layout of the IC designed using Cadence Virtuoso and the DB 350nm BCD process design kit (PDK). Based on this layout, post-simulation was performed considering parasitic components within the chip.

As shown in Fig. 10, GaN power devices generally require a lower turn-on voltage compared to Si devices. In this work, the GS-065-018 device was driven with a gate voltage of 6.5 V. Under this condition, the rising propagation delay was measured to be 16.26 ns, while the falling propagation delay was 17.66 ns based on simulation results.

As shown in Fig. 11, the proposed UVLO exhibits hysteresis behavior during both supply voltage ramp-up and ramp-down conditions. The UVLO is deactivated when the supply voltage reaches 4.5 V during power-up, after which the output signal is properly enabled. During power-down, the UVLO is activated again when the supply voltage decreases to 3.4 V, thereby providing a hysteresis window that prevents repetitive output toggling (chattering) near the threshold voltage. Consequently, stable and reliable UVLO operation is ensured under slowly varying or noisy supply conditions.

As shown in Fig. 12, an over-current condition is detected in the flyback converter during the second turn-on of the GaN switch. Upon detection, the switch is immediately turned off, and the input PWM signal is blocked. After the user-defined FRT has elapsed and the current has sufficiently decayed to a stable and safe level, the input PWM signal is again forwarded to the gate driver output, demonstrating proper and controlled recovery operation.

IV. CONCLUSION

In this paper, a gate driver IC with integrated protection circuits was proposed to improve the reliability of high-speed power conversion systems employing GaN power devices. To address the reliability challenges arising from fast switching operation, the proposed design incorporates a separated output buffer structure, a low-power hysteretic UVLO circuit, and a robust OCP scheme.

The separated output buffer prevents short-circuit current during switching transitions and allows independent control of turn-on and turn-off behavior. In addition, the proposed UVLO circuit ensures stable operation during power-up and power-down while minimizing static current consumption. For OCP, leading edge blanking is employed to suppress false triggering caused by switching noise, and a fault reset time–based mechanism is introduced to prevent repetitive fault chattering and excessive thermal stress.

The effectiveness of the proposed gate driver was verified through simulations using a flyback converter configuration, demonstrating stable operation under normal and fault conditions. The proposed design provides a reliable and practical solution for gate driving and protection of fast-switching power devices. Future work will focus on experimental validation to further demonstrate the performance of the proposed architecture.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center(IDEC), Korea. This paper was supported by Korea Instituter Advancement of Technology(KIAT) grant funded by the Korea Government(MOTIE) (RS-2024-00401466, HRD Program for Industrial Innovation); in part by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIT) (RS-2025-23323980); in part by the Technology Innovation Program (RS-2022-00154983, Development of Low-Power Sensors and Self-Charging Power Sources for Self-Sustainable Wireless Sensor Platforms) funded By the Ministry of Trade, industry & Energy(MI, Korea); in part by Glocal 30 University Project

REFERENCES

[1] A. A. Kerai, S. J. Shah, L. Maheshwari, K. A. Khan, I. Makda, H. Qamar, A. Usman, “Comparative performance analysis of GaN FET and silicon MOSFET in closed-loop synchronous buck converter for electric vehicle auxiliary power Module,” *Proc. of IEEE Workshop on Control and Modeling for Power Electronics*, pp. 1–5, Jun. 2024.

[2] S. Yerra, H. S. Krishnamoorthy and G. S. Kulothungan, “Simplified gate driving strategy for GaN-Based multi-level buck converters operating at MHz switching frequencies, *Proc. of IEEE Applied Power Electronics Conference and Exposition*, pp. 735–740, Jun. 2021.

[3] H. Li, X. Li, X. Wang, L. Liu, S. Bala, J. Wang, “E-mode GaN HEMT short circuit robustness and degradation,” *in Proc. IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1995 - 2002.

[4] M. Fernandez et al, “Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs,” in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9012 - 9022, Nov. 2017.

[5] P. Williford, F. Wang, S. Bala, J. Xu, “Short Circuit Study of 600 V GaN GITs,” in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Raleigh, NC, USA, USA, 2019.

[6] Y. Wu, C. Li, J. Liu, and Z. Zheng, “An ultrafast and low-invasive short-circuit current limiting method by gate voltage control for SiC MOSFETs with kelvin-source,” *IEEE Trans. Power Electron.*, vol. 39, no. 12, pp. 15696–15708, Dec. 2024.

[7] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, “Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5570–5581, Oct. 2014.

[8] D.-P. Sadik, “Short-circuit protection circuits for silicon-carbide power transistors,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 1995–2004, Apr. 2016.

[9] K. Song, W. Oh, and J. Choi, “A UVLO with zero static power consumption power-on reset circuit in HVIC,” *IEEE Applied Power Electronics Conference and Exposition*, pp. 1085–1089, March 2017.

RS-2024-00401466, HRD Program for Industrial Innovation
This paper was supported by Korea Instituter Advancement of Technology(KIAT) grant funded by the Korea Government(MOTIE)
This research was supported by the Regional Innovation System & Education(RISE) program through the Gyeongbuk RISE CENTER, funded by the Ministry of Education(MOE) and the Gyeongsangbuk-do, Republic of Korea.(2026-RISE-15-118)
Glocal 30 University Project
This work was supported by the Industrial Strategic

Technology Development Program funded by the Ministry of Trade Industry & Energy(MOTIE, Korea) under Grant RS-2024-00420538.
This work was supported by Korea Planning & Evaluation Institute(KEIT) grant funded by the Korea Government(MOTIE)(RS-2024-00404313, Development of a 650 V GaN-based power converter single IC for mobile device charging adapter)

Myeong-Ho Kim received the B.S. degree in electronics engineering from Kyungpook National University, Daegu, South Korea, in 2024. He is currently pursuing the integrated master's and Ph.D. degrees with the Graduate School of Semiconductor Technology, Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

His current research interests include analog-integrated circuit design and power management IC design.

Min-Sik Kim received the B.S. degree in electronics engineering from Kyungpook National University, Daegu, South Korea, in 2023. He is currently pursuing the integrated master's and Ph.D. degrees with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

His current research interests include analog-integrated circuit design and power management IC design.

Jong-Hun Kim received the B.S. degree (summa cum laude) in electronics engineering from Pukyong National University (PKNU), Busan, South Korea, in 2022, and the M.S. degree in electrical engineering from Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2024. He is currently pursuing the Ph.D. degree with the graduate school of semiconductor technology, Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

His research interests include power management integrated circuits, power electronics, wireless power transfer systems, gate drivers, and power amplifiers.

Seung-Ju Lee received the B.S. degree in display engineering from Dankook University, Cheonan, South Korea, in 2021, and the M.S. degree from the Department of Electrical Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2024. He is currently pursuing the Ph.D. degree with the Graduate School of Semiconductor Technology, Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

His research interests include analog-integrated circuit designs, such as power management ICs, linear regulators, switched capacitor/inductive converters, and hybrid converter topologies.

Mun-Jung Cho received the B.S. degree in Electrical Engineering from Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2023. She is currently pursuing an integrated M.S./Ph.D. degree in Electrical Engineering at Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

Her research interests include analog integrated circuit design such as power management ICs, switched capacitor/inductive converters, isolated and multiple-output converters, hybrid converters, and RF energy harvesting interfaces.

Eun-Jae Ko received the B.S. degree in electronics and electrical engineering from Ewha Womans University, Seoul, Korea. She is currently pursuing the integrated M.S. and Ph.D. degrees at the Graduate School of Semiconductor Technology, Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

Her research interests include analog integrated circuit design and power management integrated circuits.

Chanhyung Lee received the B.S. degree in electronic engineering from Sogang University, Seoul, South Korea, in 2026. He is currently pursuing the integrated master's and Ph.D. degrees with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, South Korea.

Hyuntak Jeon received the B.S. degree in electronic and electrical engineering from Hongik University, Seoul, South Korea, in 2015, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2017 and 2021, respectively.

He was a Senior Researcher with the Agency for Defense Development (ADD), Daejeon, from 2021 to 2022. In 2022, he joined the School of Semiconductor Engineering, Chungbuk National University, Cheongju, South Korea, where he is currently an Assistant Professor. His research interests include mixed-signal and power management IC design.

Se-Un Shin received the B.S. degree in electronics engineering from Kyungpook National University, Daegu, South Korea, in 2013, and the integrated master's and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2018.

From 2018 to 2019, he was a Postdoctoral Associate with the University of Michigan, Ann Arbor, MI, USA, where he was involved in the development of low-power analog circuit design and automation. From 2019 to 2020, he served as a Faculty Member for the School of Electronics and Electrical Engineering, Dankook University, Cheonan, South Korea. From 2021 to 2023, he held a Faculty Position with the Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea. Since 2023, he is an Assistant Professor with the Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang, South Korea. His current research interests include analog-integrated circuit design and power management IC design, energy harvesting, battery charger, wireless power transfer systems, switched capacitor/inductive converters, and hybrid converter topology.