A 0.0031-mm^2 6-Bit 400-MS/s Charge-Injection DAC Based Loop Unrolled Asynchronous Successive Approximation Register ADC

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Abstract - **This paper presents a 6-bit charge-injection DAC based loop unrolled SAR (ci-LU SAR) ADC targeting high-speed and area-efficient column readout for highly parallel computing-in-memory (CIM) macros. To reduce the dominant DAC area overhead in prior LU SAR ADCs, the proposed architecture replaces the conventional CDAC with a charge-injection DAC (ciDAC) while preserving the sequential domino-style comparator operation of LU SAR conversion. A self-calibrating offset-cancellation scheme is applied to each comparator to mitigate comparator offset mismatch, which is critical in multi-comparator LU architectures. Implemented in 65-nm CMOS, the ADC achieves 400 MS/s with a 1.0-V supply while occupying 0.003157 mm^2 core area, where the DAC network accounts for only 11.3% of the core area. Post-layout simulations show 35.73-dB SNDR and 47.86-dB SFDR at Nyquist input, with 3.36-mW power consumption, 168-fJ/conversion-step Walden FoM, and 5.64-bit ENOB.**

Keywords— **Charge-injection DAC, loop-unrolled, offset calibration, successive approximation register (SAR)**

I. INTRODUCTION

As Deep Neural Network (DNN) accelerators are becoming increasingly integrated into diverse edge devices, the demand for Computing-In-Memory (CIM) architectures is on the rise to address the memory wall problem. In particular, parallel analog computing within the memory macro enables the energy-efficient execution of a massive amount of Matrix-Vector Multiplication (MVM), achieving high throughput.

Recent CIM macros have further enhanced the high computing parallelism of MVM operations by employing a method where all the bit cells in a column can be accessed simultaneously for computation [1], [2]. At the same time, as the number of columns scales to hundreds, the silicon area per CIM array becomes a primary design issue. In these architectures, the readout circuitry-specifically the column-parallel ADCs-plays a critical role in determining the overall system performance. Since the analog multiply-accumulate (MAC) results from each column must be converted into the digital domain for subsequent processing, the speed and area of these column ADCs directly dictate the throughput and computing density of the entire CIM macro [3], [4]. Consequently, it is crucial to design the column ADC for both high operational speed and area efficiency to maximize computing density.

Low-precision CIMs use a single-slope (SS) ADC with low resolution [5], which provides inherent uniformity but is energy-inefficient due to its linear counting operation [6]. This energy-inefficiency is exacerbated at higher resolutions. Therefore, the SS ADC is not suitable as a column ADC for recent large-scale CIM arrays that target high computing parallelism [2]. The successive approximation (SAR) ADC architecture, based on a serial binary search, is considered a suitable option for recent CIM arrays due to its superior energy efficiency and small area [7], [8]. However, the SAR ADC is inherently limited in speed because its conversion is performed through a serial binary-search procedure, requiring multiple clock cycles per output code. To further increase the MVM throughput in highly parallel CIM macros, flash ADCs have been adopted to provide a much faster column readout [9], [10]. This speed advantage, however, comes with a severe scaling penalty: the power consumption and area of a flash ADC increase exponentially with resolution, making high-bit flash implementations impractical for dense CIM arrays. For example, an N-bit flash ADC requires 2N-1 comparators, directly translating into large area and power overhead.

For balanced performance in the medium resolution range, a Loop-Unrolled SAR (LU SAR) ADC can be a meaningful alternative, as it can eliminate the reset time of the comparator, thereby reducing the logic delay from the critical path while having N comparators for an N-bit LU SAR ADC [11]. However, this ADC still employ multiple comparators to improve speed, which may lead to a relatively large area overhead. In LU SAR ADCs, the DAC network occupies a significant portion of the area comparable to the comparators, and all prior works employ

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capacitive DACs (CDACs) as their core DAC structure.

To preserve the structural advantages of the LU SAR architecture that enable high-speed operation while mitigating the area overhead, we propose a charge-injection DAC based LU SAR (ci-LU SAR) ADC structure. In this design, the CDAC-which typically constitutes the second largest area contributor in prior LU SAR ADCs-is replaced by a highly area-efficient charge-injection DAC (ciDAC). The 0.0031-mm², 6-bit, 400-MS/s ci-LU SAR ADC enables significantly higher area efficiency than any other 6-bit LU SAR ADC, while meeting the resolution and signal bandwidth requirements for a column ADC in CIM applications [2].

The organization of this paper is as follows. Section II presents the area-saving aspects of a ciDAC and introduces the proposed SAR ADC structure. Section III explains how the ciDAC merges into the LU SAR and how the offset calibration unit is performed in each comparator. And also, we introduce a new layout implementation of the ciDAC. Section IV provides simulation results, followed by the conclusions in Section V.

II. ARCHITECTURE OF THE PROPOSED ADC

A. Leveraging the Area Advantages of a Charge-Injection DAC

In the ciSAR ADC architecture [12], the differential input signal is first sampled onto a pair of sampling capacitors (C_S), as shown in Fig. 1(a). Once the sampling is complete, the sign of the sampled input is evaluated to determine the MSB decision. Subsequently, the SAR conversion proceeds using a set-and-down switching scheme [13], where the DAC voltage is adjusted by injecting fixed charge packets. The ciSAR utilizes charge-injection cells (CICs) to inject specific quanta of charge into the sampling nodes. During the binary search process, these CICs transfer charge from a reservoir node-typically implemented by the parasitic capacitance of NMOS transistors as depicted in Fig. 1(b)-to the C_S. The charge transfer is governed by a local timing logic: when both the transfer and enable signals are high, transistors M1 and M2 are activated to inject charge into the C_S, thereby updating the DAC output voltage for the next bit trial.

DAC area saving of the ciDAC can be accomplished by: (1) each CIC is composed of few transistors and (2) reusability of CICs [12]. In a CDAC, each capacitor is formed using metal layers, and due to capacitor matching requirements, it is difficult to scale down the unit capacitor size. In contrast, a CIC uses a small number of transistors. In addition, CICs can be reused multiple times in a SAR conversion. By reusing the CICs for the subsequent transfer cycles, the DAC area of charge-injection SAR (ciSAR) ADC can be reduced at least by half or even more. However, a CDAC based SAR ADC requires dedicated capacitors for each step, and these scale up to a binary fashion as the resolution increases. Therefore, the area overhead problem of LU SAR ADCs can be improved further if we replace the area-consuming CDAC with a ciDAC that demonstrates superior area efficiency, which sets the motivation of the proposed ADC structure in the following paragraph.

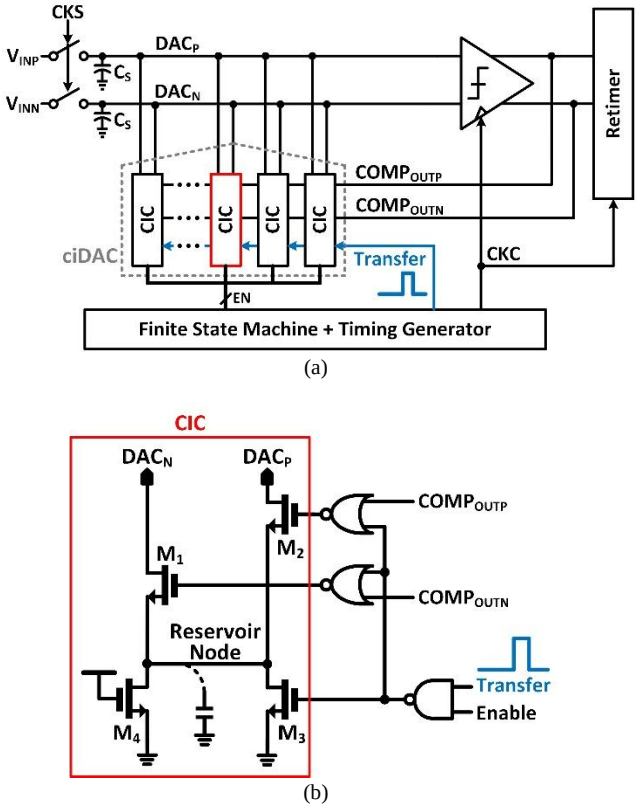


Fig. 1. Conventional ciSAR ADC structure (a)block diagram (b)and its charge-injection cell(CIC)

B. Proposed Charge-Injection DAC based Loop Unrolled SAR ADC

In order to address the area overhead issue in LU SAR ADCs, this work presents a design that substitutes the area-consuming CDAC with an alternative architecture, while preserving the sequential operation of domino-style comparators-the key mechanism enabling high-speed conversion in LU SAR schemes. The architecture of the proposed 6-bit SAR ADC is shown in Fig. 2. The ADC consists of bootstrapped sampling switches, sampling capacitors (C_S), 6 comparators each with an offset calibration unit, transfer pulse and comparator clock (CKC) generators, and 16 charge-injection cells (CICs).

Fig. 3 shows the timing diagram of the proposed ci-LU SAR ADC. After the sample/hold operation by the bootstrapped switches, the comparators operate sequentially from the first comparator to the final comparator. During each bit-conversion step, once the bit comparison is completed, the DAC switching is triggered by the transfer pulse. To meet the goal of the proposed ADC, this work combines (1) the LU-SAR characteristic that feeds the comparison result directly into the DAC input to maintain speed and (2) the reusability of the ciDAC to improve area efficiency.

Specifically, $D_{OUTP,N}[5]$ is distributed to all 16 CICs, while each of $D_{OUTP,N}[4:0]$ is routed to its corresponding CIC[4:0]. Each CIC then selects the appropriate $D_{OUTP,N}$ value-either

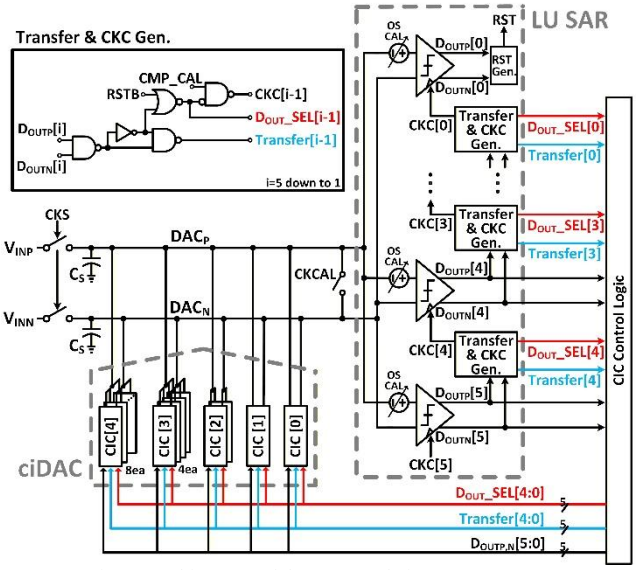


Fig. 2. Architecture of the proposed ci-LU SAR ADC

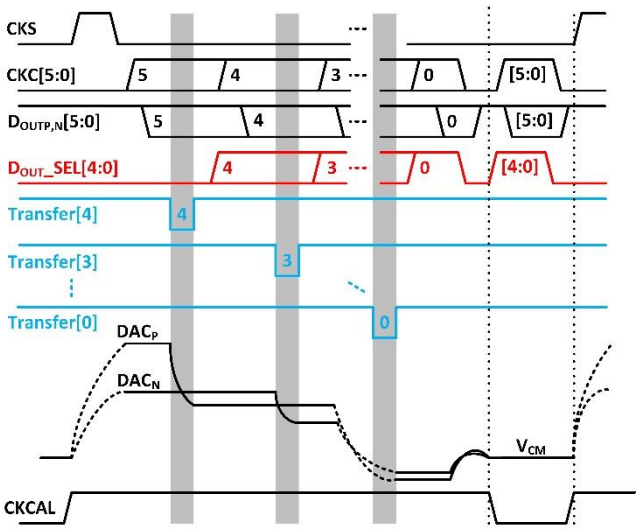


Fig. 3. Timing diagram and switching scheme of the proposed ci-LU SAR ADC

$D_{OUTP,N}[5]$ or its local $D_{OUTP,N}[4:0]$, depending on the conversion step-so that the DAC switching occurs accordingly. As shown in Fig. 4, each CIC receives both $D_{OUTP,N}[5]$ and $D_{OUTP,N}[4:0]$ through a MUX, and the D_{OUT}_SEL[i] signal selects which input is applied to the CIC in the current conversion step. The D_{OUT}_SEL[i] signal is aligned with the waveform used to clock the comparators: when D_{OUT}_SEL[4:0] are all low, all CIC[4:0] perform most-significant-bit (MSB) DAC switching according to $D_{OUTP,N}[5]$ value, and when a given D_{OUT}_SEL[i] is high, CIC[i] performs subsequent DAC switching according to its corresponding $D_{OUTP,N}[i]$ value. Therefore, every one of CICs participate in two DAC-switching events across the conversion, thereby realizing the reuse function of the ciDAC.

After all bit conversions are completed, the reset signal (RST), generated by the final comparator, precharges all comparators to prepare them for the offset-calibration mode. During the calibration phase, the comparator input nodes (DAC_P and DAC_N) are shorted to the common-mode voltage (V_{CM}).

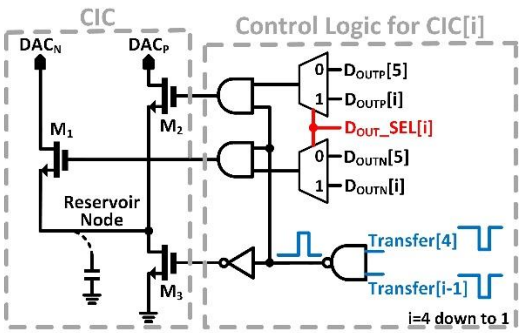


Fig.4. Proposed CIC and its control logic

TABLE I. Transistor Size Table of CIC

Transistor name	Transistor size W/L [nm/nm]	Device Type
M_1	400/190	High-V_{th} NMOS
M_2	400/190	High-V_{th} NMOS
M_3	380/310	High-V_{th} NMOS

III. HARDWARE IMPLEMENTATION

A. Charge-Injection Cell and its Control Logic

The details of CIC structure used in the proposed ci-LU SAR ADC is shown in Fig. 4, with the specific device dimensions in TABLE I. Since the proposed ADC relies on charge injection quantization rather than capacitor ratio matching, ensuring that all CICs inject an identical charge quantum when enabled is of paramount importance, even in the presence of severe device mismatch and PVT variations. To achieve this robustness, several design techniques have been implemented. First, high threshold-voltage NMOS devices are strategically employed for $M_{1\text{-}3}$. Furthermore, their channel lengths are intentionally chosen to be significantly longer than the minimum process node feature size. This allocation effectively mitigates the channel-length modulation effect and drastically suppresses the circuit's sensitivity to threshold-voltage mismatches. Second, a separate low-voltage supply is routed exclusively to the local AND gates that modulate the gate drives of M_1 and M_2. This targeted power routing successfully scales down the gate-source voltage, thereby lowering the overdrive voltage of the switching devices to ensure a well-controlled charge injection mechanism [14].

Through these combined structural optimizations, a reliable operating region is secured where the CIC consistently delivers a uniform charge quantum regardless of the DAC output level. To verify the operational integrity across all PVT corners, the simulated amount of charge injection as a function of the DAC node voltage is evaluated in Fig. 5. As demonstrated by the robust corner simulation curves, the CIC enters a flat, stable saturation region when the node voltage exceeds 0.5V. To ensure that the circuit never enters the highly non-linear triode region under any PVT variations, the ADC input common-mode voltage is set close to the supply voltage V_{DD} [12]. Concurrently, the ADC input range is set to 0.3 V_{PP}, ensuring that the entire signal trajectory safely resides within the flat CIC saturation range in Fig. 5.

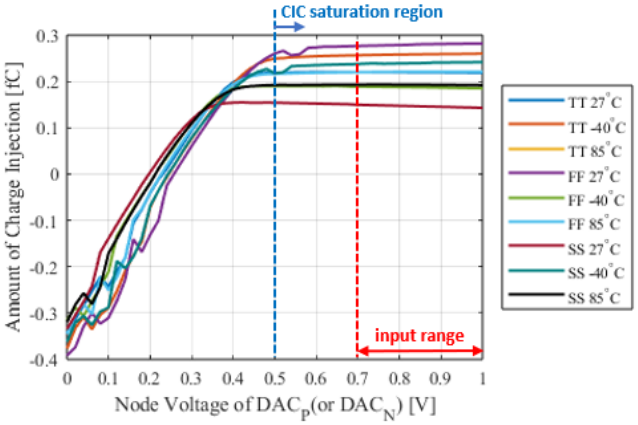


Fig.5. Simulated charge injection characteristics of the proposed CIC under different PVT corners

TABLE II. Monte Carlo Simulations Results of the Unit Voltage Drop (ΔV_{CIC}) by CIC against PVT Variations

PVT Corner		Mean (μ)	Sigma (σ)	coefficient of variation ($\frac{\mu}{\sigma} \times 100$)
TT	27°C	4.792 mV	104.3 uV	2.17%
	-40°C	4.638 mV	120.8 uV	2.60%
	85°C	4.941 mV	96.4 uV	1.95%
FF	27°C	5.364 mV	301.6 uV	5.62%
	-40°C	5.241 mV	348.2 uV	6.64%
	85°C	5.48 mV	277 uV	5.05%
SS	27°C	4.3 mV	106.6 uV	2.47%
	-40°C	4.125 mV	127.3 uV	3.08%
	85°C	4.47 mV	96.63 uV	2.16%

The ciDAC transfer pulse is generated by the comparator outputs ($D_{OUTP,N}$), and its short pulse width is defined by an inverter-delay-based pulse generator, as illustrated in the upper-left corner of Fig. 2. While the structural optimization of the CIC guarantees a uniform charge injection under an ideal transfer pulse, ensuring a uniform transfer pulse is consistently delivered to the ciDAC during every DAC switching phase is also critical to prevent code-dependent non-linearities. To guarantee this stringent pulse-width uniformity across all operating conditions, the following design considerations are implemented.

First, a dedicated buffer is inserted immediately before the NAND gate in Fig. 4. This buffering mechanism ensures sharp and deterministic transition edges of Tranfser[i-1], suppressing timing variations or jitter caused by mismatched signal slopes. Second, strict load matching and symmetrical routing are applied to the Transfer[4] and Transfer[i-1] paths to ensure identical capacitive loading across all switching configurations.

To evaluate the overall linearity and robustness of the proposed charge-injection DAC (ciDAC), Monte Carlo simulations were performed to analyze the statistical distribution of the unit voltage step (ΔV_{CIC}) dropped by a single CIC cell. Since the matching property of a single CIC directly governs the differential non-linearity (DNL) and integral non-linearity (INL) of the overall ciDAC, verifying ΔV_{CIC} across process corners and temperature variations is critical.

Table II summarizes the simulated mean (μ), standard deviation (σ), and coefficient of variation (σ/μ) of ΔV_{CIC} under various PVT conditions, including TT, FF, and SS

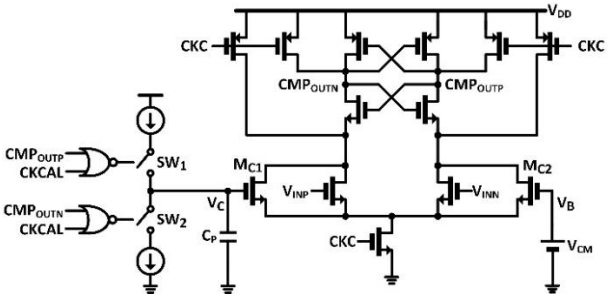


Fig. 6. Individual comparator schematic including offset calibration unit

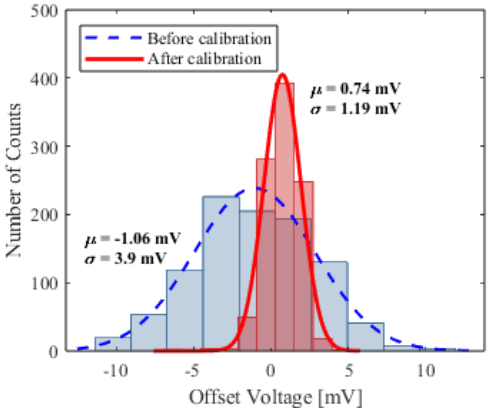


Fig. 7. Simulated input-referred comparator offset variation at V_{CM}=0.6V before/after offset calibration.

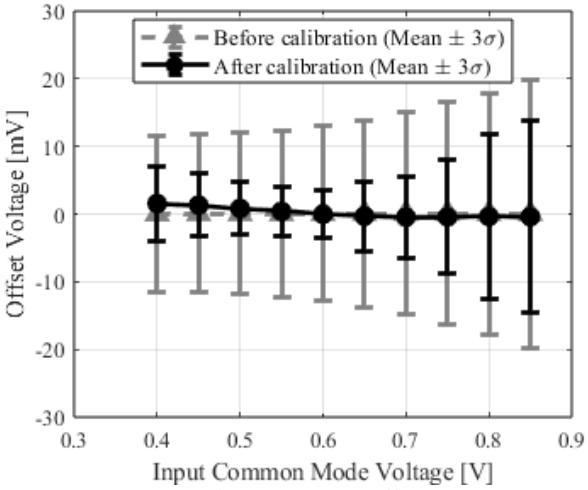


Fig. 8. Simulated input-referred comparator offset variation vs DAC common-mode voltage before/after offset calibration.

corners at temperatures of -40°C, 27°C, and 85°C. Across all evaluated PVT variations, the variation ratio is consistently maintained below 7%. These tightly controlled statistical distributions demonstrate the overall linearity and high yield of the ciDAC.

B. Comparator and its Offset Calibration Unit

Since the proposed ci-LU SAR ADC architecture utilizes 6 comparators, offset mismatches between them become a critical factor degrading the system's linearity. To address this issue, this design implements a self-calibrating offset cancellation circuit [15] to every comparators.

Every 6 Comparator unit consists of a StrongARM comparator, compensation current source (M_{C1} and M_{C2}) and charge pump circuit. At a start of calibration phase, right before the next sampling phase in Fig. 3, the inputs of comparators (DAC_P and DAC_N) are connected to the common mode voltage V_{CM}=0.6V, which corresponds to the average DAC common-mode voltage during the SAR conversion. If the comparator output is a High or Low signal due to an inherent offset, this output drives the charge pump to adjust the voltage V_C across the compensation capacitor C_P. The adjusted V_C controls the gate of the compensation current source, balancing the current at the internal nodes and forcing the offset voltage to converge toward zero after several quantization cycles. In the next conversion mode, the voltage stored on C_P is maintained, allowing the comparator to operate with the offset canceled.

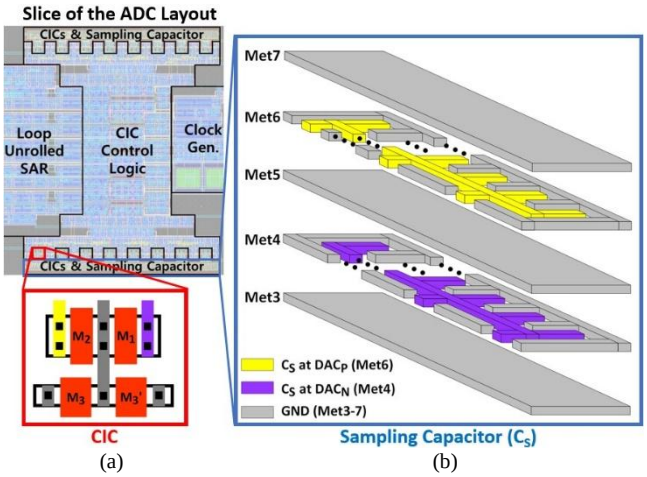
Fig. 7 shows the Monte Carlo simulated input-referred offset variation of the StrongARM comparator at V_{CM}=0.6V, which corresponds to the average DAC common-mode voltage during the SAR conversion. Before the offset calibration, the comparator exhibits an offset variation of 3σ=11.7mV, which is larger than 0.5LSB, leading to ADC linearity degradation. This error is mainly due to the device mismatch in the comparator. However, there are limitations in increasing the device size, because enlarged devices lead to increased parasitic capacitance which degrade speed and linearity of high speed ADCs. Therefore, the proposed offset calibration cancel out the device mismatch without deteriorating the performance. After calibration, the offset variation is reduced to 3σ=3.57mV, which is below 0.5LSB. This verifies the effectiveness of the implemented offset calibration.

Fig. 8 further evaluates the offset behavior over the DAC common-mode voltage range. Due to the common-mode-dependent characteristic of the StrongARM latch, the uncalibrated comparator shows noticeable offset variation as the common-mode changes due to the monotonic switching scheme. However, after calibration, 3σ is maintained below 0.5LSB across the overall DAC common-mode range Therefore, although the proposed ci-LU SAR architecture employs multiple comparators, the proposed offset calibration sufficiently suppresses comparator offset mismatches and preserves the linearity of the ADC.

C. Proposed Layout Implementation of CIC and Sampling Capacitor

While early ciDAC designs were implemented without regard to differential layout structures, recent works have explored various techniques to integrate ciDACs into fully differential ADC layouts. For instance, [16] and [17] attempted to achieve a differential layout by placing the ciDAC in the center of the ADC, while [18] employed two separate ciDACs arranged differentially. Building on the C_S layout concept in [14], this work introduces a more compact C_S implementation and co-locates it with the CICs in a fully differential, symmetric layout.

Fig. 9(a) and (b) display a slice of the ADC layout, illustrating the structure of the CIC and the adjacent



(a) (b)

Fig. 9. Proposed layout implementation of (a)CIC and (b)sampling capacitor

sampling capacitor on the lower side of the ADC. Although [14] proposed an area-efficient sampling capacitor arrangement to reduce the area of the ciDAC and C_S, the proposed work further enhanced the integration density of the C_S by adopting a finger structure DAC layout from [19]. Furthermore, while the layout in [14] improved density, it suffered from a mismatch between the C_S values on the DAC_P and DAC_N sides. This work aims to eliminate this discrepancy as well as simultaneously achieving a fully differential layout for C_S.

In the lower side of the ADC layout, the C_S for DAC_P is connected to the CIC via Met6, while the C_S for DAC_N connects via Met4. Conversely, in the upper side layout, the connections are swapped: DAC_P connects via Met4 and DAC_N via Met6. This cross-coupling technique ensures that the total parasitic and effective capacitance for DAC_P and DAC_N are matched. Through this approach, both the CICs and C_S are laid out fully differentially. Furthermore, the 16 CICs are arranged in a common-centroid pattern to minimize gradient mismatch.

IV. SIMULATION RESULTS AND ANALYSIS

A 6-bit ci-LU SAR ADC was designed to achieve a 400 MS/s conversion rate in a 65nm process. Fig. 10 shows its core layout with highlighted sub-blocks, where the ciDAC significantly reduces the area of the DAC network compared to a conventional CDAC-based implementation. As a result, the DAC network occupies 4 μm x 32 μm (279 μm^2 total), which corresponds to only 11.3% of the total core area of 41 μm x 77 μm (3157 μm^2).

Fig. 12 shows a simulated 2048-point power spectral density at 400 MS/s sampling frequency with a Nyquist-rate input. Before comparator offset calibration, significant harmonic distortion is observed due to comparator offset mismatches. After the proposed self-calibrating offset cancellation, the SNDR/SFDR improve from 29.64dB/41.22dB to 35.73dB/47.86dB, respectively. The total power consumption is 3.36 mW at 400 MS/s under a

TABLE III. Performance Summary and Comparison with Prior Work

	*This work	JSSC' 12 [11]	TCASII' 17 [20]	TCASII' 18 [21]	JSSC' 23 [22]	TCASI' 22 [23]	Elec. Letters 25 [24]
Process (nm)	65	40	40	55	40	28	500
Architecture	ci-LU SAR	LU SAR	LU SAR	5b LU SAR +2b SAR Ping-Pong	LU SAR 2x TI	LU SAR	LU SAR
Resolution (bits)	6	6	6	6	6-8	6	6
Supply Voltage (V)	1.0	1.0	1.2	1.2	1.1	1.2	5
Active Area (mm^2)	0.0031	0.014	0.004	0.03	0.0312	0.0038	-
Sampling Rate (GS/s)	0.4	1.25	0.7	1.3	$0.9_{@6b}$	1.5	0.01
$ENOB_{@Nyq.}$ (bits)	5.64	4.1	5.5	4.77	5.26	4.45	5.44
$SNDR_{@Nyq.}$ (dB)	35.73	26.8	34.8	30.5	$33.4_{@6b}$	28.6	34.53
$SFDR_{@Nyq.}$ (dB)	47.86	39	47.8	36.3	$48.4_{@6b}$	-	46.27
Power (mW)	3.36	6.08	0.95	3.5	**0.7	5.8	10.81
[1]Walden FoM_W (fJ/conv)	168	272	30	98.4	**20	176	24901
[2]IRD FoM ((TS/s·conv)/mm^2)	6.43	1.53	7.92	1.18	1.10	8.62	-

*simulated result **result w/o clock receiver and sampling switch
[1]Walden Figure of Merit, $FoM_W=P_{DC}/(F_{S,NYQ}\cdot 2^{ENOB})$
[2]Information Rate Density (IRD) $FoM=0.001\cdot F_{S,NYQ}\cdot 2^{ENOB}/Active\ Area$

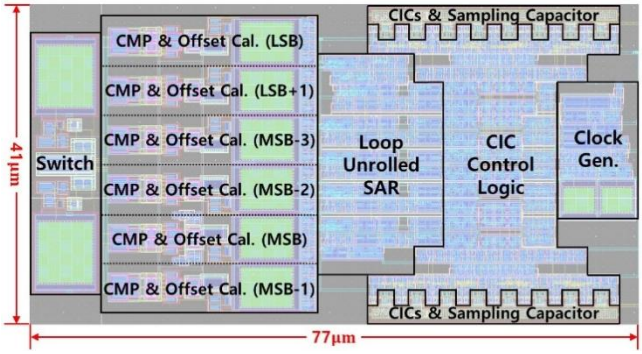


Fig. 10. Proposed layout structure of CIC and sampling capacitor

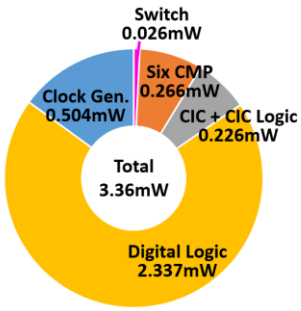


Fig. 11. Power breakdown of the proposed ci-LU SAR ADC

1.0 V supply. Fig. 11 illustrates the detailed power breakdown of the proposed ci-LU SAR ADC. The digital logic consumes the largest portion of power at 2.337 mW, while the clock generator and six comparators consume 0.504 mW and 0.266 mW, respectively. The remaining power is distributed between the CIC and its logic (0.226 mW) and the two sampling switches (0.026 mW). The simulated Walden figure-of-merit (FoM) at the Nyquist rate is 168 fJ/conversion-step, and the information rate density (IRD) FoM is 6.43, where a higher value indicates better efficiency. As summarized in Table III, this work achieves

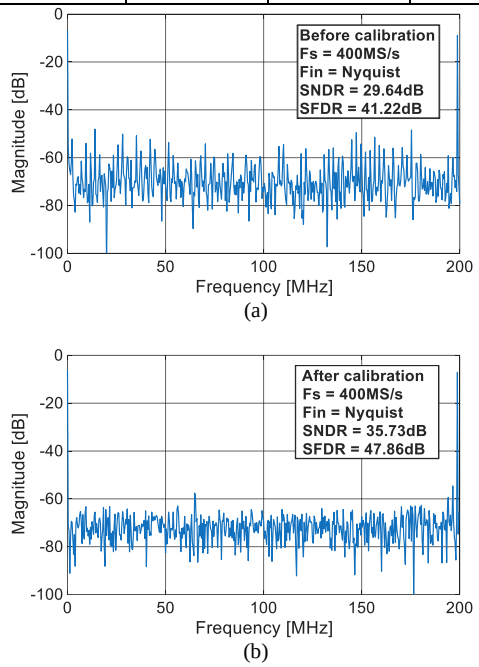


Fig. 12. Simulated 2048-point FFT spectrum result (a)before and (b)after offset calibration

the smallest active area among reported 6-bit LU SAR architecture, while maintaining an ENOB of 5.64 bits, despite being implemented in a less advanced technology node.

V. CONCLUSION

A 6-bit 400-MS/s ci-LU SAR ADC has been proposed to address the DAC area overhead of conventional LU SAR ADCs by replacing the CDAC with an area-efficient, reusable ciDAC. In 65-nm CMOS, the design achieves a compact 41 μm × 77 μm core, with the DAC network occupying only 11.3% of the core area. This work reports the smallest area among previously reported 6-bit LU SAR ADCs. Comparator offset mismatch is mitigated by embedding a self-calibrating offset-cancellation loop in each

Strong ARM-based comparator, where the calibration control voltage settles within a 24-mV range. Post-calibration simulations demonstrate improved linearity, achieving 35.73-dB SNDR and 47.86-dB SFDR at 400 MS/s and Nyquist input, while consuming 3.36 mW from a 1.0-V supply. With a 6-bit resolution, 400-MS/ sampling rate, and 0.0031-mm^2 core area, the proposed ADC satisfies key column ADC requirements in CIM macro-moderate resolution, wide but sub-GS/s input bandwidth, and a compact area compatible with tight pitch of memory-thereby making it well-suited for column ADC in large-scale CIM arrays.

ACKNOWLEDGMENT

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