A 1-Gb/s DDFS-based Baseband FDMA 8-Qubit Controller

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***Abstract* - We propose a direct digital frequency synthesizer (DDFS) based baseband multi-qubit controller with integrated pulse shaping and digital-to-analog converter (DAC). It supports eight multi-qubit control and four pulse shapes operating at 1 GHz clock speed. The digital baseband waveform generator offers programmable frequency, phase, amplitude, and pulse envelope. Pulse shaping demonstrates significant sidelobe suppression, leading to reduced adjacent channel interference. Clock gating is applied, resulting in a 9.46 % reduction in power consumption for single qubit control. The proposed baseband controller is implemented in 65 nm low-power (LP) CMOS process and achieves 62.13 dB of spurious-free dynamic range (SFDR) at the single frequency output signal. The total active area of the chip is 4 mm².**

***Keywords*—Direct digital frequency synthesizer (DDFS), frequency-division multiple access, quantum computing, qubit controller**

I. INTRODUCTION

Quantum computing has attracted considerable interest in many fields with its ability to address computational problems that are beyond the reach of classical computers in significantly reduced running time in certain algorithms [1], [2]. However, realizing large-scale quantum processors requires precise and scalable control of qubits, and it poses significant challenges in terms of wiring complexity, power consumption, and system integration. To address these challenges, designing transmitters for efficient and scalable qubit control has become a critical issue.

One commonly adopted approach for qubit control is an RF transmitter architecture that employs digital baseband signal generation followed by DAC and I/Q up-conversion mixer. This transmitter structure exhibits high spectral efficiency due to its single-sideband modulation, and it enables image rejection without requiring high order filters [3]. Moreover, the digital baseband signal generation has recently attracted attention for scalable qubit control [4]. By digitally synthesizing the baseband waveform, this architecture enables precise frequency and phase control, flexible waveform generation, and improved robustness against process and temperature variations. In this work, we focus on the digital baseband signal generation block of the transmitter, assuming a conventional I/Q up-conversion stage.

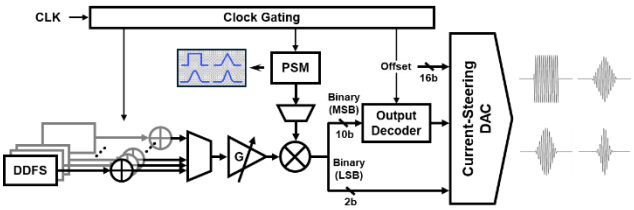

Fig. 1. Overall block diagram of baseband qubit controller.

Frequency-division multiple access (FDMA) has been widely adopted as an efficient strategy for multi-qubit control, enabling multiple qubits to be driven simultaneously through a single control line by assigning distinct frequencies [5]. This approach significantly reduces wiring complexity and improves system scalability; however, it introduces stringent requirements on spectral purity and inter-channel interference suppression [4], [6]. In FDMA-based qubit control systems, high SFDR should be achieved, as spurious components can lead to unintended excitation of neighboring qubits. To prevent interference with idle qubits, an SFDR better than 44 dB is required for 99.99% fidelity [3]. Additionally, to lower spectral leakage, pulse shaping techniques are required to confine the signal energy within the allocated frequency band while maintaining precise control over the pulse envelope. Implementing pulse shaping in the digital baseband domain allows precise and programmable control of the pulse envelope, independent of additional analog filtering. Additionally, clock gating is applied to optimize the power consumption in digital circuits.

The digitally synthesized baseband waveform must be converted to the analog domain with sufficient linearity and bandwidth to be upconverted by mixer and transmitted to the qubits. The current-steering (CS) DAC is adopted for this application due to its high-speed operation and linearity.

In this work, we present a baseband 8-qubit controller based on the DDFS and the CS DAC, targeting FDMA-based multi-qubit operation.

II. CIRCUIT IMPLEMENTATION

The overall architecture of the proposed baseband part of

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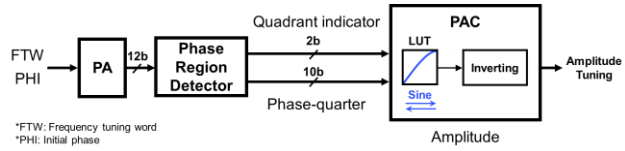


Fig. 2. Block diagram of the quarter-method employed DDFS.

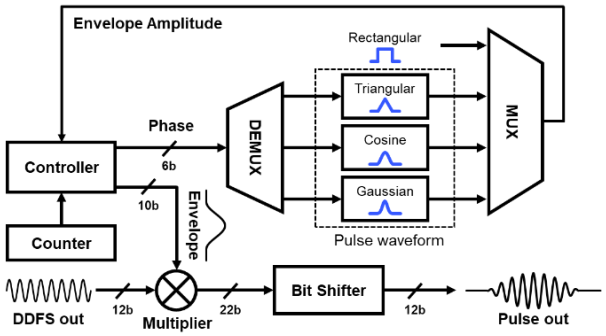


Fig. 3. Digital pulse shaping module architecture.

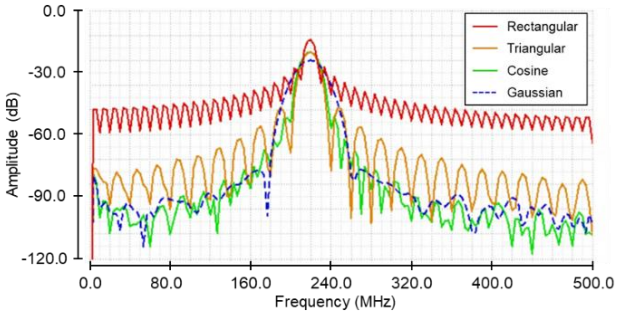


Fig. 4. Simulated spectra for pulse shaping at 220 MHz.

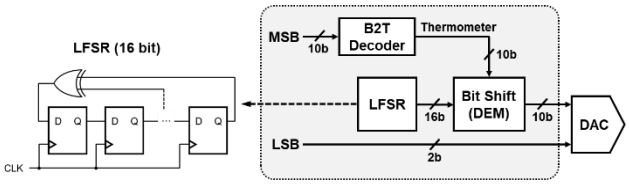


Fig. 5. Digital output binary-to-thermometer converter and DEM module.

the qubit controller is illustrated shown in Fig. 1. The DDFS generates frequency, phase and amplitude tunable digital waveforms. Parallel eight DDFSs are included to generate a maximum of eight frequency components. A pulse shaping module generates an envelope and then multiplies it by the DDFS output signal. An output decoder converts the output signal format to interface with the CS DAC.

A. Direct Digital Frequency Synthesizer

A ROM-based DDFS is implemented using the quarter method to generate a baseband arbitrary sinusoidal waveform with preset frequency, phase, and amplitude [7]. Fig. 2 presents a block diagram of the proposed DDFS circuit. A phase accumulator accumulates the phase with a programmable step, referred to as frequency tuning word (FTW), to control the output signal frequency. A phase region detector indicates the current phase quadrant to apply the quarter method. Based on the detected quadrant indicator, the phase rotation direction and amplitude polarity are determined. In the phase-to-amplitude converter (PAC), a look-up table (LUT) stores one quarter of the sine waveform. Based on the LUT phase index, the appropriate amplitude of the sinusoidal waveform is generated. Finally, the amplitude of the generated sinusoidal waveform is adjusted according to external control inputs. By operating eight DDFS cores in parallel, the proposed architecture generates control signals with up to eight frequency components, enabling precise control of phase, amplitude, and offset for each signal.

B. Pulse Shaping Module

Pulse shaping is necessary for actual control of qubits to ensure that control signals are generated at the desired point in the frequency domain. It resolves the unnecessary sidelobe performance by employing the pulse shaping module. Fig. 3 shows the block diagram of the designed pulse shaping module. Each point of the pulse shape data is pre-stored in the LUT except for the rectangular pulse. The rectangular pulse is generated directly using 1-bit logical value. When a pulse shape is selected through external control inputs, a pulse shape controller controls the indexing of LUT phases as well as the multiplexer and demultiplexer to produce a 100 ns control pulse waveform. By exploiting the symmetry of the pulse shapes, only half of each waveform period needs to be stored in the LUT, enabling an area-efficient implementation. The pulse envelope is generated through the controller and LUTs, then it is multiplied by the DDFS output signal. The bit shifter aligns the amplitude data of the generated pulse waveform. In this system, four types of pulse shapes are selectable among rectangular, triangular, cosine, and Gaussian.

Fig. 4 shows the simulation results of the designed pulse shaping module with DDFS in the frequency domain. The four single-frequency signals at 220 MHz are shaped into 100 ns pulses using rectangular, triangular, cosine, and Gaussian shapes, respectively. The triangular, cosine, and Gaussian pulses exhibit reduced adjacent-band interference compared to the rectangular pulse, with the cosine pulse providing significant sidelobe suppression of 30.74 dB while maintaining a relatively narrow main lobe width of 30 MHz.

C. Output Decoder

The MSB 10-bit of the qubit control pulse signal is converted into a thermometer format by the output decoder to match the unary weighted DAC architecture. A dynamic element matching (DEM) technique is applied to attenuate the effects of linearity degradation caused by unit current source mismatch and imbalanced dynamic switching of the DAC. A linear feedback shift register (LFSR) is used to generate the pseudo-random code for the DEM technique, and the usage frequency of unit current cells changes according to the random code.

D. Current-Steering DAC

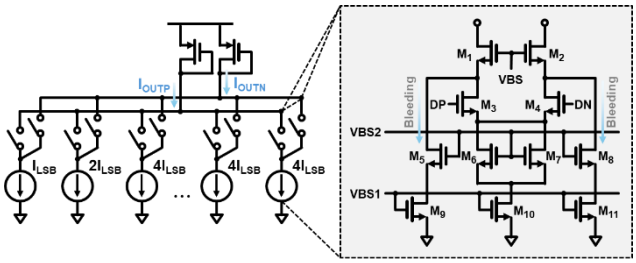
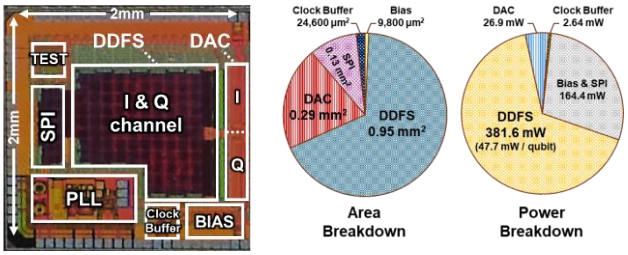


Fig. 6. Schematic of current steering DAC.

The digital control signal generated by the DDFS and pulse shaping module is converted to an analog baseband signal through a DAC. A current-steering DAC structure favorable for high-speed operation is applied to prevent performance degradation even when generating eight different frequency signals within the target bandwidth of 500 MHz. The DAC is designed with a 12-bit resolution to ensure a high signal-to-noise ratio (SNR). The DAC operates based on a unary decoding method where each current unit has the same weight on the MSB 10 bits, and additional LSB 2 bits are binary decoded. This method is used in conjunction with the DEM technique to mitigate the nonlinear effects caused by mismatches between each unit.

Fig. 6 shows the structure of the proposed segmented current-steering DAC, which comprises unary-weighted MSBs and binary-weighted LSBs. The cascode structure is implemented using transistors M_1-M_2 and M_5-M_8, which reduces code-dependent distortion and improves current matching and linearity. The current value of the unit cell is approximately 400 nA, and the bleeding current provides a continuous current path during code transitions, mitigating severe glitches and contributing to enhanced SFDR performance.



(a) (b)

Fig. 7. (a) Chip microphotograph with (b) area and power breakdown.

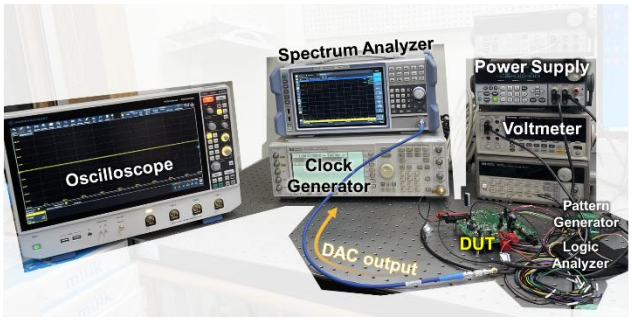
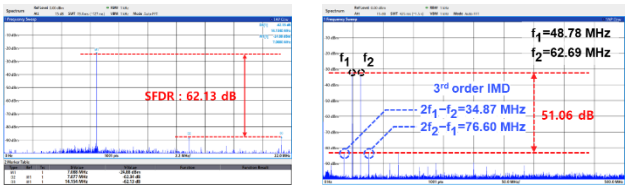


Fig. 8. Measurement setup.



(a) (b)

Fig. 9. Measured (a) single frequency output at 7.09 MHz and (b) two-tone test with 48.78 MHz and 62.69 MHz.

TABLE I. Measured SFDR according to the Output Signal Frequency.

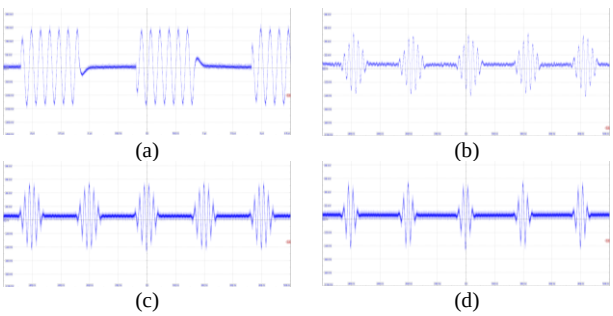
	7.24 MHz	48.7 MHz	156.09 MHz	250.5 MHz	361.39 MHz	468.78 MHz
SFDR	61.09 dB	55.20 dB	52.03 dB	52.21 dB	40.06 dB	33.11 dB
P_{signal}	-24.72 dBm	-25.89 dBm	-24.91 dBm	-25.94 dBm	-25.37 dBm	-26.18 dBm

III. RESULTS AND DISCUSSIONS

Fig. 7 shows the chip microphotograph fabricated in 65-nm LP CMOS technology. The total area is 4 mm^2, and the DAC and DDFS, including the I/Q channels, are 0.29 mm^2 and 0.95 mm^2, respectively. The power consumption of the DAC is measured to be 26.9 mW, while the DDFS consumes 47.7 mW per qubit when generating eight qubit control signals. By applying clock gating, the digital domain power consumption for synthesizing a single frequency signal is reduced from 144.78 mW to 131.08 mW, corresponding to a 9.46 % improvement. The measurement setup includes a signal generator for a 1.0 GHz clock signal, a pattern generator for SPI communication, an oscilloscope and a spectrum analyzer for DAC output measurement as shown in Fig. 8. The differential DAC output is converted to voltage using current mirror and converted to the single-ended output through off-chip balun.

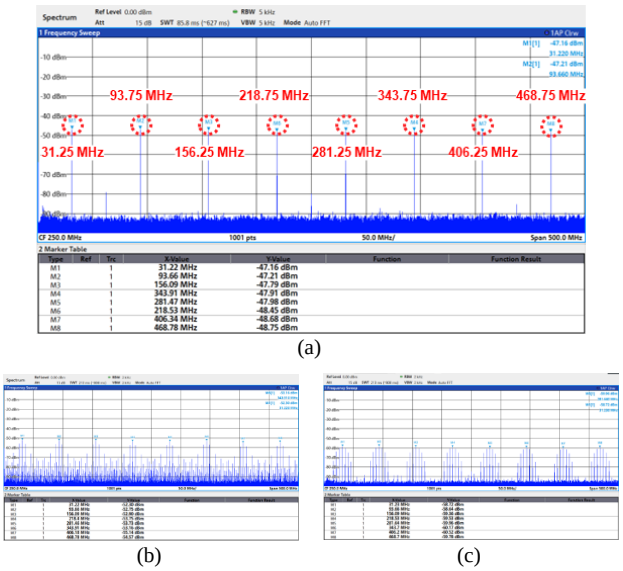
Fig. 9. (a) presents the measured single-frequency output from DDFS and DAC. The proposed DDFS and DAC achieve 62.13 dB SFDR at the output frequency of 7.09 MHz. Table I summarizes the measured SFDR performance across different output frequencies. An SFDR greater than 52 dB is achieved below 250.5 MHz, while it degrades at higher frequencies. A two-tone test was performed at frequencies of 48.78 MHz and 62.69 MHz to evaluate the nonlinear distortion and intermodulation products of the DAC as shown in Fig. 9. (b). The measured spectrum exhibits third-order intermodulation products, resulting in an SFDR of 51.06 dB.

The pulse shaping plays a key role in controlling the trade-



(a) (b) (c) (d)

Fig. 10. Measured pulse waveform of (a) rectangular, (b) triangular, (c) cosine, and (d) Gaussian.



(a)

(b) (c)

Fig. 11. Measured 8-tone frequency output spectrum for (a) without pulse shaping and (b) rectangular, (c) cosine pulse shaping.

off between qubit operation speed and energy leakage to the unaddressed qubits. Four types of pulse shaping were experimentally demonstrated to verify the pulse shaping performance of the fabricated chip. Fig. 10 shows the measured time-domain pulse waveforms at the clock frequency of 1 GHz and the output frequency of 62.5 MHz.

The measured frequency domain responses of the simultaneously generated eight frequency components outputs are shown in Fig. 11. (a). The output frequencies are spaced at 62.5 MHz and are measured at 31.25 MHz, 93.75 MHz, 156.25 MHz, 218.75 MHz, 343.75 MHz, and 406.25 MHz, with signal power levels of approximately -49 to -47 dBm. The spectral distributions obtained by applying rectangular and cosine pulse shaping to the eight frequency tones are compared in Fig. 11. (b) and (c). For the individual qubit control output, the measured sidelobe suppression levels achieved by rectangular and cosine pulse shaping are 12.83 dB and 30.71 dB respectively. When applied to multi-frequency operation, the proposed multi-qubit control system exhibits significantly reduced inter-channel interference compared to the conventional rectangular pulse when the cosine pulse shaping is applied, demonstrating its effectiveness in suppressing spectral overlap between different qubit channels. A summary of the chip performance is provided in Table II.

TABLE II. Performance Summary of Proposed Baseband Multi-Qubit Controller

Data Bandwidth	500 MHz
Frequency Tuning Resolution	12-bit
Frequency Tuning Range	977 kHz – 500 MHz @ 1 GHz
Maximum Number of Supporting Qubits	8
Pulse Shaping	Rectangular/Triangular/Cosine/Gaussian
SFDR	62.13 dB @ 7.09 MHz
Power Dissipation	Analog: 29.52 mW* Digital: 47.7 mW / qubit

* Including DAC I/Q channel & clock buffer

IV. CONCLUSION

The DDFS-based baseband multi-qubit controller is proposed. This architecture supports parallel operation of eight frequency channels, enabling simultaneous control of up to eight qubits for FDMA. Four types of pulse shaping were implemented to investigate their impact on spectral characteristics. To eliminate unnecessary power consumption in the digital domain, a clock gating circuit was applied to optimize the operating conditions of the qubit controller. The proposed baseband qubit controller is implemented in a 65 nm LP CMOS process, and validated to provide an effective and scalable solution for multi-qubit control systems.

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