A Leakage-Attenuated Auto-Zeroing High-Pass Filter Using Switch Voltage Regulation

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***Abstract* – This paper presents leakage-attenuated feedback (LAF) auto-zeroing high-pass filter (AZHPF) for various analog front-end applications. AZHPF is widely used to cancel DC offset. However, AZHPF suffers from leakage induced voltage decay during auto-zeroing phase. This leads to large offset error and performance degradation particularly at low operation frequency. To overcome this limitation, LAF is proposed. As a result, the proposed LAF AZHPF achieves improved offset cancellation. Simulation results verify the effectiveness of the proposed approach, making the proposed AZHPF suitable for low-frequency precision applications. In this proposed design, an error amplifier is used to regulate the voltage across the switches connected to the sampling capacitor. By maintaining equal voltage levels at both switch nodes, the stored offset voltage is preserved over time without increasing the sampling capacitance. Simulation results demonstrate the proposed design successfully achieves lower offset error than the conventional design over wide range from 10 mHz to 1 kHz. In particular, the proposed approach validates its effectiveness as a general solution for leakage current prevention at low frequency in auto-zeroing circuits.**

***Keywords*—Auto-zeroing, offset cancellation, high-pass filter, leakage current, feedback regulation.**

I. INTRODUCTION

In precision analog front-end systems, it is important to accurately extract the AC component of the signal by effectively removing DC offset. The DC component typically comes from bias voltage, while the information is mainly contained in AC component. In convention designs, various architectures such as preamplifiers [1], or RC high-pass filters (HPFs) were used to cancel offset voltage. RC HPFs require extremely large RC time constants to achieve very low cutoff frequencies, which results in large circuit area and slow transient response. Moreover, passive RC HPFs suffer from inherent limitations such as passband attenuation and limited realizability when only resistors and capacitors are used [2]. To overcome these limitations, auto-zeroing high-pass filter (AZHPF) can be a good alternative. Fig. 1 shows the concept of AZHPF, in which the DC component is canceled and the AC component is extracted from the input signal. By using switches and a single sampling capacitor, AZHPFs can effectively cancel DC offset of the input signal without large passive components such as resistors and capacitors.

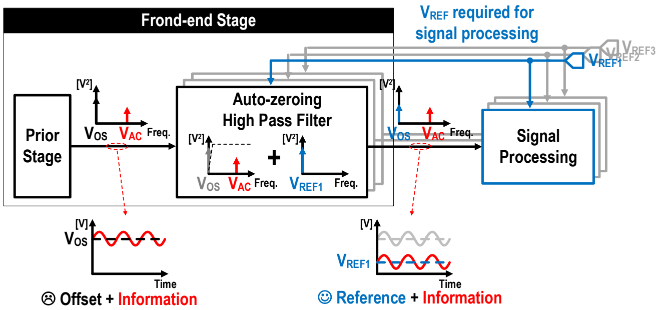

Fig. 1. The concept of AZHPF for DC offset removal.

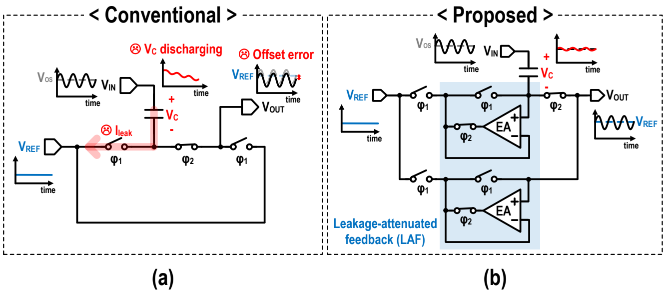

Fig. 2. (a) Conventional AZHPF structure and (b) proposed AZHPF structure.

The operation of a conventional AZHPF, as shown in Fig. 2(a), is described as follows. A conventional AZHPF periodically samples and removes the DC offset of the input signal by using a sampling capacitor and switches. During φ_1, the sampling capacitor stores the voltage difference between the DC signal of the input signal and the reference voltage V_{REF}. In φ_2, stored voltage is used to cancel the DC offset of the input signal, allowing only the AC component of the input signal to appear at the output around V_{REF} at the output.

However, DC channel leakage currents through the turned-off switches and the sampling capacitor cause the voltage across the capacitor to gradually decrease. As a

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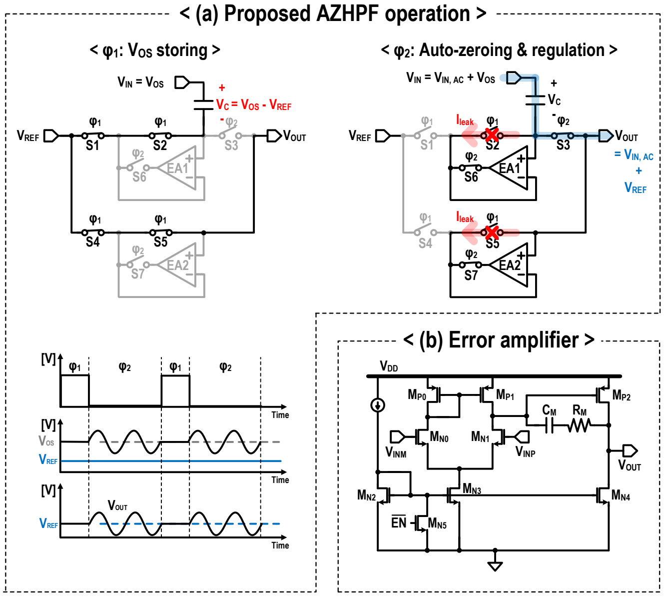

Fig. 3. (a) The proposed AZHPF operation for each phase (b) error amplifier structure.

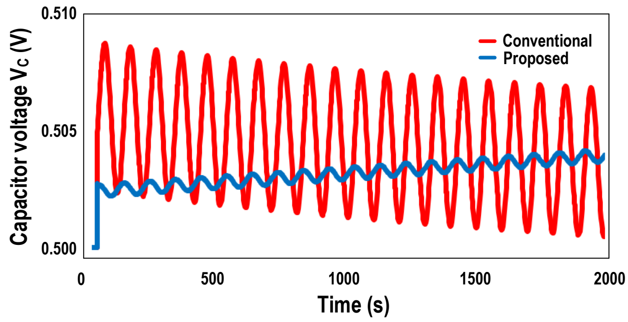

Fig. 4. Simulation results of voltage across capacitor.

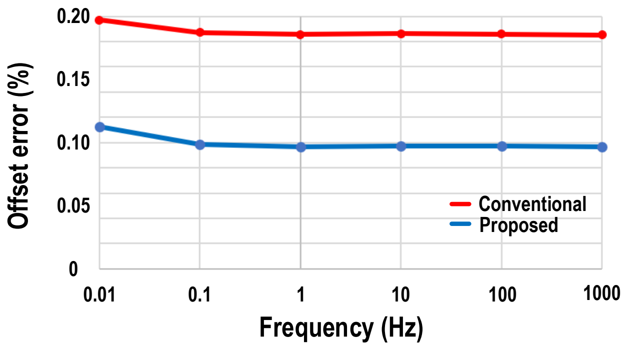

Fig. 5. Simulated offset error as a function of input frequency for the conventional and proposed AZHPFs.

result, the stored offset voltage cannot be maintained, leading to inaccurate DC offset cancellation and offset shift to V_{REF}. In charge-based circuits, low-leakage switches are essential, as leakage currents directly limit the hold time of stored signals [3]. The error caused by leakage current becomes more severe as the hold time increases and the operating frequency decreases. As a result, DC leakage currents significantly degrade the offset compensation performance of conventional AZHPF.

Various circuit techniques have been proposed to suppress switch leakage, including approaches that regulate the terminal voltages of transistors to minimize leakage currents. By reducing the voltage difference across the switch terminals, channel leakages can be effectively suppressed [4].

This work applies such a voltage regulation technique to an AZHPF and proposes a leakage-suppressed AZHPF based on switch terminal voltage feedback. By regulating the voltage across the switch terminals through an error amplifier–based feedback loop, the proposed structure effectively suppresses leakage currents.

II. PROPOSED ARCHITECTURE

Fig. 2(b) shows the proposed AZHPF architecture presented in this paper, which operates with a 5V supply voltage. An error amplifier-based feedback path is added to control the voltage across the turned-off switches connected to the sampling capacitor. This structure preserves the conventional switching and sampling operation while minimizing leakage current. The error amplifier senses the voltages at both nodes of the switch and regulates two node voltages by adjusting its output.

Fig. 3 (a) shows the operation of the proposed AZHPF in two clock phases, the offset voltage storing phase (φ_1) and the auto-zeroing and regulation phase (φ_2), and also presents the timing diagram of the auto-zeroing clock along with the corresponding waveforms. During φ_1, the sampling capacitor is directly connected to the reference voltage V_{REF} node through the switches S1, S2, S4 and S5, which are turned on. As a result, the voltage across the sampling capacitor is charged to the difference between the DC offset of the input signal V_{OS} (Fig. 3) and the reference voltage V_{REF}. This operation stores only the input DC offset on the sampling capacitor. And this stored voltage is then used in the following phase (φ_2) to remove the DC offset from the input signal.

$$V_C = V_{OS} - V_{REF} \qquad (1)$$
$$V_{OUT} = V_{REF} \qquad (2)$$

During φ_2, all signal paths to V_{REF} node are disconnected as the corresponding switches are turned off, while the sampling capacitor is directly connected to the output node through the switch S3, which is turned on. The voltage previously stored on the sampling capacitor ($V_{OS} - V_{REF}$) is then combined with the input signal. As a result, the stored voltage cancels the DC offset component of the input signal. Therefore, only the AC component referenced to V_{REF} appears at the output. Consequently, the output voltage can be expressed as (4).

$$V_{IN} = V_{IN,AC} + V_{OS} \qquad (3)$$
$$V_{OUT} = V_{IN,AC} + V_{REF} \qquad (4)$$

It indicates effective removal of the input DC offset. At the same time, the feedback loop switches S6 and S7 that was turned off during φ_1 are turned on in φ_2. The error amplifiers EA1 and EA2 actively regulate the voltages at both nodes of the switch connected to sampling capacitor. It maintains a near-zero voltage difference across the switch. This regulation prevents to make DC leakage current path.

Thereby preserving the stored voltage on the sampling capacitor and ensuring accurate offset cancellation. The error amplifier is designed with consideration of the feedback loop stability (Fig. 3(b)). The Miller capacitance C_M and the Miller resistor R_M are approximately 100 fF and 23 kΩ. The simulated DC gain and unity-gain bandwidth of the error amplifier are 78.87 dB and 72.39 MHz, respectively, which ensure sufficient loop gain and settling.

Due to finite gain of the error amplifier, the voltage across the switch terminals cannot be perfectly regulated to zero. As a result, a small residual error remains, which is inversely proportional to the loop gain of the error amplifier.

III. SIMULATION RESULTS

Fig. 4 shows the voltage waveforms across the sampling capacitor of the conventional AZHPF and the proposed AZHPF. The simulation is performed at an input frequency of 10 mHz. During the auto-zeroing phase, the DC voltage across the sampling capacitor without LAF gradually decreases over time. In contrast, capacitor voltage in the proposed LAF AZHPF remains stable without noticeable decay, with a slight voltage increase over time. It demonstrates effective attenuation of leakage-induced voltage loss. A slight voltage increase is attributed to residual non-ideal switching effects, such as asymmetric junction leakage in the switches, which become more noticeable after the channel leakage is suppressed by the proposed structure.

Fig. 5 compares the offset error of the conventional AZHPF and the proposed AZHPF over an input frequency range from 10 mHz to 1 kHz. The simulations are performed at six frequency points distributed on logarithmic scale. For each frequency, the output voltage is averaged over 10 periods of the input signal, corresponding to the hold duration, to extract the DC offset. The offset error is defined as the difference between the averaged output voltage of the AZHPF and the ideal reference voltage. The offset error is generally largest at low frequency and gradually decrease as the frequency increases. This trend is because of the longer operation time and hold duration at lower frequency. It causes more significant voltage decay on the sampling capacitor. To quantitatively verify the leakage attenuation, the net leakage current from the sampling capacitor is averaged during the hold phase. The proposed LAF structure reduces the average leakage current from 19.48 aA to 7.67 aA. As shown in Fig. 5, the proposed AZHPF achieves lower offset error than the conventional AZHPF at all simulated frequency points. At the lowest simulated frequency of 10 mHz, the conventional AZHPF reaches 0.20%, while the proposed AZHPF reduces it to 0.11%. This result demonstrates that the proposed LAF structure successfully suppresses DC leakage-induced errors over the entire frequency range.

IV. CONCLUSION

This paper presented a LAF AZHPF which improves DC offset cancellation accuracy in precision analog front-end applications. While conventional AZHPFs effectively remove DC offset without large passive components, their accuracy is limited by DC leakage currents. Leakage current through the turned-off switch occurs switching capacitor voltage decay which leads to offset errors and performance degradation especially at low operating frequencies.

TABLE I. Comparison between Conventional and Proposed AZHPF

	Conventional AZHPF	Proposed AZHPF
Process	180-nm	180-nm
Sampling Capacitance	10 pF	10 pF
Supply Voltage	5 V	5 V
Frequency Range	10 mHz−1 kHz	10 mHz−1 kHz
Capacitor Leakage Current @10 mHz	11.73 aA	7.63 aA
Current Consumption	2.67 pA	42.28 uA
Offset Error @10 mHz	0.20%	0.11%

To address this limitation, proposed AZHPF architecture with LAF was proposed. By implementing an error amplifier to regulate the voltage across the turned-off switches connected to the sampling capacitor, the proposed structure effectively minimizes the DC leakage currents. As a result, the stored offset voltage is preserved stably over time, leading to successful offset cancellation without increasing sampling capacitance.

Simulation results showed that the proposed AZHPF achieves lower offset error than the conventional AZHPF over range from 10 mHz to 1 kHz frequency. In particular, the proposed design achieves stable offset compensation at low-frequency, where conventional structures suffer from leakage-induced voltage decay. These results show that the proposed design provides an effective and general solution for leakage attenuation in auto-zeroing circuits, making it suitable for a wide range.

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