Total-Ionizing Dose Effects in CMOS Operational Amplifiers with NMOS and PMOS Differential Pairs

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Abstract - **This paper investigates the impact of total ionizing dose (TID) effects on two-stage CMOS operational amplifiers employing NMOS and PMOS differential input pairs. Previously reported TID-induced threshold voltage shifts for a 180-nm CMOS process are adopted and applied at the circuit level through controlled gate voltage offsets for a fair comparison under identical design constraints. The transistor width and length are fixed, and the effective device size is adjusted by varying the number of transistor fingers to match bias conditions and power consumption between the two amplifier configurations. Circuit-level simulations are performed under a TID condition of 125 krad (SiO_2) and compared with pre-irradiation baseline results. The results show that both NMOS and PMOS differential pair amplifiers maintain stable operation without functional failure. Key small-signal performance metrics, including DC gain, bandwidth, and phase margin, exhibit only moderate changes while stable operation is preserved after TID exposure. In contrast, power consumption shows a more noticeable increase, particularly in the NMOS-input amplifier, reflecting a stronger sensitivity of bias current to TID-induced device degradation.**

Keywords— **CMOS, differential pair, operational amplifier, total ionizing dose (TID), radiation effects**

I. INTRODUCTION

Integrated circuits operating in radiation environments such as space systems, high-energy physics experiments, and nuclear instrumentation are exposed to various radiation-induced effects that can significantly degrade long-term reliability and performance. In particular, analog and mixed-signal circuits are highly sensitive to small parameter variations, as even minor changes in device characteristics can directly translate into noticeable performance degradation or functional failure at the circuit level.

Radiation effects in CMOS technologies can be broadly classified into single-event effects (SEEs) and total ionizing dose (TID) effects. SEEs are caused by individual high-energy particles and typically result in transient or permanent events, whereas TID effects arise from the cumulative deposition of ionizing radiation over time [1]-[3]. TID induces permanent changes in device characteristics through charge trapping in oxide regions and the generation of interface states, leading to threshold voltage shifts, mobility degradation, and variations in leakage and bias currents [4]-[6]. Owing to their cumulative and irreversible nature, TID effects are particularly critical for analog circuits that are required to maintain stable performance over extended operational lifetimes.

Extensive studies have been reported on TID-induced degradation at the device level, as well as on radiation-hardened-by-design techniques primarily targeting digital circuits. However, systematic circuit-level investigations of analog building blocks under TID stress remain relatively limited. Moreover, existing studies often focus on a single circuit topology, making it difficult to isolate the impact of architectural choices on radiation tolerance. In particular, a direct comparison between NMOS and PMOS differential pair operational amplifiers under identical TID conditions has not been sufficiently explored.

In this study, we investigate the influence of the TID effect on a two-stage operational amplifier (OPAMP) using NMOS and PMOS differential pairs. This study adopts previously reported TID degradation characteristics for a 180-nm CMOS process and applies controlled threshold voltage variations at the circuit level. To ensure a fair comparison, identical transistor dimensions are used for both amplifier implementations, while the number of transistor fingers is adjusted to match the power consumption and bias conditions between the NMOS- and PMOS differential pair designs.

By comparing key performance metrics including DC gain, bandwidth, phase margin, gain bandwidth product, and power consumption before and after irradiation, this work provides practical insight into how the choice of input differential pair affects TID-induced performance degradation in two-stage OPAMPs. These results offer useful design guidance for selecting suitable analog circuit topologies intended for radiation-exposed environments.

The organization of the paper is as follows. In Section II, the adopted TID-induced device degradation characteristics and the circuit-level implementation are described in detail, and in Section III, simulation results under TID stress are presented and analyzed. Section IV summarizes the findings of this work.

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II. DEVICE DEGRADATION AND CIRCUIT IMPLEMENTATION UNDER TID EFFECTS

A. TID-Induced Device Degradation

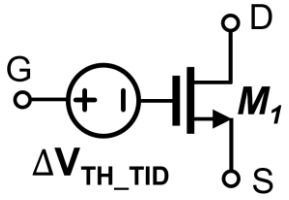


Fig. 1. Implementation of the TID-induced threshold voltage shift using an equivalent gate-level voltage source

This work adopts a previously reported TID degradation model for a 180-nm CMOS process to evaluate radiation-induced performance variations at the circuit level [7]. The objective of this study is to investigate how TID-induced device degradations translate into performance changes in analog circuits, particularly OPAMPs with different input differential-pair configurations. According to prior experimental studies on 180-nm CMOS technologies, TID exposure primarily manifests as a threshold-voltage shift due to charge trapping in oxide regions and the formation of interface states [7]. Based on these results, threshold-voltage shift magnitudes of 23 mV for NMOS devices and 12 mV for PMOS devices under a total dose of 125 krad (SiO_2) are adopted in this work [7].

In this study, the TID effect is modeled as a first-order threshold-voltage perturbation at the circuit level. The adopted threshold-voltage shifts are implemented using equivalent gate-level voltage offsets with opposite polarities for NMOS and PMOS devices so that the corresponding post-irradiation threshold-voltage shifts in [7] can be reproduced in circuit simulation (see Fig. 1). By introducing a controlled voltage source in series with the gate terminal, the effective threshold voltage of each transistor is modified without altering the underlying device model parameters. This approach allows systematic evaluation of TID-induced performance variations while maintaining compatibility with standard CMOS simulation frameworks. Other TID-related effects, such as mobility degradation and leakage-current increase, are recognized as important physical mechanisms but are not independently parameterized in the present work. Therefore, the post-TID simulation results should be interpreted as circuit responses under an adopted Vth-shift-based TID abstraction rather than as a complete device-level reconstruction of all radiation-induced degradations.

It should also be noted that the threshold-voltage shifts adopted from [7] were obtained under specific device bias conditions, whereas the transistors in an operating OPAMP experience different terminal voltages depending on their circuit roles. Therefore, the exact TID-induced threshold-voltage shift may vary from device to device in a practical circuit. Nevertheless, the reported results in [7] provide a useful first-order indication of the threshold-voltage degradation trend under TID stress, which can be translated to circuit-level operating-point perturbations. In this work,

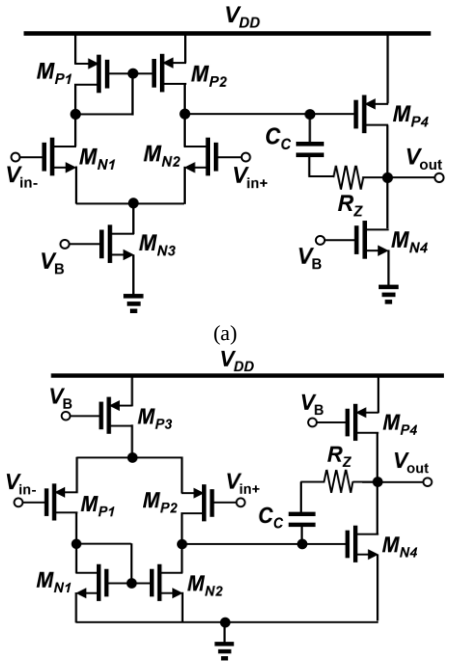


Fig. 2. Two-stage operational amplifier schematic used for TID effect analysis: (a) NMOS differential pair and (b) PMOS differential pair

these values are used as representative first-order perturbations to enable a controlled comparison between NMOS- and PMOS-input OPAMP architectures under a common TID condition. Accordingly, the present approach is intended to compare the relative circuit-level sensitivity and degradation trends of the two topologies rather than to provide an exact transistor-by-transistor prediction of post-irradiation parameter shifts.

B. Two-Stage Operational Amplifier Schematic

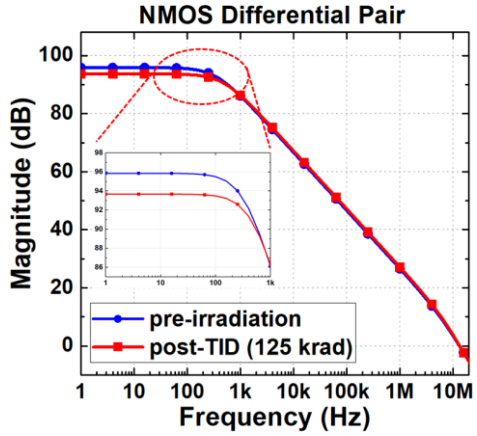
TABLE I. Number of Fingers of Transistors in Two-Stage Operational Amplifiers with NMOS and PMOS Differential Pairs

Parameter	NMOS diff. pair	PMOS diff. pair
M_{N1}, M_{N2}	2	3
M_{P1}, M_{P2}	4	7
M_{N3}	4	–
M_{P3}	–	14
M_{N4}	8	13
M_{P4}	17	19

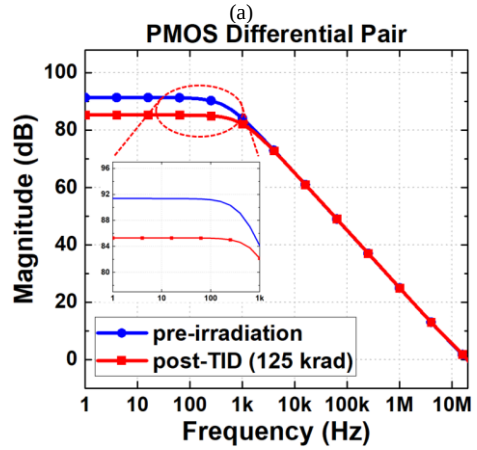
(Transistor dimensions are fixed to W/L = 5 μm / 5 μm for all devices)

The circuit architectures investigated in this study are two-stage OPAMPs employing either an NMOS or a PMOS differential pair. The schematics of the two amplifier configurations are shown in Fig. 2. Except for the type of input differential pair, the overall topology including biasing scheme and Miller compensation network is kept identical to ensure a fair comparison.

To maintain consistency with the adopted TID



(a)



(b)

Fig. 3. Open-loop magnitude responses of the two-stage operational amplifiers with (a) NMOS and (b) PMOS differential pairs before and after TID stress (125 krad)

characterization data, the transistor width and length are fixed to W/L = 5 µm / 5 µm for all devices in both amplifier implementations. This constraint arises because the referenced TID data were reported for this specific unit-device structure [7]. In addition, the relatively long channel length helps suppress the effect of channel-length modulation, so that the circuit-level comparison is less influenced by short-channel-induced gain variation. Accordingly, circuit sizing is performed only by varying the number of fingers. Although the OPAMPs in this work employ multi-finger transistors, the exact post-irradiation threshold-voltage shift of each device may differ from that of the single-device reference because layout-dependent effects, such as STI-related edge variations, can affect threshold voltage and current characteristics. Nevertheless, the data in [7] still provides a practical first-order basis for representing the TID-induced degradation trend at the circuit level. Under this common device-level constraint, the present study focuses on comparing the relative degradation trends of NMOS- and PMOS-input OPAMP architectures rather than predicting layout-dependent shifts for each individual transistor instance.

The NMOS differential pair OPAMP is first designed as a reference configuration. Subsequently, the PMOS differential pair amplifier is scaled by adjusting the number of transistor fingers to achieve comparable bias currents and overall power consumption.

TABLE II. Design Parameters of Two-Stage OPAMPs with NMOS and PMOS Differential Pairs before Irradiation and under TID Stress (125 krad)

Parameter	NMOS diff. pair		PMOS diff. pair	
	Pre-TID	Post-TID	Pre-TID	Post-TID
Input-stage g_m (μS)	110	117	126	130
Second-stage g_m (μS)	353	359	672	685
First-stage tail current (μA)	32.5	36.8	32.9	34.9
Second-stage drain current (μA)	67.7	75.4	69.8	72.9

The number of fingers of the transistors employed in each amplifier is summarized in Table I. In addition, key small-signal and bias parameters, including the transconductance and bias currents of the first and second stages, are listed in Table II for both pre-irradiation and post-TID conditions. These parameters provide insight into how the adopted threshold-voltage shifts modify the operating point of each amplifier and serve as a basis for interpreting the performance variations discussed in the following section. It should be noted that Table II reflects the operating-point changes obtained under the adopted threshold-voltage-shift-based model. In actual irradiated devices, additional TID-induced effects, such as mobility degradation and other secondary mechanisms, may further modify the transconductance and bias current. Therefore, the values in Table II should be interpreted as first-order circuit-level indicators rather than as a complete representation of all TID-induced parameter variations.

III. SIMULATION RESULTS AND DISCUSSION

Circuit-level simulations were carried out to evaluate the impact of TID effects on the two-stage OPAMPs employing NMOS and PMOS differential input pairs. All simulations were performed under identical biasing and loading conditions, and the results obtained after TID exposure corresponding to 125 krad (SiO_2) are compared with the pre-irradiation baseline.

Fig. 3 illustrates the bode plots of the two amplifier configurations before irradiation and under TID stress. In both amplifiers, TID exposure causes limited changes in the overall frequency-response shape, although noticeable reductions in low-frequency gain are observed. These changes reflect the impact of threshold-voltage shifts on the operating point and small-signal parameters of the transistors, rather than a drastic alteration of the overall frequency response characteristics. In the NMOS differential pair amplifier, the DC gain decreases from 95.9 dB to 91.4 dB after TID exposure. The PMOS differential pair amplifier exhibits a larger reduction in DC gain, decreasing from 91.4 dB to 85.3 dB under the same TID condition. Although the magnitude of DC-gain degradation differs between the two architectures, both amplifiers maintain stable frequency responses without severe distortion or instability. Table III summarizes the key performance metrics of both amplifiers before irradiation and under TID stress of 125 krad. As also

indicated by Table II, both amplifiers exhibit slight increases in transconductance and bias current after TID exposure, indicating that the operating points of both stages are shifted under the adopted TID condition. Despite the reduction in DC gain, the gain-bandwidth product (GBW) remains nearly unchanged for both amplifier configurations. These results suggest that the slight increase in transconductance after TID exposure is accompanied by a reduction in effective output resistance, so that the low-frequency gain decreases while the GBW is largely preserved. In a Miller-compensated two-stage OPAMP, the dominant pole is mainly determined by the RC time constant at the high-impedance first-stage node. After TID exposure, the operating-point shift changes the small-signal parameters and reduces the effective resistance at this node, while the compensation capacitance remains unchanged. Consequently, the corresponding time constant decreases, shifting the dominant pole to a higher frequency and increasing the bandwidth after TID exposure. This behavior is consistent with the general relation in a Miller-compensated two-stage OPAMP, where the DC gain is determined by both transconductance and output resistance, whereas the GBW is primarily governed by the effective transconductance and compensation capacitance. The phase margin exhibits a modest decrease after TID exposure, with the NMOS differential pair amplifier changing from 58° to 54°, while the PMOS differential pair amplifier shows a smaller variation from 74° to 72°. Since the overall topology and Miller compensation network are unchanged, the pole-zero structure is not drastically disturbed, and both designs remain sufficiently stable after TID exposure. The power consumption of both amplifiers increases after TID exposure, consistent with the increase in bias currents summarized in Table II.

TABLE III. Simulated Performance of Two-Stage OPAMPs with NMOS and PMOS Differential Pairs before Irradiation and under TID Stress

Parameter	NMOS diff. pair		PMOS diff. pair	
	Pre-TID	Post-TID	Pre-TID	Post-TID
DC gain (dB)	95.9	91.4	91.4	85.3
Bandwidth (Hz)	344	475	481	967
Phase margin (deg)	58	54	74	72
GBW (MHz)	13.5	13.6	19.7	20.0
Power (μW)	187	215	185	194

The NMOS differential pair amplifier exhibits a larger increase in power consumption, rising from 187 μW to 215 μW, whereas the PMOS differential pair amplifier increases from 185 μW to 194 μW under the same TID condition. This trend can be associated with the larger effective threshold-voltage perturbation applied to NMOS devices, which leads to a more pronounced change in operating current. To further interpret these trends, Table II lists the transconductance and bias current values of the first and second stages before and after TID exposure. Although both designs experience changes in transconductance and bias current following TID-induced threshold-voltage shifts, the resulting variations in DC gain, phase margin, and power consumption differ depending on the input differential pair configuration. In particular, the larger DC-gain reduction observed in the PMOS differential pair amplifier indicates that gain degradation is not determined by current increase alone. Rather, the post-TID gain is governed by the combined changes in transconductance and effective output resistance, and these quantities are affected differently in the two amplifier configurations. These results highlight that the choice of NMOS or PMOS input differential pairs influences how TID-induced operating-point shifts propagate to circuit-level performance, even when identical transistor dimensions and comparable power consumption are maintained.

Overall, the simulation results show that TID exposure at 125 krad does not lead to functional failure of the two-stage OPAMPs investigated. Key small-signal performance metrics, including DC gain, bandwidth, and phase margin, exhibit moderate changes after TID exposure, while both NMOS- and PMOS-input differential pair configurations remain within stable operating ranges. In contrast, changes in power consumption are more evident, with the NMOS differential pair amplifier showing a relatively larger increase compared to the PMOS differential pair design. These observations indicate that, under the considered TID condition, device degradation primarily manifests as changes in bias current and power consumption, while the overall frequency-domain performance of both amplifiers remains largely preserved.

IV. CONCLUSION

This work investigated the impact of TID effects on two-stage OPAMPs employing NMOS and PMOS differential input pairs. By applying previously reported TID-induced threshold voltage shifts for a 180-nm CMOS process at the circuit level, a controlled comparison between the two input architectures was performed under identical design constraints. Simulation results under a TID condition of 125 krad (SiO_2) indicate that both amplifier configurations maintain stable operation without functional failure. While DC gain, bandwidth, and phase margin exhibit only noticeable but non-critical changes after TID exposure, power consumption shows a more noticeable change, with the NMOS differential pair amplifier exhibiting a relatively larger increase. These results suggest that, under the considered TID condition, device degradation is more prominently reflected in power-related characteristics than in small-signal frequency-domain performance.

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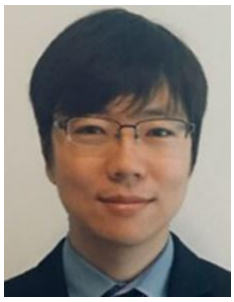

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