A 2-Level Buck Converter Using Adaptive ON/OFF-Time Control for Frequency-Stable Operation

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***Abstract* - This paper presents an adaptive ON/OFF-time (AOOT) control technique for a 2-level buck converter designed in a 180-nm BCD technology. Conventional adaptive on-time (AOT) control provides a simple comparator-based structure; however, its fixed on-time operation inherently results in switching-frequency variation and ripple-dependent behavior, which can lead to sub-harmonic oscillation under wide operating conditions. The proposed AOOT scheme adaptively generates both ON- and OFF-time according to the input and output conditions, thereby enabling direct regulation of the switching period and reducing ripple-dependent instability associated with conventional AOT control under the simulated operating conditions, without requiring a complex compensation network. A 1-MHz buck converter is evaluated in simulation with a 2.5-V input, supporting a wide output-voltage range from 0.5 to 2.0 V and a maximum load current of 2.5 A (5-W output power). Simulation results demonstrate that the proposed AOOT control maintains a near-target 1-MHz switching period under the representative simulated load and output voltage conditions, while achieving predictable steady-state operation. The proposed AOOT adaptively generates both ON- and OFF-time according to operating conditions, enabling direct regulation of the switching period while reducing the dependence on output-ripple-based retriggering without high-order compensation or ripple-injection circuits.**

***Keywords*— adaptive ON/OFF Time control, buck converter, comparator-based control, sub-harmonic oscillation, switching-frequency stability**

I. INTRODUCTION

Buck converters are widely employed in low-voltage power-management applications owing to their high efficiency and simple structure. Conventional voltage-mode (VM) and current-mode (CM) pulse width modulation (PWM) control schemes regulate the output voltage using an error amplifier (EA) and a ramp-based modulator, as shown in Fig. 1(a) [1].

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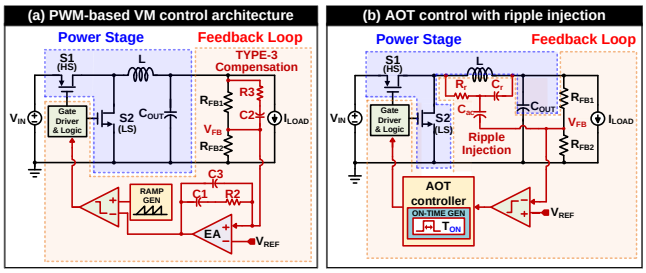

Fig. 1. Conventional buck converter control schemes: (a) PWM voltage-mode control with compensation, (b) AOT control with ripple injection

To ensure loop stability over wide operating conditions, high-order compensation networks such as Type-III compensators are typically required, increasing circuit complexity and passive component count [2]. Adaptive On-time (AOT) control has been introduced to reduce this complexity by eliminating fixed-frequency oscillators and high-order compensation networks [3]. As illustrated in Fig. 1(b), AOT employs a comparator-based structure that utilizes output-voltage ripple to trigger switching events, inherently combining PWM and pulse frequency modulation (PFM) characteristics [4]. However, with low-ESR output capacitors, insufficient ripple can lead to unstable comparator operation and sub-harmonic oscillation [5]. Although ripple-injection techniques can enhance stability, they require additional circuitry and passive components, leading to increased area and cost [6], [7].

To overcome these limitations, this paper proposes an adaptive ON/OFF-time (AOOT) control technique for a 2-level buck converter [8]. The proposed AOOT adaptively generates both ON- and OFF-time according to operating conditions, enabling direct regulation of the switching period without high-order compensation or ripple-injection circuits [9]. Simulation results in a 180-nm BCD technology verify stable frequency operation over wide operating conditions and a peak simulated efficiency of 92.51%.

II. CONVENTIONAL AOT CONTROL AND LIMITATIONS

A. Operation of a 2-level buck converter

Fig. 2 shows a conventional 2-level buck converter employing AOT control. As illustrated in Fig. 2(a), the converter consists of a 2-level power stage, a feedback

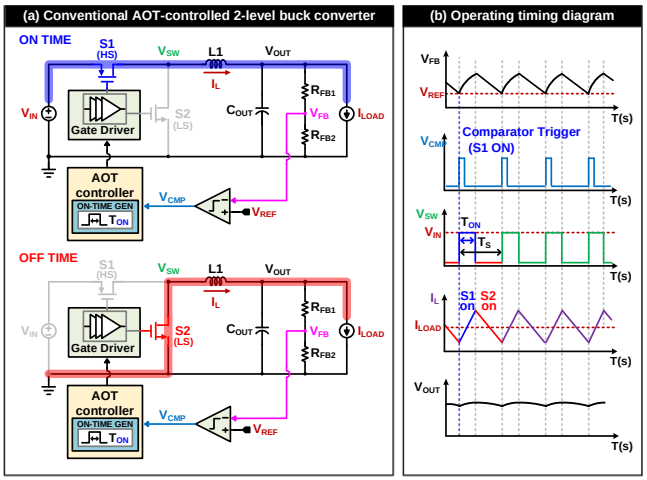

Fig. 2. Conventional AOT-controlled 2-level buck converter (a) block diagram, (b) operating timing diagram

network, a comparator, an ON-time generator, and a gate driver with dead-time control. The output voltage is sensed and compared with a reference to generate the high-side (HS) and low-side (LS) gate signals. Fig. 2(b) presents the timing diagram. When the comparator is triggered, the HS switch turns on for a predefined ON-time, followed by LS conduction after a dead-time interval, allowing the inductor current to decrease and supply the load. Under steady-state and ideal conditions, the inductor volt-second balance yields

$$(V_{IN} - V_{OUT})T_{ON} = V_{OUT}T_{OFF} \quad (1)$$

leading to,

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \approx \frac{V_{OUT}}{V_{IN}} \quad (2)$$

These equations define the fundamental operating point of the buck converter and serve as the basis for the subsequent control analysis.

B. Conventional AOT control principle

Fig. 3 illustrates the operating principle of conventional AOT control. Unlike fixed-frequency PWM control, AOT does not explicitly define the switching period; switching is triggered by a comparator event, and only the ON-time is directly generated by the controller [10].

In conventional AOT implementations, the ON-time generator incorporates input-voltage feedforward, such that the ON-time is proportional to the ratio of the output voltage to the input voltage. Based on the steady-state volt–second balance of an ideal buck converter in (2) and assuming a nominal switching period T_{SW}, the ON-time is given by

$$T_{ON} = D \cdot T_{SW} = T_{SW} \cdot \frac{V_{OUT}}{V_{IN}} \quad (3)$$

This relationship is widely used in practical AOT controllers [11], which commonly implement the ON-time generator using a voltage-to-current conversion of V_{IN}, resulting in

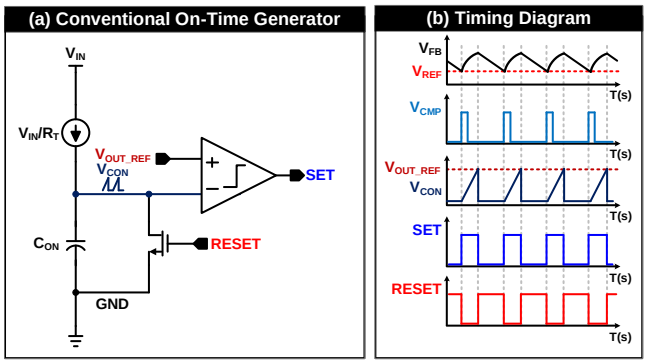

Fig. 3. Conventional AOT control mechanism (a) On-time generator (b) timing diagram.

$$T_{ON} = K \cdot \frac{V_{OUT}}{V_{IN}} \quad (4)$$

where K corresponds to the nominal switching period.

As shown in Fig. 3(b), when the comparator is triggered, the HS switch is turned on for the duration of T_{ON}, after which the converter remains in the OFF state until the next triggering event. Consequently, only the ON-time is explicitly controlled in conventional AOT schemes, while the OFF-time and switching period are implicitly determined by the system dynamics [12].

C. Switching-frequency variation due to parasitic effects

Although the ON-time expression in (4) includes input-voltage feedforward, the switching frequency is not strictly fixed in practice due to parasitic resistances in the power stage. Considering the on-resistances of the HS and LS switches and the inductor DC resistance (DCR), the inductor voltage during the HS and LS conduction intervals is given by

$$V_{L,ON} = V_{IN} - V_{OUT} - I_L(R_{HS} + R_{DCR}) \quad (5)$$

and

$$V_{L,OFF} = -V_{OUT} - I_L(R_{LS} + R_{DCR}) \quad (6)$$

respectively, resulting in load-dependent variations of the inductor current slope [13]. As the load current increases, the parasitic voltage drops increase the magnitude of the inductor current slope, which accelerates the comparator retriggering based on output-voltage ripple. Consequently, the switching frequency increases with load current in conventional AOT-controlled converters [11]. This parasitic- and load-dependent frequency variation complicates frequency planning and causes spectral spreading, especially over wide load-current ranges.

D. Sub-harmonic oscillation and ripple-injection

A fundamental limitation of conventional AOT control is its reliance on output-voltage ripple for stable comparator operation. When low-ESR output capacitors are used, insufficient ripple can cause irregular switching and sub-

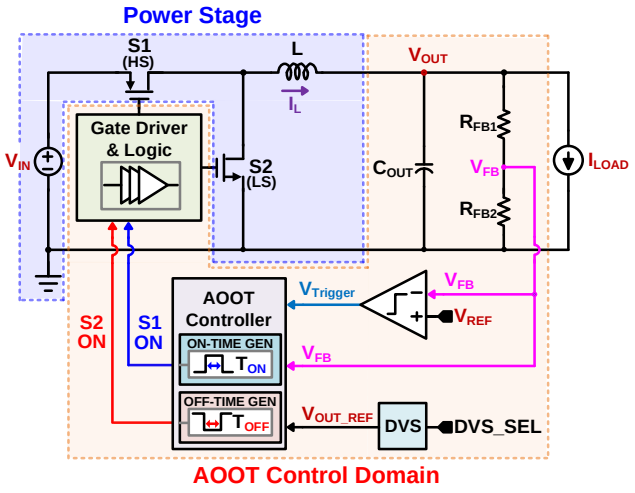

Fig. 4. Top block diagram of proposed AOOT buck converter

harmonic oscillation in certain operating regions [14]. To mitigate this issue, ripple-injection techniques are commonly employed to artificially enhance the sensed ripple. However, this approach requires additional circuitry and passive components, increasing silicon area and design complexity [15]. Moreover, the switching frequency remains implicitly determined and sensitive to operating conditions, motivating the need for an alternative control approach with more predictable behavior.

III. PROPOSED ADAPTIVE ON/OFF TIME CONTRL

A. Top architecture of the proposed AOOT Converter

Fig. 4 shows the block diagram of the proposed AOOT controlled buck converter. The system consists of a 2-level buck power stage, a feedback network, a comparator, adaptive ON- and OFF-time generation blocks, and a gate driver. In addition to the sequential ON- and OFF- time generators, the proposed AOOT controller includes a load-regulation feedback path. This path senses the output-voltage error and compensates the internal reference used for timing generation so that the effective ON/OFF timing can be adjusted according to the output-voltage regulation. Unlike conventional AOT control, which defines only the ON-time, the proposed AOOT explicitly generates both ON- and OFF-time intervals, allowing the switching period to be directly determined by design.

B. Adaptive ON-time generation

As illustrated in Fig. 5(a), the proposed AOOT control generates the ON-time using a charge-based timing mechanism. An EA produces a charging current I_{CON} proportional to the input voltage V_{IN}, which charges the timing capacitor C_{ON} and increases the capacitor voltage V_{CON} linearly. The ON-time is defined as the interval required for V_{CON} to reach a threshold voltage V_{THON}, and is given by

$$T_{ON} = \frac{C_{ON} \cdot V_{THON}}{I_{CON}} \quad (7)$$

Since I_{CON} depends on V_{IN}, the ON-time is adaptively adjusted according to the input-voltage condition, satisfying the volt-second balance requirement.

C. Adaptive OFF-time generation

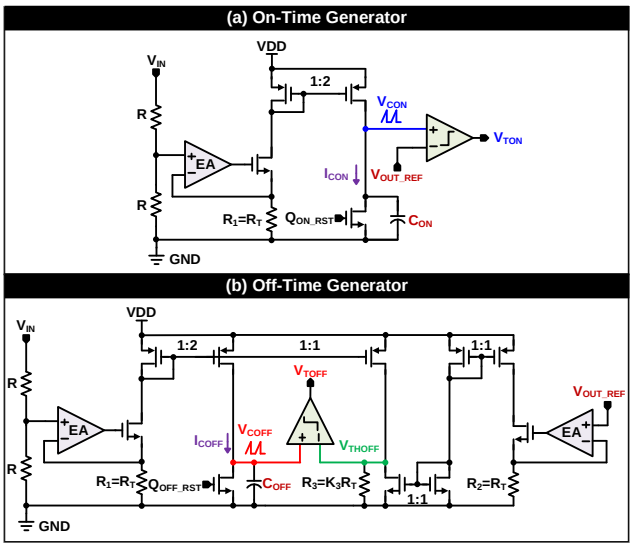

Fig. 5. Schematic of the proposed adaptive ON- and OFF-time generation circuits (a) On-time generator (b) Off-time generator

After the ON-time interval, the OFF-time is generated using an independent charge-based timing mechanism, as shown in Fig. 5(b). A separate EA generates a charging current I_{COFF}, which charges the timing capacitor C_{OFF} until the capacitor voltage reaches the threshold V_{THOFF}.

The resulting OFF-time is given by

$$T_{OFF} = \frac{C_{OFF} \cdot V_{THOFF}}{I_{COFF}} \quad (8)$$

By explicitly generating the OFF-time without relying on output-voltage ripple, the proposed AOOT control eliminates ripple-based retriggering inherent in conventional AOT schemes. Accordingly, the switching period is explicitly defined as

$$T_S = T_{ON} + T_{OFF} \quad (9)$$

making the switching frequency a deterministic design parameter. As illustrated in Fig. 6, the ON- and OFF-time generators operate sequentially to ensure predictable switching behavior. Since the proposed AOOT controller explicitly generates both the ON-time and OFF-time intervals, the next switching transition is not directly determined by a small output-ripple crossing as in conventional AOT control. Instead, the switching period is primarily defined by the sequential timing intervals, TSW = TON + TOFF. Therefore, the proposed AOOT scheme reduces the dependence on output-ripple-based retriggering and mitigates the susceptibility to ripple-dependent sub-harmonic behavior under the simulated operating conditions. Instead, the switching period is primarily defined by the sequential timing intervals of ON-time and OFF-time. Therefore, the proposed AOOT control reduces the dependence on output-ripple amplitude and mitigates the

susceptibility to ripple-dependent sub-harmonic behavior under the simulated operating conditions.

Although the ON- and OFF-time intervals are generated sequentially, the proposed AOOT controller does not operate as an open-loop timing generator. The output voltage is continuously monitored through the feedback path, and the load-regulation circuit generates an error-dependent internal reference. The error signal can be expressed as

$$V_{ERR} = V_{REF} + V_{OUT} \quad (10)$$

$$V_{REF,INT} = V_{REF} + KLR(V_{REF} - V_{OUT}) \quad (11)$$

where KLR denotes the load-regulation gain. When VOUT decreases below the target value, VERR becomes positive and $V_{REF,INT}$ is increased, which increases the effective delivered energy by extending the ON-time and/or reducing the OFF-time. Conversely, when V_{OUT} rises above the target value, the feedback comparator does not issue additional switching action until the output voltage returns toward the target level. Therefore, a timing-ratio mismatch does not accumulate as an unbounded energy error over successive cycles; instead, the load-regulation feedback path provides negative feedback that limits the output-voltage drift under the designed timing range and simulated operating conditions.

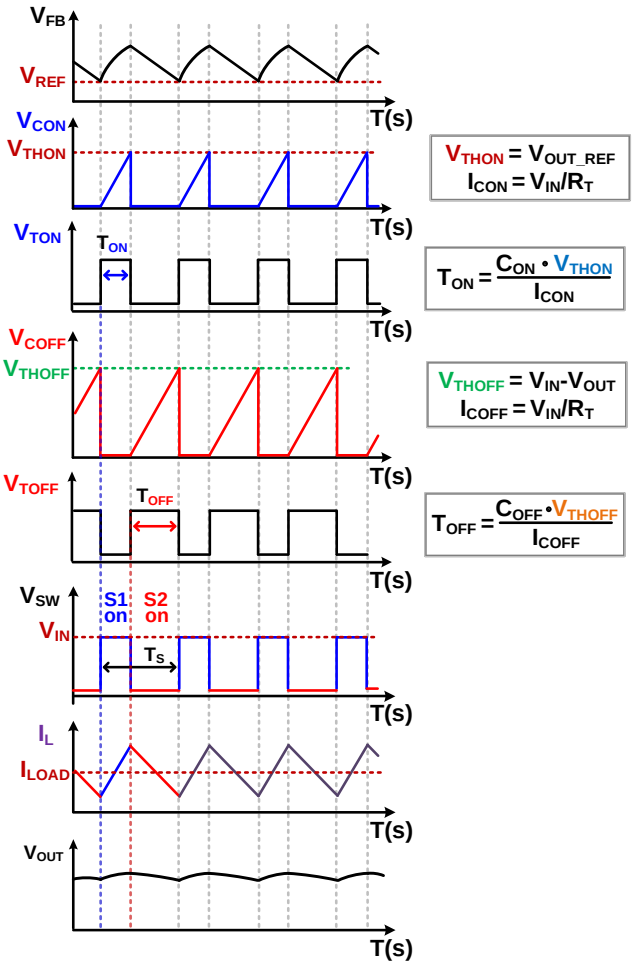

Fig. 6. Timing diagram and operating principle of the proposed AOOT-controlled buck converter

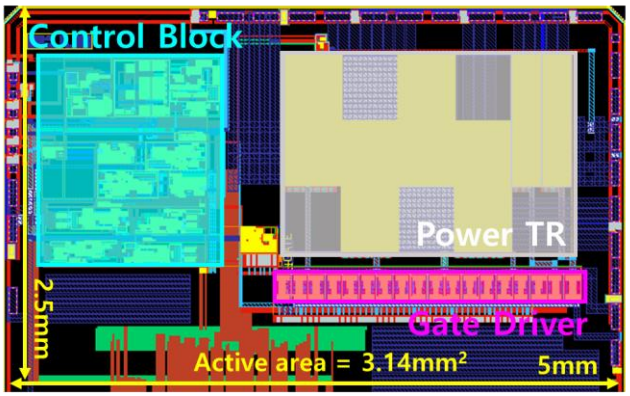

Fig. 7. Layout of the proposed AOOT-controlled 2-level buck converter implemented in a 180-nm BCD process.

IV. SIMULATION RESULTS

A. Proposed 2-level AOOT buck converter

The circuit-level simulations were performed using the main off-chip output-filter components specified as follows. The output inductor and output capacitor were set to L=4.7μH and C_{OUT}=10 μF, respectively. The dc winding resistance of the inductor was set to R_{DCR}=16.5mΩ. The output capacitor was modeled as a 10-μF MLCC with R_{ESR}=20 mΩ. Unless otherwise noted, the converter was evaluated with V_{IN}=2.5V, V_{OUT}=0.5–2.0V, and I_{LOAD}=0.1–2.5 A.

Fig. 7 shows the layout of the proposed AOOT-controlled 2-level buck converter implemented in a 180-nm BCD process. The layout consists of a control block including the AOOT timing generators, a power stage, and a gate driver.

The control block integrates the comparator and adaptive ON- and OFF-time generation circuits, while the gate driver provides non-overlapping HS and LS gate signals. The total active area of the converter is 3.14 mm^2, including both the control circuitry and power-stage devices. The layout confirms that the proposed AOOT control can be realized with a compact structure without additional ripple-injection or complex compensation circuits.

B. Simulation results under wide load conditions

The present work focuses on the steady-state switching-period generation and frequency behavior of the proposed AOOT control. Accordingly, the simulation results in Figs. 8 and 9 are used to verify deterministic ON/OFF timing operation under representative light- and heavy-load steady-state conditions.

Fig. 8 and Fig. 9 show the simulation waveforms of the proposed AOOT controlled buck converter under light-load (I_{LOAD} = 0.1 A) and heavy-load (I_{LOAD} = 2.5 A) conditions, respectively. For both cases, V_{OUT} = 0.5 V and 2.0 V are evaluated. The waveforms include the AOOT-generated ON signal, OFF signal, switching-node voltage (V_{SW}), inductor current (I_L), and output voltage (V_{OUT}).

The light- and heavy-load simulation waveforms in Figs. 8 and 9 verify that the proposed AOOT timing generator maintains a near-target 1-MHz switching period under the representative evaluated conditions. Therefore, the

presented results support the deterministic timing behavior of the proposed AOOT scheme under the selected light- and heavy-load cases, rather than implying an exhaustive load-sweep frequency-deviation characterization.

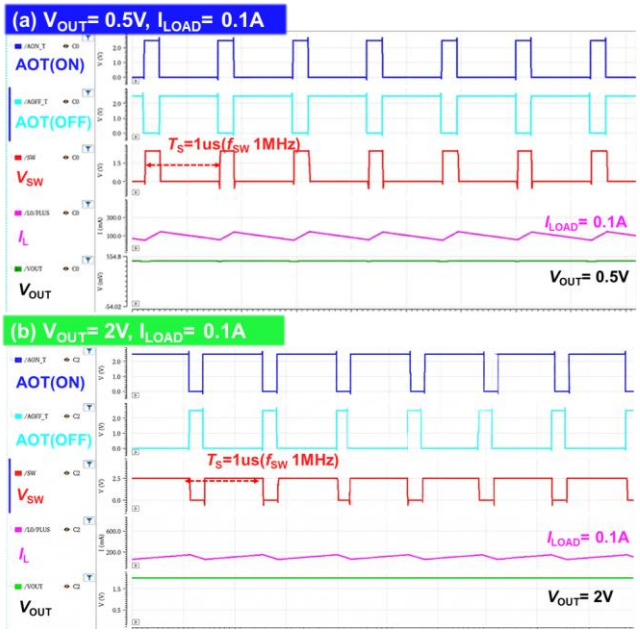

Fig. 8. Simulation waveforms V_{OUT} = 0.5 V and 2.0 V under a light-load condition (I_{LOAD} = 0.1 A).

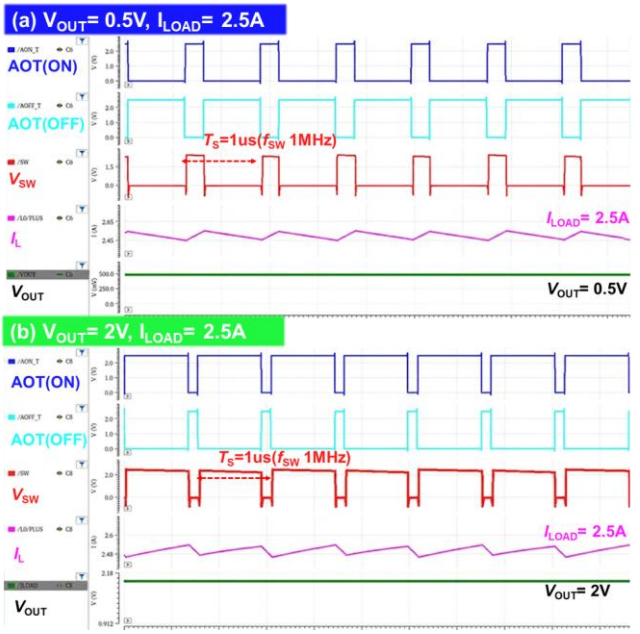

Fig. 9. Simulation waveforms V_{OUT} = 0.5 V and 2.0 V under a heavy-load condition (I_{LOAD} = 2.5 A).

With the selected output-filter components, the inductor ripple current is approximately 85mApp at the representative V_{OUT}=0.5V and 2.0 V conditions. This corresponds to an ESR-induced ripple of approximately 1.7mVpp and a capacitive ripple of approximately 1.1mVpp, resulting in an estimated output ripple of approximately 2.8mVpp. Within the evaluated output-voltage range, the estimated worst-case ripple occurs near V_{OUT}=1.25V and is approximately 4.3mVpp. These values clarify the output-ripple magnitude used in the simulations and support the discussion of ripple-dependent behavior.

Under heavy-load conditions, the inductor current magnitude increases as expected; however, the switching behavior remains deterministic with well-defined timing intervals. Notably, the switching frequency remains constant across both load and output-voltage conditions, verifying that the switching period is explicitly defined by the AOOT timing mechanism rather than being implicitly determined by ripple-dependent retriggering. The representative light- and heavy-load simulations show that the output voltage remains regulated without cumulative drift while the AOOT-generated ON/OFF signals maintain a regular sequential timing pattern. This behavior supports that the proposed load-regulation-assisted AOOT timing prevents successive-cycle energy-error accumulation under the simulated conditions.

C. Efficiency performance

Fig. 10 shows the simulated efficiency of the proposed converter as a function of load current at V_{IN} = 2.5 V. The converter supports a maximum output power of 5 W and achieves a peak simulated efficiency of 92.51% at V_{OUT} = 2.0 V and I_{LOAD} = 0.7 A.

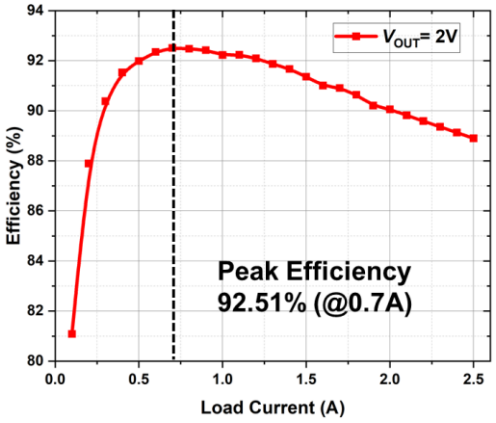

Fig. 10. Simulation efficiency versus load current

Table 1. Performance Comparison with Prior AOT/COT-Based Buck Converters

	TPEL 2015 [5]	TPEL 2019 [6]	TCAS-I 2022 [8]	This Work
Process	180nm CMOS	180nm CMOS	180nm CMOS	**180nm BCD**
Topology (Control Scheme)	AOT w/ SLCC & DTW	Analog Time-Optimized OTC	AOT (V^2 Control)	**Adaptive ON/OFF-Time (AOOT)**
V_{IN} (V)	2.7–3.6 V	3.3 V	2.7–4.7 V	**2.5 V**
V_{OUT} (V)	1.0–1.2 V	0.6–1.2 V	1.6 V	**0.5–2.0 V**
Max. I_{LOAD} (A)	1.1 A	1.25 A	0.1 A	**2.5 A**[a]
Switching Frequency (MHz)	1	1.5	4	**1 MHz**[b]
Freq. Variation	Reduced (±2.6%)	Load dependent	Stable (Const.)	**Stable (Const.)**
Peak Efficiency, η (%)	88.2%	90.2%	92.1%	**92.51%**[c]
Inductor (uH)	N/A	1	4.7	**4.7**
Capacitor (µF)	N/A	4.7	4.7	**10**

Footnotes:
(a) Simulated maximum load current
(b) Nominal switching frequency
(c) Simulated peak efficiency

Table I summarizes the key simulated specifications and performance metrics. Table 1 compares the performance of the proposed AOOT-controlled buck converter with prior AOT/COT-based designs. The referenced works are based on silicon measurement results, whereas this work reports simulation results. As summarized in Table 1, the proposed converter maintains a constant switching frequency of 1 MHz over wide load and output-voltage conditions, unlike conventional AOT/COT implementations that exhibit load-dependent frequency variation. Although the peak efficiency is comparable to that of prior designs, the proposed AOOT scheme achieves predictable frequency behavior without requiring ripple-injection or complex compensation circuits. The use of practical passive component values further demonstrates the suitability of the proposed control for compact buck converter applications.

V. CONCLUSION

This paper presented an AOOT control technique for a 2-level buck converter to achieve stable switching-frequency operation with a simple comparator-based architecture. While conventional AOT control adaptively defines only the ON-time and implicitly determines the switching period through ripple-based retriggering, the proposed AOOT scheme reduces the dependence on ripple-based retriggering under the simulated operating conditions while maintaining deterministic ON/OFF timing behavior by explicitly generating both ON- and OFF-time intervals, thereby defining the complete switching period by design. Circuit-level simulation results confirm that the proposed AOOT-controlled buck converter maintains deterministic ON/OFF timing and near-target switching-period operation under the evaluated representative load-current and output-voltage conditions. The converter achieves a peak simulated efficiency of 92.51% using practical passive component values, while reducing the dependence on ripple-based retriggering under the simulated operating conditions. This makes the proposed AOOT control suitable for compact low-voltage power-management applications.

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