A High-Voltage DC-DC Buck Converter with Dual-Parameter Maximum Power Point Tracking for Triboelectric Nanogenerator Energy Harvesting

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Abstract - **This work presents a high-voltage (HV) energy-harvester interface integrated circuit (EHI-IC) designed for efficient energy extraction from triboelectric nanogenerators (TENGs) operating in high-impedance, low-frequency oceanic environments. TENGs produce short-duration, HV pulses with equivalent source resistances in the 2–10 MΩ range, posing challenges for conventional power management circuits. The proposed EHI-IC incorporates a full-bridge rectifier followed by an HV DC-DC buck converter with a dual-parameter maximum power point tracking (MPPT). A voltage-to-current calibration block and a power-to-bit converter provide digital monitoring of input power, enabling dynamic adjustment of the converter duty cycle to maximize power transfer. Zero-current-switching (ZCS) control ensures precise timing of power switches, minimizing reverse current and improving efficiency. Fabricated in a 0.18-µm HV bipolar CMOS-DMOS (BCD) process with a compact 3 mm² footprint, the EHI-IC achieves output voltage between 1.3 and 1.8 V and MPPT efficiencies up to 95.5%. The end-to-end efficiency of EHI-IC achieved 90.4% with a power consumption of 926.8 nW. Experimental and simulation results validate reliable operation for self-powered Internet of Things (IoT) and wearable applications.**

Keywords- **Buck Converter, Energy Harvesting, MPPT, TENG**

I. INTRODUCTION

The growing demand for self-powered electronic systems has intensified research in ambient energy harvesting, providing sustainable alternatives for powering low-power devices and Internet of Things (IoT) applications. Among various ambient sources, including mechanical motion, thermal gradients, solar radiation, radio-frequency (RF) signals, biological energy, and ocean wave energy, which is often referred to as blue energy, is particularly promising. Covering approximately 71% of the Earth's surface and containing 96.5% of its water, oceans represent a vast and renewable energy resource for future technologies.

Multiple renewable energy modalities exist in the ocean, such as wave motion, tidal forces, thermal gradients, and salinity differences. For energy harvesting, devices including thermoelectric generators (TEGs), biofuel cells (BFCs), photovoltaic generators (PVGs), and vibrational energy harvesters (VEGs) have been explored. Among VEGs, triboelectric nanogenerators (TENGs) are especially attractive due to their lightweight design, low cost, scalable fabrication, and compatibility with flexible structures [1], [2].

Fig. 1(a) shows a flexible TENG-based energy harvester designed using fluorinated ethylene propylene (FEP) and polyethylene terephthalate (PET) to capture wave-induced mechanical motion. Fig. 1(b) shows the equivalent circuit model of the TENG [1], and Fig. 1(c) shows the variation in the TENG internal voltage source (V_S) per TENG pair. while Fig. 1(d) depicts its operation based on the contact–separation mechanism.

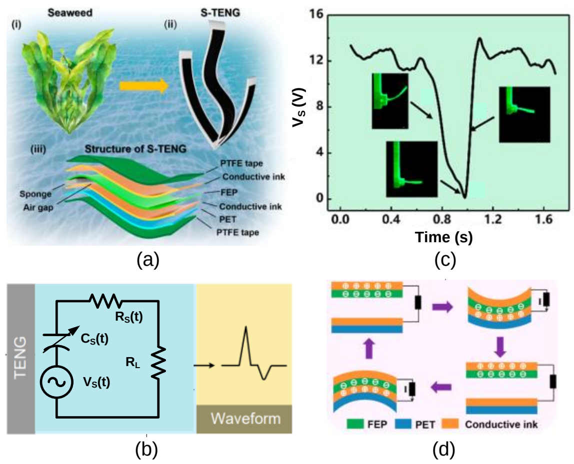

Fig. 1. Flexible TENG-based energy harvester; (a) design for ocean wave energy harvesting [1], (b) equivalent circuit model of the TENG, (c) measured voltage per TENG pair, (d) operating mechanism illustrating charge transfer between FEP and PET layers.

The TENG generates a short-circuit current of approximately 2.5 µA and a peak power of ~10 µW [2], confirming its potential for harvesting low-frequency oceanic vibrations. However, its inherent characteristics, short-duration, high-voltage (HV) pulses and high equivalent resistance (1-10 MΩ) [3], [4] pose challenges for efficient energy extraction using conventional power management circuits.

To address these limitations, HV rectification followed by DC-DC conversion with maximum power point tracking (MPPT) is required. Previous studies have shown that

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pairing electrostatic energy harvesters with full-bridge rectifiers mitigates diode threshold effects, improving overall conversion efficiency [3], [4]. Nevertheless, implementing HV converters in standard CMOS processes is constrained by oxide breakdown and power losses.

Recent advancements highlight the need for ultra-low-power MPPT controllers capable of dynamically matching the converter input impedance to the high source resistance of TENGs [5], [6]. Among existing methods, the fractional open-circuit voltage (FOCV) technique is widely used in TEGs and BFCs due to its simplicity and suitability for high-power-density harvesters. However, FOCV suffers from several limitations, including the requirement for a large sample-and-hold (S/H) capacitor, sampling-related energy losses, and difficulty in fully integrating the circuit on-chip without external components. Moreover, FOCV interrupts power flow to the load (R_L) during the sampling interval, reducing overall system efficiency.

To address these limitations, this work introduces an HV energy-harvester interface IC (EHI-IC) integrating a DC-DC buck converter with a dual-parameter MPPT controller. The proposed mixed-signal MPPT architecture incorporates a compact on-chip sample-and-hold (S/H) circuit tailored to TENG characteristics, enabling continuous power delivery and achieving stable, efficient energy conversion for self-powered IoT and wearable systems.

II. EXPERIMENTS

A. Proposed HV DC-DC buck converter

Fig. 2 shows the schematic of the proposed HV buck converter architecture. The design incorporates a full-bridge rectifier to convert the time-varying TENG output into a regulated DC voltage. Two HV switches (S_{P1} and S_{N1}) control the energy transfer through the inductor (L), generating an output voltage (V_{OUT}) in the 1.8 V range.

The power stage is driven by MPPT control based on pulse-width modulation (PWM), which uses subcircuits, such as buffers, level shifters, and zero-current-switching (ZCS) controllers to ensure reliable operation of the HV converter. The inductor current (I_L) is sensed using a low-pass-filter-based current-to-voltage converter formed by R_{FL} and C_{FL}, as described in [7].

The MPPT controller employs the perturb-and-observe (P&O) algorithm to adaptively tune the ON-time of the S_{P1} gate signal (Φ_{SP1}), enabling the converter to track the maximum power point (MPP) under varying TENG conditions.

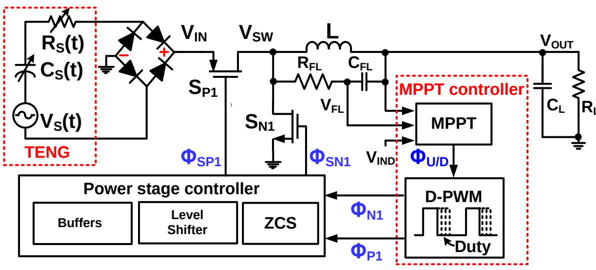


Fig. 2. Block diagram of proposed HV buck converter

B. MPPT operation

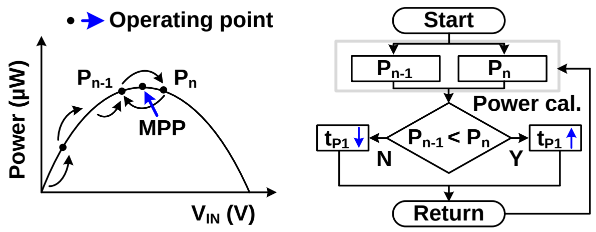
According to the maximum power transfer theorem, source resistance (R_S) must match the input impedance (R_{IN}) to achieve optimal energy extraction. The equivalent R_{IN} is defined in (1), and its full derivation is provided in [6, eq. 17]. In this expression, t_{P1} denotes the ON-time of the Φ_{SP1} pulse, f_{CLK} represents the switching frequency, and β is the voltage ratio between V_{OUT} and V_{IN} of the converter.

$$R_{IN} = \frac{2L}{t_{P1}^2 f_{CLK}(1-\beta)}. \quad (1)$$

The proposed converter dynamically varies the t_{P1} value via PWM, while the remaining parameters remain fixed at their initial values.

Fig. 3(a) shows the P&O-based MPPT operation when the converter is activated for energy harvesting. Operating at the MPP allows the system to achieve the highest MPPT efficiency (η_{MPPT}). The arrow indicates the movement of the operating point, which settles near the MPP during steady-state operation. After reaching steady state, the P&O process introduces small oscillations around the MPP.

Fig. 3(b) presents the simplified MPPT algorithm implemented in the proposed controller. When the MPPT function starts, it calculates the input power (P_{IN}) from the voltage source (V_S) using the clock signal (Φ_{CLK}). The controller compares the previous power sample (P_{n-1}) with the current power value (P_n) and determines whether to increase or decrease the t_{P1} interval. As a result, the R_{IN} is adjusted dynamically, as described in (1), to extract the maximum available power from V_S.



(a) (b)

Fig. 3. (a) Operating point variation on power vs voltage curve, (b) flow chart of the proposed MPPT algorithm.

C. MPPT controller

Fig. 4 presents the detailed block diagram of the proposed HV DC-DC converter, which is divided into an HV side (HVS) and a low-voltage side (LVS). The HVS includes an HV level shifter (HVLS) with a buffer to constantly drive S_{P1}. The HVLS is implemented using a conventional capacitor-coupled structure that converts the low-voltage Φ_{P1} signal into Φ_{SP1} while tracking variations in V_{IN}.

All sub-blocks in the LVS operate at 1.6 V logic (V_{DD} = 1.6 V). Therefore, a voltage scale-down (VSD) circuit is used to reduce the V_{FL}, V_{OUT}, and the switching-node voltage (V_{SW}) to the LVS domain. The voltage difference between V_{OUT} and V_{FL} is proportional to I_L and is represented by V_{SI}, while the scaled version of V_{SW} provides V_{SV}, which reflects V_{IN} when S_{P1} is ON. These signals are generated by the voltage and current calibration (V-I Cal) block, which consists of a differential-amplifier stage that produces V_{SI}

and a voltage-follower stage that generates V_{SV}.

Next, the power-to-bit converter (PBC), enabled by Φ_{EN}, multiplies V_{SV} and V_{SI} to form an 8-bit digital value representing the P_{IN}, denoted as 8-bit Φ_{PBC}. This digital power information is stored in two registers, REG_A and REG_B, which hold information for P_n and P_{n-1} for MPPT operation.

A digital 8-bit comparator (CM_D) evaluates P_n and P_{n-1} values to determine whether the P_{IN} has increased or decreased. Based on this comparison, the CM_D generates a $\Phi_{U/D}$ signal, which is applied to an 8-bit counter. The counter output then updates the pulse-delay controller (PDC), which adjusts the t_{P1} of the control signal Φ_{P1}. The Φ_{CLK} generated by an on-chip oscillator (OSC) and pulse generator synchronizes all stages of the MPPT operation.

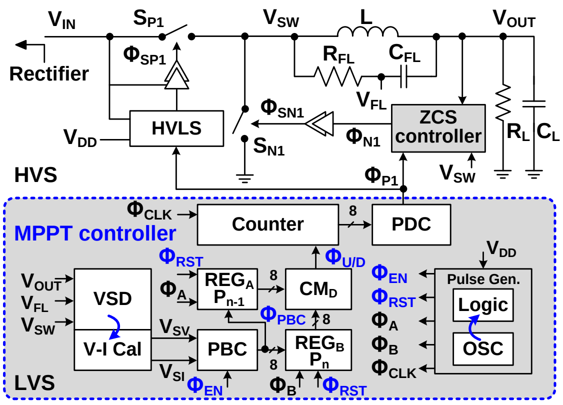


Fig. 4. Block diagram of the proposed HV converter with MPPT controller.

The ZCS controller further improves efficiency by detecting the zero-current condition of I_L using the scaled-down V_{SW} and V_{OUT} signals. After detecting the zero-crossing instant, the controller adjusts the delay of Φ_{N1} to enable efficient energy transfer to the R_L. This implementation follows the design approach reported in previous work [6].

D. Power-to-bit converter (PBC)

Fig. 5(a) presents the schematic of the PBC, which is designed into two functional sections separated by a dashed boundary. The voltage-to-time conversion section and the power-to-bit conversion section. The PBC operates entirely based on the two analog inputs, V_{SV} and V_{SI}, generated by the V-I Cal block. In the voltage-to-time conversion section, the process begins when Φ_{EN} transitions high. This activates the ramp generator through the voltage-to-time conversion control signal (Φ_{VT}). Once enabled, the capacitor (C_{RA}) is charged by the current source (I_{RA}), resulting in the capacitor voltage (V_{RA}) increasing linearly with time. When V_{RA} rises, the comparator continuously evaluates V_{RA} against the reference input V_{SV}. When the comparator detects that V_{RA} has reached V_{SV}, it triggers the D flip-flop to generate the conversion-finish signal (Φ_{FIN}), which subsequently forces Φ_{VT} to transition low. This mechanism ensures that the duration of the Φ_{VT} pulse is determined by the relationship between V_{SV} and the ramp slope set by I_{RA} and C_{RA}.

The power-to-bit conversion section comprises a cross-coupled SR latch, a voltage-controlled delay (VCD) block, and an 8-bit counter. While Φ_{VT} remains high, the SR latch and the VCD block form a positive-feedback timing loop that generates a high-frequency pulse train at Φ_{PB}. This Φ_{PB} signal functions as the clock input to the 8-bit counter during the Φ_{VT} high interval. As a result, the counter output accumulates a number of pulses proportional to the effective product of V_{SV} and V_{SI}, providing a digital representation of the P_{IN} as an 8-bit binary code, denoted Φ_{PBC}.

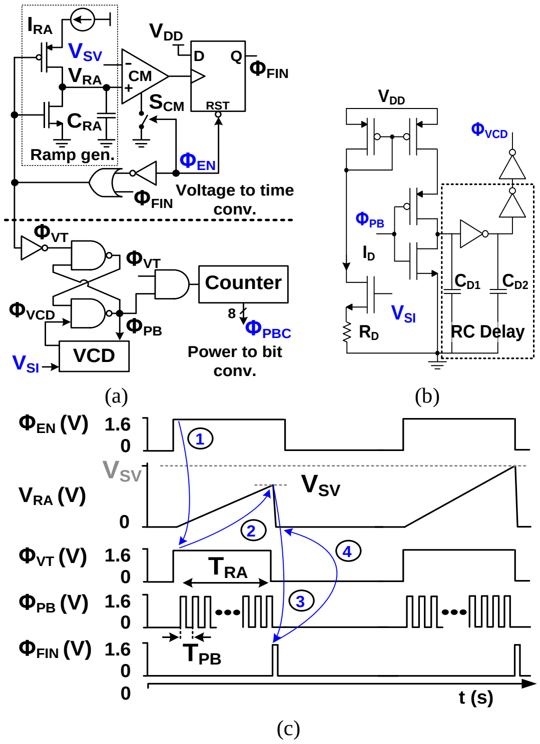


Fig. 5. (a) Schematic of the PBC, (b) voltage-controlled delay (VCD). (c) functional waveforms of the PBC.

Fig. 5(b) shows the internal design of the VCD block, which includes an RC delay network composed of two inverters and two capacitors ($C_{D1,2}$). The effective delay of this RC network is modulated by the V_{SI} level via a source-degeneration configuration comprising a resistor R_D and a MOSFET. When a Φ_{PB} pulse arrives, the VCD block produces a delayed version of the signal at its output (Φ_{VCD}), which then feeds back to the SR latch. Due to the positive feedback loop, the oscillation period (T_{PB}) of Φ_{PB} becomes directly dependent on V_{SI}, enabling analog-dependent frequency modulation.

Fig. 5(c) shows the timing waveform of the PBC, which operates in four major steps. Initially, V_{RA} is discharged to zero while Φ_{EN} is low. Once Φ_{EN} transitions high, V_{RA} ramps upward linearly, and Φ_{VT} becomes high, marking the beginning of the voltage-to-time conversion interval. In the second step, when V_{RA} reaches V_{SV}, the comparator output switches high, forcing Φ_{VT} low through the corresponding logic circuitry. During the entire interval in which Φ_{VT} is high, the duration of this pulse, T_{RA}, can be expressed as (2).

$$T_{RA} = \left(C_{RA} V_{SV}\right) / I_{RA} . \quad (2)$$

At the same time, Φ_{PB} begins to oscillate with a period T_{PB}, which can be approximated by (3). In this expression,

C_{EF} represents the effective capacitance of the RC delay block, and I_D denotes the current flowing through R_D. For simplicity, the current can be expressed as $I_D = (k\ V_{IN})$ due to the source degeneration, where k is a proportionality constant determined by the device parameters and bias conditions.

$$T_{PB} = \left(C_{EF}V_{DD}\right)/I_D = \left(C_{EF}V_{DD}\right)/kV_{IN}. \quad (3)$$

The final Φ_{PBC} is produced by counting the number of oscillation pulses (N) generated during the interval T_{RA}. This relationship is expressed in (4), showing that the pulse count is directly proportional to the P_{IN}.

$$N = \left\lceil \frac{T_{RA}}{T_{PB}} \right\rceil = \frac{kC_{RA}}{C_{EF}I_{RA}V_{DD}} V_{SV}V_{SI}. \quad (4)$$

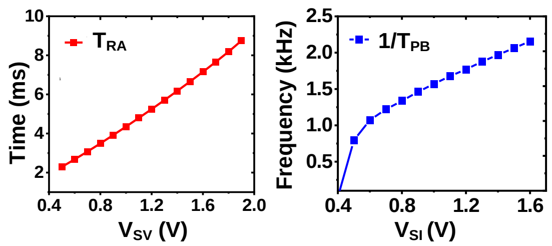
In the third step, the Φ_{FIN} transitions high, indicating the completion of the voltage-to-time conversion. Following this event, Φ_{FIN} enables the discharge path for C_{RA}, bringing V_{RA} back to zero, which marks the fourth step of the PBC operation.

Fig. 6(a) shows the variation of T_{RA} as a function of V_{SV}, demonstrating a relatively linear relationship across the evaluated voltage range. This high linearity ensures that the voltage-to-time conversion accurately represents V_{SV}, which is essential for MPPT operation and dynamic adjustment of the Φ_{SP1} duty cycle.

Fig. 6(b) presents the simulated frequency of Φ_{PB} as a function of V_{SI}. The results show a linear function above approximately 0.5 mV, attributed to the source degeneration operating in the saturation region. This behavior confirms the validity of (3), which is based on the linear approximation of the delay-block current (I_D).

As described in the VSD operation, V_{IN} and I_{IN} are proportional to V_{SV} and V_{SI}, respectively. Therefore, the binary-coded output Φ_{PBC} maintains proportionality to the P_{IN} as expressed in (4). A source-degeneration resistor (R_D = 33 MΩ) is used to enhance linearity further and improve the accuracy of the delay modulation.

These results confirm the relatively linear and robust nature of the proposed MPPT system. The correspondence between V_{SV}, V_{SI}, and the final digital output ensures reliable power tracking and efficient energy conversion, making the proposed approach well-suited for high-impedance energy harvesters.



(a) (b)

Fig. 6. Simulated results of (a) time to voltage conversion as a function of V_{SV}, (b) frequency of the Φ_{PB} as a function of V_{SI}.

III. RESULTS AND DISCUSSIONS

A. Simulation results

Fig. 7 shows the simulation results of the proposed EHI-IC. At the beginning of the operation, the V_{IN} equals the V_S of 36 V. As the MPPT process begins, the duty cycle of the Φ_{SP1} signal is dynamically adjusted. Through this adaptation, V_{IN} gradually converges to 17 V, which corresponds to the MPPT voltage (V_{MPPT}), approximately half of V_S. This stabilization at the expected V_{MPPT} confirms that the proposed MPPT controller effectively identifies and maintains the operating point for maximum power transfer.

In parallel, the Φ_{SN1} signal is regulated by the ZCS controller to suppress reverse leakage current and avoid premature activation of S_{N1}. The controller ensures that S_{N1} turns ON only when the I_L reaches zero, preventing negative current from flowing through load capacitance (C_L) and improving overall conversion efficiency. The simulation results also show that the V_{OUT} of the EHI-IC remains stable at 1.6 V, demonstrating proper buck converter operation under HV input conditions.

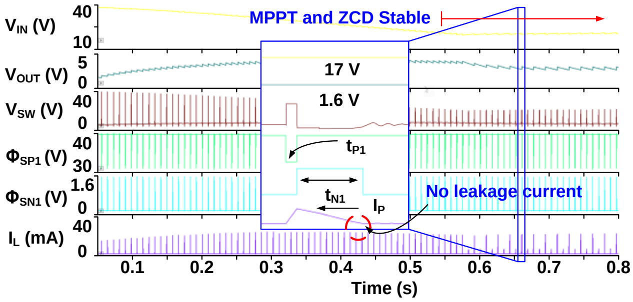


Fig. 7. Simulated overall performance of the EHI-IC.

Collectively, these results validate the capability of the proposed circuit to manage and regulate energy transfer from a high-impedance TENG source while sustaining η_{MPPT}. The combined MPPT and ZCS control enables efficient energy harvesting and stable low-voltage output generation suitable for self-powered systems.

Fig. 8 shows the simulated T_{RA} variation for process corners. Overall results show relatively low dependency on process corner variation. In the TT corners, T_{RA} becomes 5.2 ms.

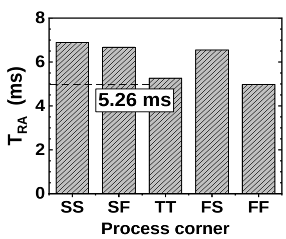


Fig. 8. Simulated process corner for T_{RA} variation at V_{SV} = 1.2 V.

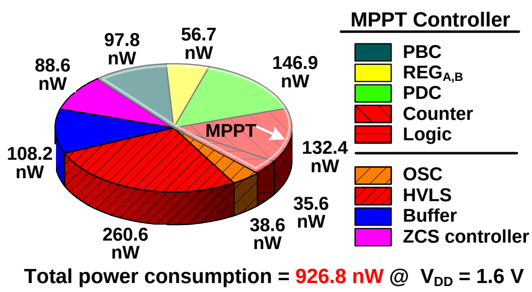


Fig. 9. Power breakdown of each subcircuit in the proposed EHI-IC. V_S = 36 V, R_S = 5 MΩ, R_{OUT} = 100 kΩ.

Fig. 9 shows the power consumption of each sub-circuit included in the EHI-IC. When the EHI-IC is powered with 1V, it consumes 926.8 nW. The power consumption of the MPPT controller, HVLS, and buffers is 969.4, 260.6, and 108.2 nW, respectively.

B. Chip micrograph

Fig. 10 shows the chip micrograph of the fabricated EHI-IC, highlighting the key sub-circuit blocks. The integrated DC-DC buck converter was fabricated using a 0.18-µm HV bipolar CMOS DMOS (BCD) process optimized for HV energy-harvesting applications. The total chip area is 3 mm².

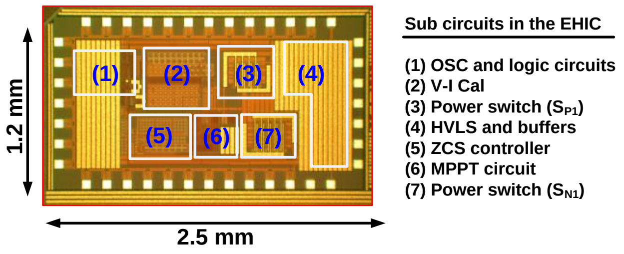


Fig.10. Chip micrograph.

C. Experiment results

Fig. 11 shows the experimental setup used to characterize the fabricated EHI-IC. The chip is mounted on a test board using a chip-on-board assembly, allowing direct electrical connections for accurate measurement. A 4.7 mH off-chip inductor was employed for the DC-DC buck conversion, while bias voltages are supplied to the on-chip oscillator. Two laboratory-grade multimeters are used to measure V_{IN} and V_{OUT} precisely. To evaluate the fabricated EHI-IC, a stable 36 V power supply and a set of resistors ranging from 1 MΩ to 10 MΩ are used to emulate the R_S of the TENG.

The measured V_{MPPT} is 13.5 V at R_S = 5 MΩ, while the regulated V_{OUT} stabilized around 1.3 V. These results confirm the effective operation of both the MPPT circuit and the DC-DC buck converter. The Φ_{CLK} is set to 120 Hz to minimize switching losses and facilitate stable operation of the proposed MPPT circuit.

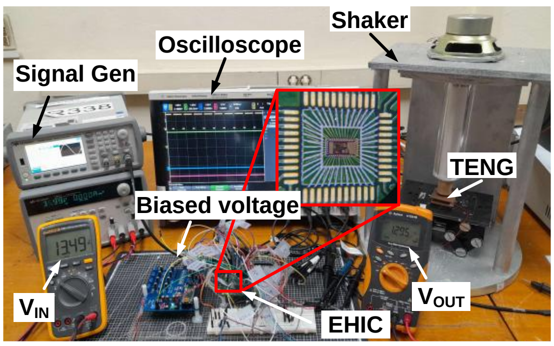


Fig. 11. Experimental setup showing the EHI-IC operation under the test conditions.

Fig. 12 shows the waveforms of Φ_{CLK} and the low-voltage switching signals Φ_{P1} and Φ_{N1} for the S_{P1} and S_{N1} power switches. The $\Phi_{U/D}$ signal exhibits periodic oscillations, indicating that the MPPT controller actively regulates the Φ_{P1} signal to adjust the duty cycle dynamically. This behavior ensures power extraction from the high-impedance source while maintaining efficient converter operation.

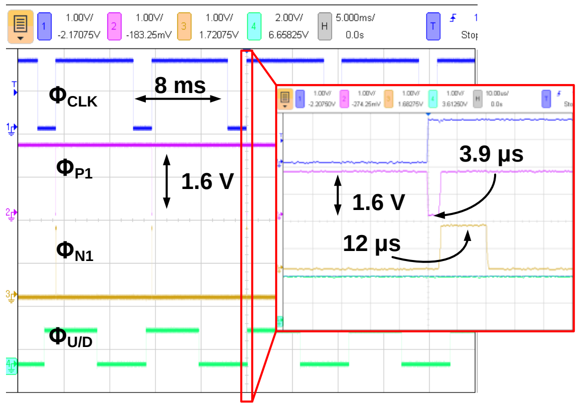


Fig. 12. Measured waveforms of the oscillator and MPPT controlling circuit V_S = 36 V, R_S = 5 MΩ, R_{OUT} = 100 kΩ.

Fig. 13 shows the V_{SW} waveform. When S_{P1} turns ON, V_{SW} rises toward the V_{MPPT}. During energy transfer from the L to the R_L, V_{SW} decreases to zero. These charging and discharging cycles produce ripples at V_{OUT}; however, in steady-state operation, the output voltage remains stable at 1.8 V under optimal load conditions, R_L = 100 kΩ. This behavior demonstrates the effective buck conversion under a high V_{IN} and confirms the reliable operation of the proposed converter.

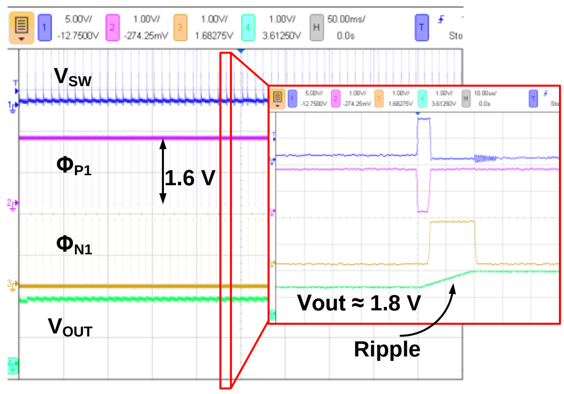


Fig. 13. Measured waveforms of the inductor voltage V_S = 36 V, R_S = 5 MΩ, R_{OUT} = 100 kΩ.

Fig. 14 presents the steady-state performance of the EHI-IC with V_S = 36 V. During MPPT operation, V_{IN} stabilizes around 13.5 V, approximately half of V_S, indicating efficient energy extraction. Using (1) and the measured parameters from Fig. 12, β = 0.13, t_{P1} = 3.9 µs, and f_{CLK} = 120 Hz. R_{IN} is calculated as 5.6 MΩ, closely matching the experimentally measured R_S = 5 MΩ. At the same time, the V_{OUT} remains steady around 1.8 V, confirming the reliable operation of the EHI-IC. These results demonstrate the effectiveness of the proposed converter for efficient energy harvesting from high-impedance sources.

Fig. 15 shows both simulated and experimental η_{MPPT} as a function of the R_S. The results show that η_{MPPT} increases gradually with R_S, reaching peak values of 99.2% in simulation and 95.5% in the experiment at approximately R_S = 5 MΩ. Beyond this point, efficiency decreases due to the

TABLE I. Performance Comparison with Previous Work

Study	[8]	[9]	[10]	This work
Source	TENG	TENG	TENG	TENG
Process (nm)	HV BCD (180)	HV BCD (180)	HV BCD (180)	HV BCD (180)
Converter type	Rectifier + Buck converter	Rectifier + Buck converter	Rectifier + Buck converter	Rectifier + Buck converter
Input voltage (V)	< 70	3.5 – 70	40	35
Impedance range (MΩ)	N.R	2	36	2 - 10
MPPT method	FOCV	FOCV	Analog P&O	Mixed-signal P&O
S/H type	Capacitive	Capacitive	Capacitive	PBC
Die area (mm^2)	5 x 5	2.8 x 0.7	2 x 2	1.2 x 2.5
Peak η_{MPPT} (%)	89.7	98	98.9	95.5
Peak η_{EE} (%)	75.6	52.9	88	90.4

growing mismatch between the converter R_{IN} and the R_S. These findings confirm the effectiveness of the proposed MPPT algorithm in maximizing power extraction from high-impedance energy-harvesting sources.

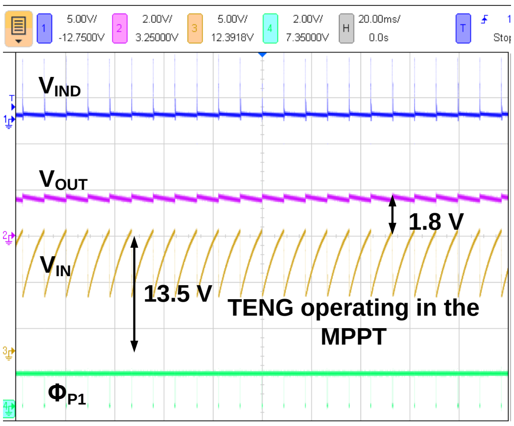


Fig. 14. Measured overall performance of the EHI-IC V_S = 36 V, R_{OUT} = 100 kΩ.

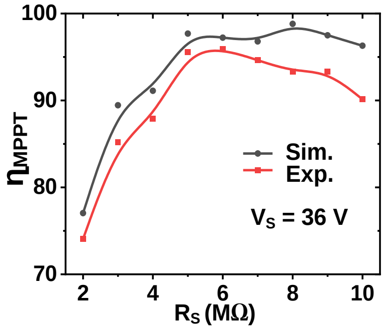


Fig. 15. η_{MPPT} as a function of R_S. V_S = 36 V, R_{OUT} = 100 kΩ.

Fig. 16 shows the simulated end-to-end efficiency (η_{EE}) as a function of output power P_{OUT}. To evaluate the η_{EE}, the R_S = 5 MΩ was chosen based on the results shown in Fig. 15. Also, V_S = 36 V were chosen, considering the CMOS breakdown voltage. As the V_S increases, η_{EE} rises due to higher available power. The peak η_{EE} value of 90.4% occurs at 36 V, yielding a P_{OUT} of 60 µW.

Table I shows the performance of the proposed EHI-IC compared with recent TENG energy-harvesting interfaces. Unlike prior designs that primarily rely on FOCV-based MPPT with capacitive S/H circuits, the proposed mixed-signal P&O method enables accurate impedance tracking over a wide R_S range (2-10 MΩ). Despite using a significantly smaller die area (1.2 × 2.5 mm²), the proposed system achieves a measured η_{MPPT} of 95.5% and η_{EE} of 90.4%, demonstrating competitive performance relative to larger and more complex analog implementations. Moreover, the integration of the on-chip mixed-signal MPPT and HV buck converter demonstrates the architecture's effectiveness in handling HV TENG outputs while maintaining stable, efficient energy transfer for low-power IoT applications.

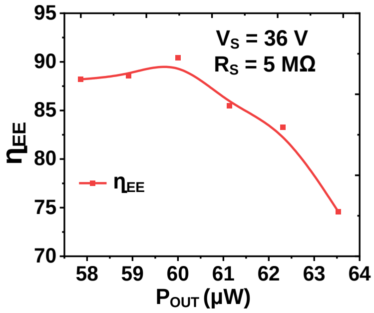


Fig. 16. Measured η_{EE} as a function of P_{OUT}. R_S = 5 MΩ, V_S = 36 V.

IV. CONCLUSION

A HV DC-DC buck converter EHI-IC was successfully designed, fabricated, and evaluated for efficient power extraction from high-impedance sources such as TENGs. The proposed architecture combines PWM-based MPPT with ZCS-controlled switching to dynamically adjust the duty cycle of the HV switch and prevent reverse current, ensuring stable energy transfer. Experimental results demonstrate that V_{IN} stabilizes near the maximum power point, while V_{OUT} remains between 1.3 and 1.8 V, confirming reliable buck conversion. The PBC and V-I Cal circuits provide an accurate digital representation of P_{IN}, enabling precise MPPT operation. Measured efficiencies reached up to 95.5% at R_S = 5 MΩ, closely matching simulation predictions. Overall, the results validate the robustness, linearity, and effectiveness of the proposed EHI-IC for high-efficiency energy harvesting from high-impedance sources.

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