Fill Factor Preservation in Front-Side Illuminated Single-Photon Avalanche Diode Arrays Using External Routing

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Abstract – **In recent years, Back-Side Illumination (BSI) has emerged as a prominent configuration for Single-Photon Avalanche Diode (SPAD) arrays, offering excellent photon detection probability (PDP). However, this comes at the cost of high fabrication complexity, reduced yield, and even degraded PDP at certain wavelengths. As a result, Front-Side Illumination (FSI), which implements the SPAD in a standard CMOS process, remains a practical and attractive alternative. In FSI-based SPAD systems, components such as quenching circuits, counters, and TDCs typically reduce the fill factor of individual pixels or the overall array. This work proposes a novel routing scheme that enables area-intensive digital components to be placed outside the array boundary. The proposed structure preserves the fill factor at both the pixel level (4.48%) and the array level (5.19%), compared to the intrinsic SPAD fill factor (5.84%), while successfully demonstrating full system functionality through pattern projection measurements.**

Keywords—**Single Photon Avalanche Diode, Front-Side Illumination, Fill-Factor Preservation**

I. INTRODUCTION

SPAD is a device capable of detecting a single photon, as its name indicates. SPAD operates above the breakdown voltage, which is known as the "geiger mode", and SPAD operating in this region may generate virtually infinite Electron-Hole Pair when detecting a single photon.[1] In reality, it may produce up to 10^5~10^6 EHPs[2], which is sufficient to cause current at the order of micro ampere and thus enough to generate digital pulse. When it comes to jitter, defined as the temporal variation between photon incidence and the edge of the signal generated by the SPAD and its peripheral circuit, SPADs exhibit adequate performance in the 100-ps range, and even in the tens-of-picoseconds range in state-of-the-art works[3], while maintaining low cost. Due to its excellent sensitivity, high gain, and superior timing performance, it is used in a wide range of applications such as Light Detection and Ranging (LiDAR), X-ray imaging, and Positron Emission Tomography (PET) [4]-[6].

A SPAD system can be configured in two ways: front-side illumination (FSI) and back-side illumination (BSI). In the FSI configuration, the SPAD is fabricated using a standard CMOS process, and photons are incident on the device through multiple metal layers before reaching the active region. In the BSI configuration, the SPAD is fabricated on a thinned wafer, and photons are incident directly on the backside of the chip, without passing through the front-side metal layers[7].

The latter exhibits higher photon detection probability (PDP) due to the aforementioned characteristics, but this comes at the expense of yield and fabrication complexity, which makes the FSI configuration more attractive in many applications. SPADs are usually used with peripheral circuits such as quenching circuits and digital components like counters and TDCs. If these digital components, which consume a large area, are included within a single pixel, the ratio of the active area—essentially the depletion region of the SPAD—clearly decreases. This leads to a decrease in the fill factor, which is defined as the ratio of the active area to the total pixel area. Placing the components external to the array still poses challenges in the FSI configuration, because metal lines cannot cross over the SPAD, which reduces the fill factor. This work introduces a novel routing scheme that alleviates the aforementioned problems by summing each pixel's output in a row- or column-wise manner and combining the two signals at the counter side.

The remainder of this paper is organized as follows. Section II introduces the overall system architecture and the structure of individual sub-blocks. Section III presents the routing verification of each sub-block. Section IV provides the measurement results, and Section V concludes the paper.

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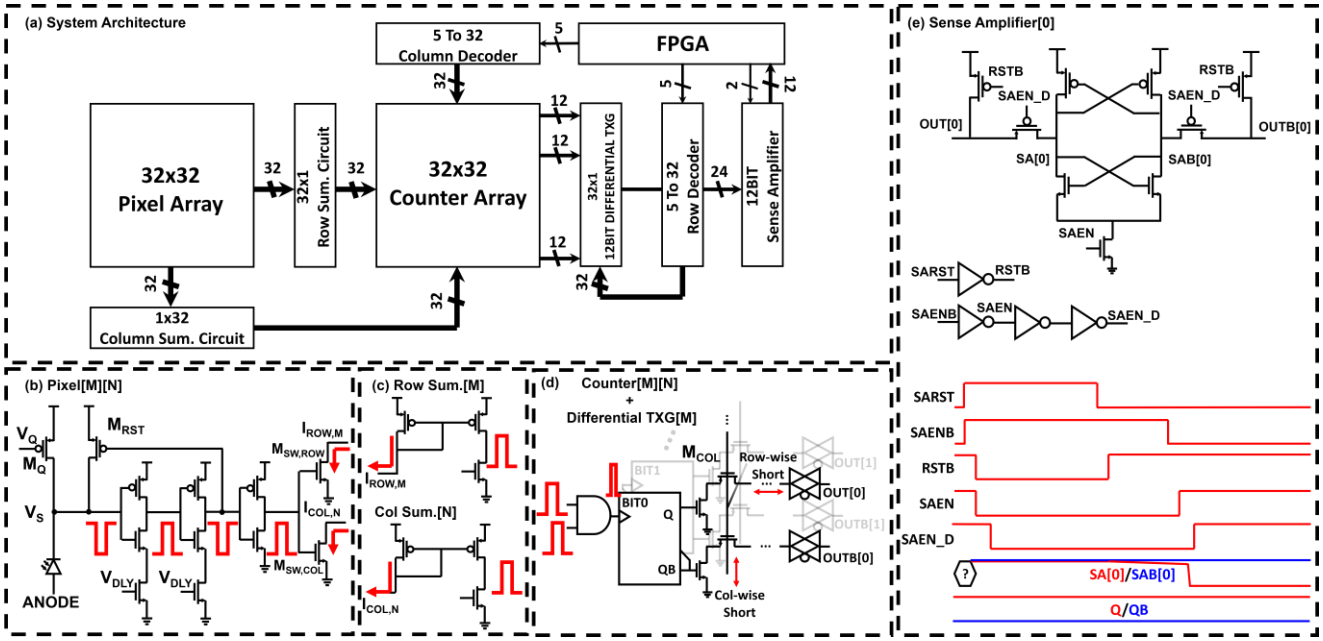

Fig. 1. Overall architecture and sub-blocks

II. SYSTEM ARCHITECTURE

Fig. 1(a) shows the overall system architecture and (b)-(e) shows detailed structure of each component included in the proposed design. All components except the FPGA are implemented on-chip.

A. Single Pixel and ROW/COL Summation Circuit

Fig. 1(b) illustrates the structure of a single pixel, which consists of a SPAD and its quenching circuit. Prior to photon detection or the occurrence of a dark count—noise arising from thermally generated electron–hole pairs or tunneling [8]—the V_S node is charged through M_Q, establishing a bias across the SPAD that exceeds its breakdown voltage. When the SPAD triggers due to previously described mechanisms, the V_S node is discharged and an active-low pulse is generated. At this moment, the bias across the SPAD falls below the breakdown voltage, temporarily disabling additional photon detection.

As the signal propagates through the first two inverters, each incorporating an additional NMOS device for delay control, the active-low pulse enables M_{RST}, which recharges the V_S node together with M_Q. This raises the SPAD bias above the breakdown voltage and restores its photon-detection capability. When the signal reaches the final inverter, an active-high output is generated, enabling $M_{SW,ROW}$ and $M_{SW,COL}$ to sink current. The drain terminals of M_{SW} devices are shorted along both the row and column directions. For example, $M_{SW,ROW}$ of Pixel[M][N] is shorted to those of Pixel[M−1][N] and Pixel[M+1][N], and is ultimately connected to the PMOS drain of ROW Sum.[M], as shown in Fig. 1(c). When $I_{ROW,M}$, $I_{COL,N}$ flow, Row Sum.[M] and Col Sum.[N] generate active-high signals, which are delivered to the AND gate of Counter[M][N] through a buffer.

B. Counter and Sense Amplifier

When both inputs of the AND gate in Counter[M][N] receive an active-high signal, the counter increments by one. If the previous counter value is 0, the Q output of the BIT0 D flip-flop becomes high while QB becomes low. All counter outputs are connected to an NMOS transistor that provides a discharge path determined by the counter state. As shown in Fig. 1(d), an additional NMOS (M_{COL}) is implemented to enable column selection. The gates of all M_{COL} transistors in the N-th column are tied together, and their drains are connected along the row direction. For example, the M_{COL} of Counter[M][N] at BIT0 is connected to those of Counter[M][N−1] and Counter[M][N+1], and ultimately to Differential Transmission Gate[M] (Differential TXG[M]). Both M_{COL} and TXG are enabled through the column/row decoder. After a counter is selected, the sense amplifier begins to operate, as it can be seen in Fig. 1(e). SAENB and SARST are first asserted to disable the sense amplifier and pre-charge the OUT/OUTB and SA/SAB nodes to VDD. Once the nodes are fully pre-charged, SARST is deasserted, and one side of the sense amplifier begins to discharge according to the counter output (Q in this case). When the SA node discharges sufficiently, SAENB is deasserted, isolating SA/SAB from OUT/OUTB and enabling the sense amplifier. The back-to-back inverters generate the final output, and SAB represents the counter value. This routing method allows the counters to be placed outside the pixel array and supports array readout without routing lines directly proportional to the number of counters. However, verification is required to ensure that routing-length differences between row and column paths do not cause failures in generating the counter clock, and to determine the appropriate timing for asserting and deasserting the sense-amplifier control signals. These considerations are addressed in the following section.

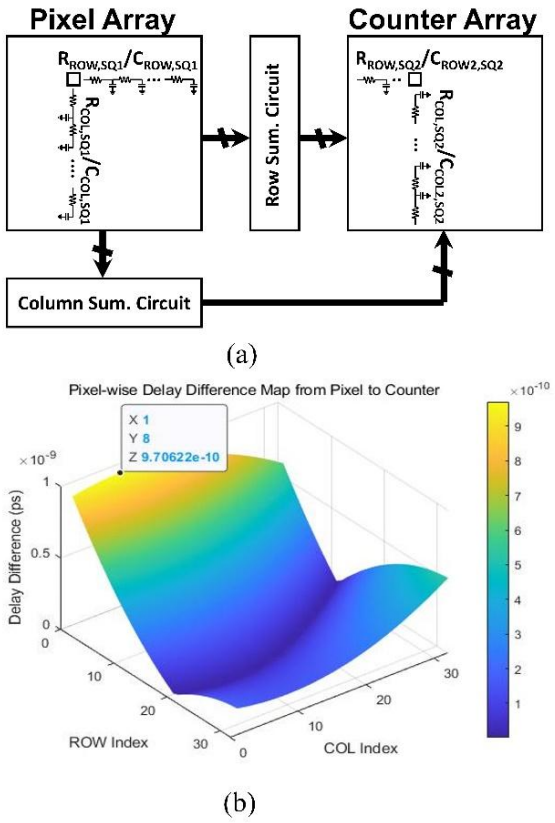

Fig. 2. (a) Parasitic RC between the pixel and counter array, and (b) Pixel-wise absolute delay difference map

III. ROUTING VERIFICATION

A. Pixel to Counter

When a SPAD within a pixel detects an incident photon, corresponding row and column signals are generated and combined at the AND gate of the counter that produces the clock signal. Due to the different routing lengths of these row and column lines, temporal misalignment between the two signals may occur. To verify that this potential mismatch does not impair system functionality, parasitic resistance and capacitance were extracted using Virtuoso PEX, and row/column delays for all pixels were evaluated. As illustrated in Fig. 2(a), the total delay consists of two components: (1) the delay from the pixel to the Row/Col Sum Circuit ($R_{ROW/COL,SQ1}$, $C_{ROW/COL,SQ1}$), denoted as $t_{d,PS,row/col}$, and (2) the delay from the Row/Col Sum Circuit to the counter ($R_{ROW/COL,SQ2}$, $C_{ROW/COL,SQ2}$), denoted as $t_{d,SC,row/col}$. The parasitic components for each unit segment were obtained by dividing the total extracted capacitance and resistance by 32, corresponding to the dimensions of the pixel and counter arrays. If N identical RC network composed of $R_{SQ}C_{SQ}$, are cascaded between nodes IN and OUT, the propagation delay when assuming a unit-step input can be calculated as follows, based on the method described in [9].

$$t_d = 0.7R_{SQ}C_{SQ}(1 + 2 + 3 + \cdots + N) \quad (1)$$

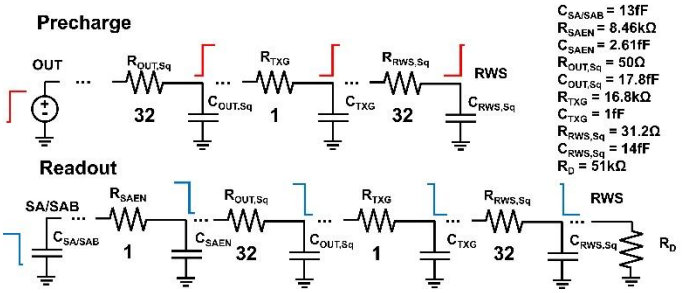

Fig. 3. Parasitic RC in the precharge/readout phases

Using this equation, the aforementioned delay components can be obtained, and the difference between the total row and column delays, denoted as $t_{d,diff}$, can be calculated accordingly.

$$t_{d,row} = t_{d,PS,row} + t_{d,SC,row} \quad (2)$$

$$t_{d,col} = t_{d,PS,col} + t_{d,SC,col} \quad (3)$$

$$t_{d,diff} = |t_{d,row} - t_{d,col}| \quad (4)$$

The extracted parasitic components for segments $R_{ROW,SQ1}/C_{ROW,SQ1}/R_{COL,SQ1}/C_{COL,SQ1}$ are 64 Ω, 7.8 fF, 42 Ω, and 12.6 fF, respectively, while the corresponding values for segments $R_{ROW,SQ2}/C_{ROW,SQ2}/R_{COL,SQ2}/C_{COL,SQ2}$ are 91 Ω, 16.2 fF, 98 Ω, and 24.1 fF, respectively. Using these values, a delay-difference map was generated, as shown in Fig. 2 (b), indicating a worst-case delay difference of approximately 970 ps. Considering that the measured SPAD dead time—during which the device remains latched following an avalanche event and cannot detect subsequent photons—is on the order of several tens of nanoseconds in this work, the delay variation caused by routing-length differences is verified not to affect overall system functionality. Furthermore, when the array is scaled to a larger size, its validity can be readily verified by performing the analysis described in this subsection and comparing the worst-case delay difference with the best-case dead time. Considering the delay difference caused by routing path variations, the proposed architecture may be disadvantageous for applications such as direct time-of-flight (dToF) and fluorescence lifetime imaging (FLIM), where precise temporal information is essential. However, it can still be suitable for applications such as 2D intensity imaging or indirect time-of-flight (iToF), in which counter-based operation is conventionally used. In this work, the system operation is verified through intensity imaging.

B. Counter to Sense Amplifier

Similar to conventional SRAM readout architectures, this work adopts a precharge-and-sense-amplifier–based method to read the value stored in a counter within the counter array. As described earlier, this approach alleviates routing complexity by reducing the number of required lines; however, careful consideration of input-signal timing is essential for reliable readout. The precharge and readout phases can be analyzed by modeling the signal path as a cascaded RC network, as shown in Fig. 3.

During the precharge and readout phases, all relevant nodes are assumed to be initially 0 V / VDD, respectively.

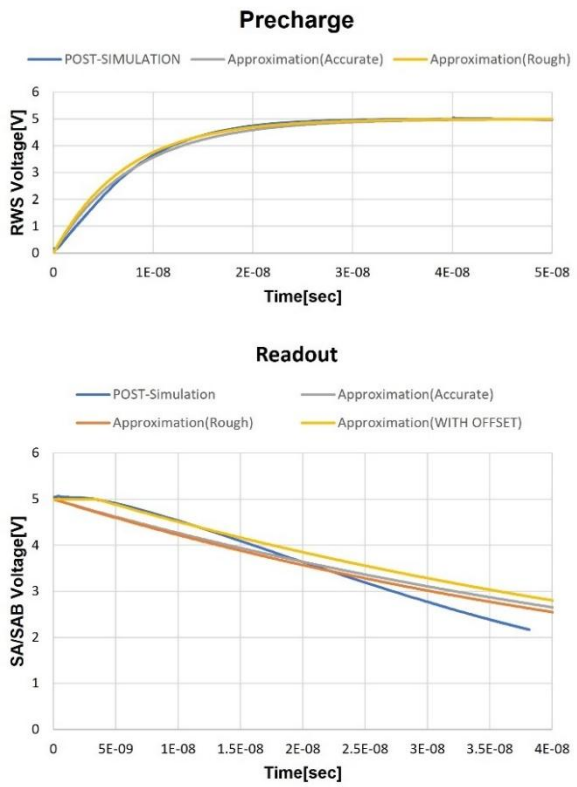

Fig. 4. Waveform derived from the simulation results and calculations

Moreover, a worst-case scenario is considered using Counter[0][0], whose distance from the sense amplifier is the longest. If N RC segments exist between the OUT/RWS node and the SA,SAB/RWS node in each configuration, and the number of each R_iC_i segment is denoted as Q_i, the voltages V_{RWS} and $V_{SA/SAB}$ during the precharge and readout phases can be derived as follows. These expressions are obtained by applying the Laplace transform and neglecting higher-order terms.

$$V_{RWS}(t) = VDD \cdot (1 - e^{\frac{-t}{\tau_{PC}}}) \tag{5}$$

$$\tau_{PC} = \sum_{i=1}^{N} \frac{Q_i(Q_i+1)}{2} R_iC_i + \sum_{i=1}^{N-1} Q_iQ_{i+1}R_iC_{i+1} \tag{6}$$

$$V_{SA/SAB}(t) = VDD \cdot e^{\frac{-t}{\tau_{RO}}} \tag{7}$$

$$\tau_{RO} = \sum_{i=1}^{N}\sum_{j=1}^{i-1} Q_iQ_jR_iC_j + \sum_{i=1}^{N}[\frac{Q_i(Q_i-1)}{2} R_iC_i + Q_i(R_iC_{SA} + R_FC_i)] + R_FC_{SA} \tag{8}$$

The resistance and capacitance of the PMOS devices in the sense amplifier and transmission gate were obtained using the method described in [9]. R_D, representing the resistance of the two series-connected NMOS transistors that provide the discharge path, was extracted by dividing the drain voltage by the drain current when the drain voltage is VDD, rather than using derivative-based small-signal resistance. The remaining parasitic components were extracted using the same procedure described in the pixel-to-counter analysis.

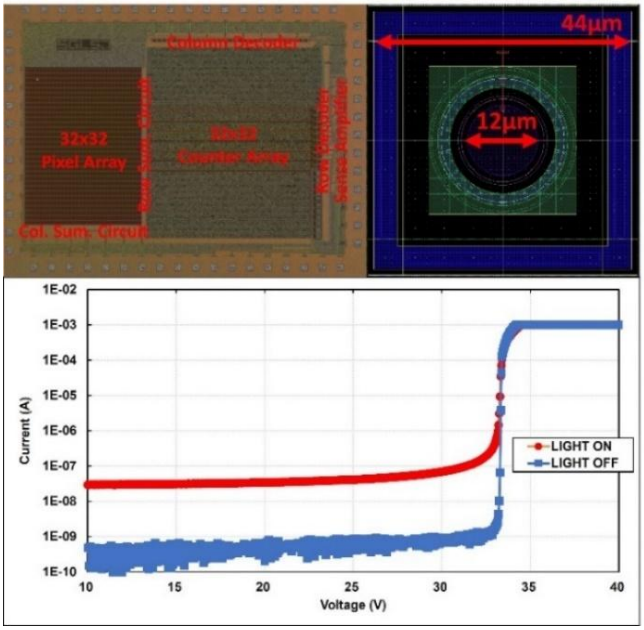

Fig. 5. Chip micrograph, SPAD layout, and measured I–V curves under different conditions

Fig. 4 shows the simulated V_{RWS} and $V_{SA/SAB}$ waveforms during the precharge and readout operations. Accurate approximations were obtained by evaluating the previously derived equations, whereas rough approximations were obtained by neglecting $R_{OUT,SQ}$ and $R_{RWS,SQ}$, assuming that MOSFET resistance dominates the delay behavior. In post-layout simulation of the precharge phase, the RWS node reached 4.95 V in 28.7 ns. The accurate and rough analytical approximations predicted 36.1 ns and 33.1 ns, corresponding to 26% and 15% errors, respectively. It can be seen that, during readout, the SA/SAB node briefly exceeds VDD. This is caused by Sense Amplifier reset PMOS gate input fed to OUT/OUTB node[9, pp. 353], and can be considered an offset that should be characterized through simulation. Monte Carlo analysis showed that a 1% voltage difference between SA and SAB is sufficient to guarantee deterministic sense-amplifier output when one side is held at VDD. Simulation results indicated that SA/SAB discharges to 4.95 V in 4.22 ns; after including a 3.5 ns offset, both the accurate and rough approximations predicted 4.1 ns, corresponding to a 2.4% error. The discrepancy between the simulation and the calculation over time is mainly caused by the changing value of R_D as the RWS voltage decreases. However, this does not pose a problem because a sufficient SA/SAB difference develops within 10ns. The results obtained can be used to determine appropriate timing for the SARST and SAENB signals and may guide future optimization of the overall system.

IV. MEASUREMENT RESULTS

The proposed SPAD array was implemented using a 0.18 μm BCDMOS process. Fig. 5 shows the chip micrograph, the layout of a single SPAD employing a PW/DNW structure,

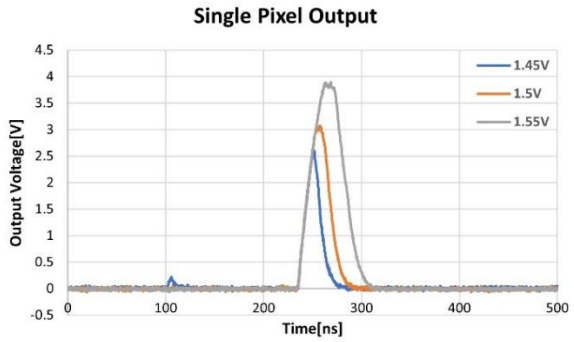

Fig. 6. Measured single-pixel output under varying V_{INV} bias conditions

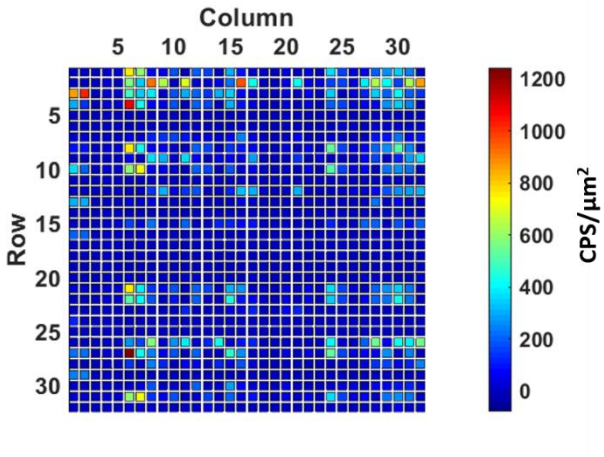

Fig. 7. Measured dark count rate (DCR) distribution of the SPAD array

and the measured I–V characteristics under two conditions. The breakdown voltage of the SPAD was measured to be 33 V, which is consistent with the value predicted from the process documentation describing the electrical specifications of the layers.

Fig. 6 presents the output voltage of a single pixel when V_{INV} is varied from 1.45 V to 1.55 V. As V_{INV} increases, the NMOS in the first inverter restricts the charging of the output node, while that in the second inverter suppresses its discharge compared to a standard inverter composed of only two MOSFETs. Measurement results show that increasing V_{INV} leads to a larger inverter delay and consequently a longer overall dead time. The measured delays are 20 ns, 32 ns, and 51 ns for V_{INV} = 1.45 V, 1.50 V, and 1.55 V, respectively, demonstrating that the delay is sufficient to prevent the system malfunction identified in the pixel-to-counter routing verification.

Fig. 7 illustrates the dark count rate (DCR) distribution of the designed array. The median DCR value is 0.51 cps/μm^2. Hot pixels, defined as pixels exceeding 600 cps/μm^2, account for 1.6% of the total array. These hot pixels are primarily attributed to process variations or fabrication defects. Fig. 8 illustrates the photon counting response of representative pixels versus incident optical power, validating the pixel operation as the CPS increases with the light intensity.

Fig. 9 illustrates the measurement setup and the resulting images obtained. A dot-matrix source was employed for illumination because of its programmable flexibility, which

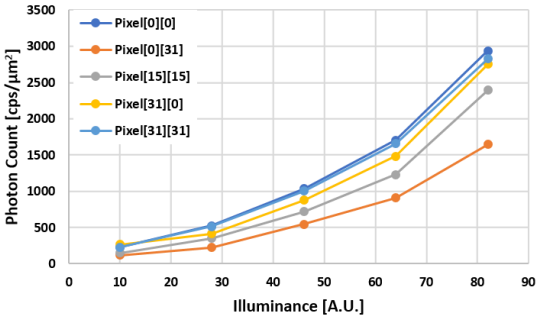

Fig. 8. Measured photon count of representative pixels as a function of incident optical power

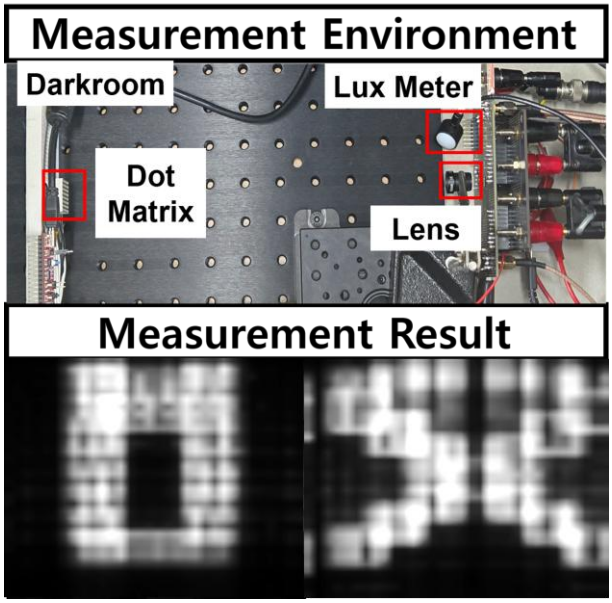

Fig. 9. Measurement environment and results of the proposed system

allows for the generation of diverse patterns in various sizes and shapes. The “0” and “X” pattern was projected onto the SPAD array using a dot-matrix light source and a lens. The resulting image confirms that each pixel can produce output proportional to the incident light intensity and validates the overall approach of placing large digital components outside the SPAD array to preserve the fill factor. However, a notable phenomenon can be observed at the top of the image, where an additional line appears that is not induced by light illumination. This is due to false counts caused by a combination of the hot pixels at the top of the array, as shown in Fig. 7, and the incident light. This issue can be alleviated by partitioning the array into sub-arrays. Additionally, allocating different codes to each pixel—for example, by using combinations of NMOS and PMOS for M_{SW} rather than only NMOS—can further reduce false counting.

Table 1 summarizes the effectiveness of the proposed method, showing that relocating the digital components outside the pixel helps preserve the FF of the entire array. This advantage becomes more evident when compared with [10], in which the fill factor decreased by 89% from the pixel level to the array level, whereas this work achieved only an 11% reduction from the SPAD level to the array level.

TABLE I.
Comparison of Pixel Array Architectures in This Brief and Previous Works

Parameter	This Work	[10]	[11]	[12]
Process (nm)	180	180	160	160
Illumination Type	FSI	FSI	FSI	FSI
Readout Architecture	External	In-Pixel	In-Pixel	In-Pixel
Pixel Array	32x32	64x64	24x24	16x16
Pixel Pitch (μm)	44	20.4	N/A	N/A
Pixel Fill-Factor (%)	4.48	32.3	N/A	N/A
Array Fill-Factor (%)	5.19	3.56	3.14	9.6
Power Consumption (mW)	67	100	40	500
Frame Rate (frames/s)	3	3	N/A	N/A

V. CONCLUSION

We present a 32×32 SPAD array implemented in a 0.18-μm BCDMOS process, where the fill factors of the SPAD device, a single pixel, and the full array are 5.84%, 4.48%, and 5.19%, respectively, exhibiting only 11% decrease of FF from SPAD to array level. Using parasitic RC extraction and simple analytical calculations, a delay map was derived, and the functionality of the proposed routing scheme was verified through the measured output of a single pixel. By applying a hand-calculated input signal, whose validity was confirmed through simulation, the system successfully reconstructed the pattern provided by a dot-matrix generator, demonstrating the overall validity of the proposed design.

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