A 20-Gb/s/pin Single-Ended Transmitter with Capacitive Peaking Driver Based Crosstalk and Inter-Symbol Interference Compensation

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***Abstract* – This paper presents a 20-Gb/s/pin single-ended transmitter that employs a capacitive peaking driver (CPD)-based crosstalk and inter-symbol interference (ISI) compensation technique, implemented in a 65-nm CMOS process. The CPD enhances high-frequency signal components and plays a central role in suppressing crosstalk and ISI, while its programmable capacitor bank enables adaptation to a wide range of channel-loss conditions. By generating the crosstalk compensation signal in advance from low-rate data of adjacent lanes, the proposed architecture achieves zero latency and aligns the shaping action with the expected disturbance window while incurring minimal power overhead, eliminating the need for highest-rate replica paths. Digitally controlled delay lines (DCDLs) further refine the timing of both crosstalk and ISI compensation. Post-layout simulation results demonstrate a horizontal eye-opening of 31.22 ps and a vertical eye-opening of 18.14 mV under a worst-case channel condition exhibiting 25.89 dB insertion loss at the Nyquist frequency. These results confirm that the CPD-based compensation scheme effectively mitigates crosstalk and ISI while maintaining energy-efficient high-speed signaling, making it a promising solution for future low-power, high-bandwidth serial interfaces.**

***Keywords*—Transmitter, Single-ended, Memory Interface, Crosstalk, Inter-symbol interference (ISI)**

I. INTRODUCTION

The rapid expansion of artificial intelligence (AI) and high-performance computing (HPC) is driving the need for increasingly higher memory bandwidth in modern processing systems. High-performance graphics processing units (GPUs) and tensor processing units (TPUs) depend on memory technologies such as HBM [1], [2], and GDDR6 to support large-scale parallel computation [3], [4], [5]. To meet these demands, memory interfaces continue to increase both the number of DQ lanes and the per-pin data rate. In particular, GDDR interfaces, which employ a relatively smaller number of pins compared to HBM, rely on higher per-pin data rates to achieve the required memory bandwidth. However, operating at multi-gigabit speeds intensifies signal-integrity challenges [6]. Switching activity in adjacent lanes generates crosstalk that causes additional vertical noise and timing errors, while frequency-dependent channel loss leads to ISI, reducing the horizontal eye-opening. These combined impairments significantly reduce eye margin and limit the robustness of high-speed single-ended memory channels [7].

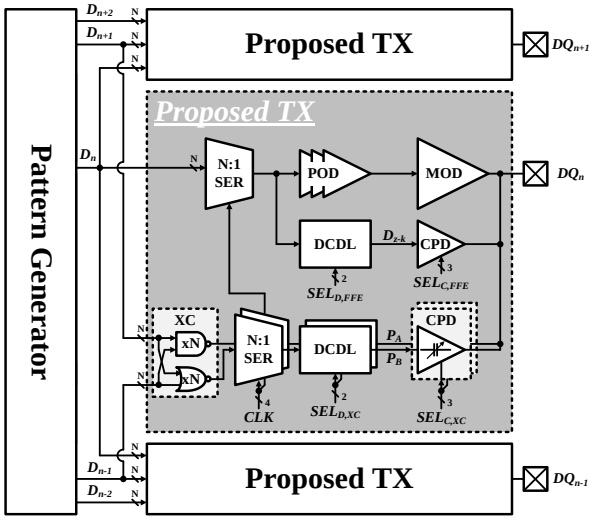

Fig. 1. Architecture of the proposed single-ended transmitter with CPD-based crosstalk and ISI compensation.

Capacitive peaking drivers (CPDs) have been used to enhance high-frequency components of the transmitted signal and partially mitigate crosstalk and inter-symbol interference (ISI) [8]. Conventional CPD-based methods can exhibit latency in the compensation path, originating from the physical routing distance that the compensation signal must traverse on the aggressor lane [9]. The resulting delay shifts the compensation pulse later than the disturbance, producing a timing misalignment at the victim node. Such latency-driven mismatch limits compensation effectiveness and can further degrade signal quality. To overcome these limitations, the proposed transmitter adopts prediction-based crosstalk compensation that achieves zero latency, while ISI is separately mitigated through programmable CPD. The transmitter predicts crosstalk from low-rate data of adjacent lanes and uses digitally controlled delay lines (DCDLs) to align the compensation timing with the expected disturbance. By combining prediction-based crosstalk

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mitigation with adaptive CPD tuning, the architecture improves signal integrity and supports reliable high-speed operation.

II. ARCHITECTURE OF THE PROPOSED TRANSMITTER

Fig. 1 illustrates the architecture of the proposed transmitter, which incorporates two signal-processing paths: a prediction-based crosstalk compensation path and a CPD-based feed-forward equalization (FFE) path for ISI mitigation. Both paths operate in parallel to condition the transmitted data and enhance signal integrity at multi-gigabit rates. In the crosstalk compensation path, disturbances originating from the adjacent lanes, DQ_{n-1} and DQ_{n+1}, are predicted using their low-rate N-bit data streams. The crosstalk compensator (XC) converts these low-rate data patterns into compensation pulses that represent the expected coupling behavior. The pulses are serialized into the highest-rate data stream and then processed by the digitally controlled delay lines (DCDLs). The DCDLs calibrate the arrival time so that the compensation aligns with the anticipated disturbance at the main lane, DQ_n, regardless of latency differences that may occur between lanes. After calibration, the two outputs P_A and P_B drive the compensation CPD to suppress coupling effects from the up and down adjacent lanes. The second path performs FFE for ISI reduction using a programmable CPD. A separate DCDL generates the delay-adjusted control signal, $D_{z\text{-}k}$, which determines the timing of the pre-emphasis relative to the main data. When applied through the CPD, $D_{z\text{-}k}$ enhances the high-frequency components of the output waveform, effectively realizing pre-emphasis suitable for varying channel-loss conditions. Independent control settings configure the CPD parameters for the main data path and for the crosstalk compensation path, enabling flexible equalization operation. The main output driver (MOD) employs an N-over-N topology with an active inductor to preserve transition quality and strengthen high-frequency response. To support verification and multi-lane evaluation, the prototype includes replicated transmitter lanes along with a pattern generator (PG) that provides selectable test sequences. Each transmitter integrates N:1 serializers (N:1 SERs), DCDLs, CPDs, XC, and MOD, operating with a 4-phase 5-GHz clocking scheme.

III. COMPENSATION CIRCUIT OPERATION

The overall operation of the proposed compensation circuits can be understood by examining the timing relationships among adjacent lanes and the behavior of conventional and proposed compensation paths. Fig. 2(a) illustrates a conventional transmitter architecture in which the crosstalk-compensation signal is generated by tapping the highest-rate data stream of aggressor lanes [8]. Because this compensation pulse inevitably experiences latency, its arrival time at the main-output driver, MOD_n, lags behind the actual disturbance. As a result, even if the compensation waveform has the correct shape, its temporal misalignment prevents effective cancellation. In contrast, Fig. 2(b) shows

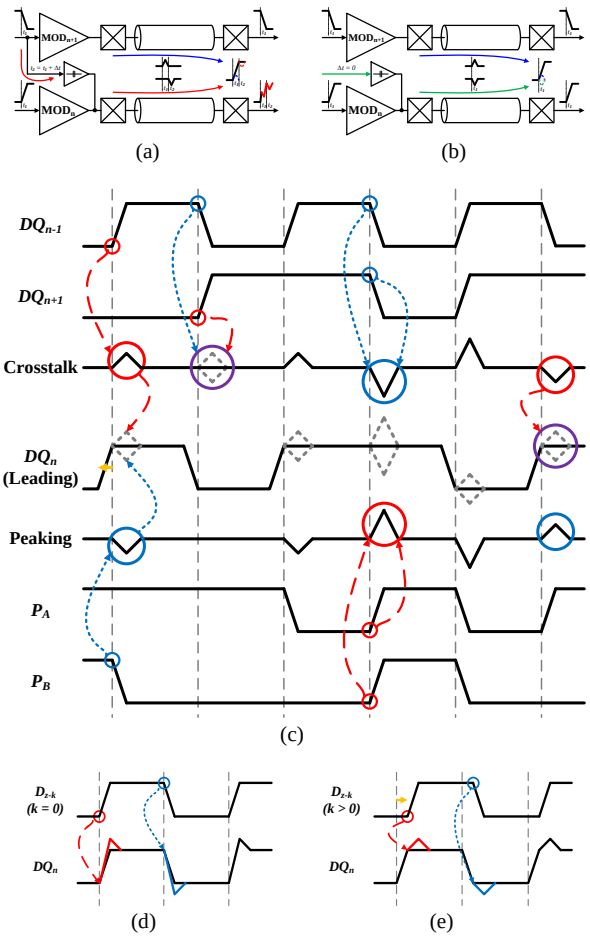

Fig. 2. Conceptual comparison of crosstalk compensation and timing diagrams of the proposed crosstalk and ISI compensation. (a) Conventional TX with latency on the compensation path. (b) Proposed latency-free compensation. (c) Crosstalk-induced distortion and timing-aligned shaping. (d) ISI compensation with $k = 0$. (e) ISI compensation with $k > 0$.

the proposed prediction-based scheme, where compensation pulses are generated directly from the low-rate data of adjacent lane. Since this process occurs before serialization, the pulses are available in advance, resulting in zero latency relative to the disturbance. The compensation window is therefore aligned to the expected timing of the crosstalk disturbance at DQ_n, rather than being tied to the switching timing of MOD_{n+1}.

With this latency issue removed, the remainder of the compensation behavior follows the mechanisms shown in Fig. 2(c). When DQ_n arrives earlier than DQ_{n-1} and DQ_{n+1} due to routing induced timing offsets, the late switching of the adjacent lanes produces a localized distortion at the victim node. Because the proposed architecture already provides a latency-free compensation pulse, the DCDL only needs to fine-tune the pulse timing to match the expected disturbance interval. As shown in Fig. 2(c), the peaking interval restores the intended slope of the DQ_n transition, and the compensation effectiveness depends primarily on timing alignment, not on the absolute ordering of lane transitions. The proposed crosstalk compensation is generated from low-rate adjacent-lane data prior to serialization. Rather than attempting to exactly replicate the high-rate aggressor waveform, the

prediction focuses on detecting the occurrence and polarity of adjacent-lane switching events in an edge-aware manner. Since the low-rate signals preserve full-swing transitions before serialization, dominant edge-related disturbances can be identified with limited sensitivity to noise or slew degradation. Although an absolute timing offset may exist between the low-rate prediction path and the high-rate data path, the proposed architecture adopts a modular and symmetric design across all lanes. As a result, the skew between prediction and data paths is largely systematic, allowing the remaining relative misalignment to be calibrated by DCDLs. The DCDLs provide unit-interval (UI)-normalized coarse timing control rather than fine-grained delay resolution, which is sufficient for aligning the compensation within the dominant disturbance window. This design choice is consistent with prior transmit equalization studies showing that tap delays around a half-UI [10] provide effective mitigation of channel-induced ISI without requiring high-resolution delay accuracy. Accordingly, the proposed architecture prioritizes timing-aligned shaping to restore edge integrity over precise delay quantization. However, excessive peaking strength can degrade signal fidelity due to the inherent high-pass characteristic of capacitive peaking, indicating the existence of an optimal trade-off. By combining moderate peaking with UI-normalized timing alignment, the proposed scheme achieves robust eye-opening improvement without relying on high-resolution delay control or excessive peaking.

The remaining ISI-related operation is depicted in Fig. 2(d) and Fig. 2(e). The auxiliary control signal $D_{z\text{-}k}$ determines where the pre-emphasis energy is applied relative to the DQ_n transition. For $k = 0$, Fig. 2(d) shows that pre-emphasis aligns with the switching instant, producing a symmetric enhancement suitable for channels with moderate high-frequency attenuation. When $k > 0$, Fig. 2(e) shows that delaying the shaping action strengthens the later portion of the edge, whereas negative k values bias the shaping toward the leading portion. The discrete tunability of k enables flexible pre-emphasis timing adaptable to diverse channel conditions without modifying the main data path.

IV. SIMULATION RESULTS

The effectiveness of the proposed compensation scheme was verified through post-layout simulations. Fig. 3 shows the switching activity of DQ_{n-1} and DQ_{n+1}, along with the generated compensation pulses. Without compensation, the near-end waveform of DQ_n exhibits noticeable distortion caused by the switching activity of adjacent lanes. This distortion becomes more pronounced at the far-end of the channel, where additional loss and reflections further degrade the signal. The corresponding near-end and far-end waveforms clearly show the perturbations introduced by crosstalk. When the proposed shaping pulses are applied, both the near-end and far-end waveforms exhibit substantially improved transition profiles and reduced disturbance. The compensated results in Fig. 3 demonstrate that the designed timing alignment and shaping mechanism successfully suppress the crosstalk-induced distortion observed at both observation points.

The impact of delay alignment on compensation

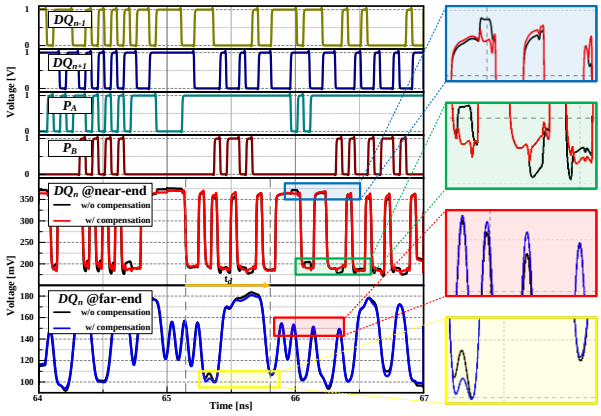

Fig. 3. Post-layout simulation results of near-end and far-end waveforms without and with the proposed crosstalk compensation.

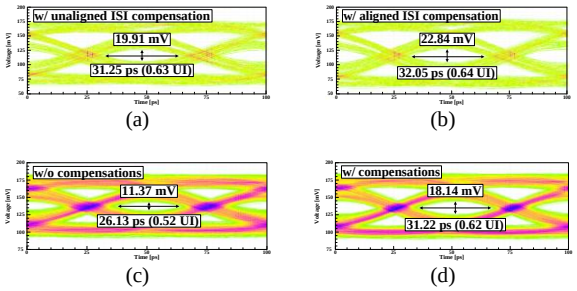

Fig. 4. Simulated eye-diagrams for (a) ISI compensation with unaligned delay, (b) ISI compensation with aligned delay, (c) without compensations under the worst-case channel condition, and (d) with the proposed ISI and crosstalk compensation under the worst-case channel condition.

effectiveness is illustrated in Fig. 4(a) and Fig. 4(b). These results compare ISI compensation with unaligned and aligned delay settings. When the compensation delay is not properly aligned, the applied peaking can occur outside the dominant disturbance window, leading to partial eye closure despite the presence of ISI compensation. In contrast, proper delay alignment restores the eye opening by applying the shaping action at the appropriate timing. This comparison highlights that delay alignment is a critical factor in CPD-based compensation and that misaligned compensation can degrade signal integrity instead of improving it. The overall effectiveness of the proposed ISI and crosstalk compensation is quantified by the eye-diagram results in Fig. 4(c) and Fig. 4(d). The worst-case channel corresponds to the longest interconnect, exhibiting an insertion loss of 25.89 dB at 10 GHz, as shown in Fig. 5(b). Without compensations, the eye-opening is limited to 11.37 mV in the vertical direction and 26.13 ps (0.52 UI) in the horizontal direction, indicating insufficient eye margin for reliable high-speed operation. With the proposed compensation enabled, the eye-opening increases to 18.14 mV and 31.22 ps (0.62 UI). These results demonstrate that the proposed timing-aligned compensation effectively enhances both vertical noise tolerance and timing margin under worst-case channel conditions.

Fig. 5 summarizes the physical implementation, channel characteristics, and power consumption of the proposed transmitter. The post-layout view in Fig. 5(a) shows that the

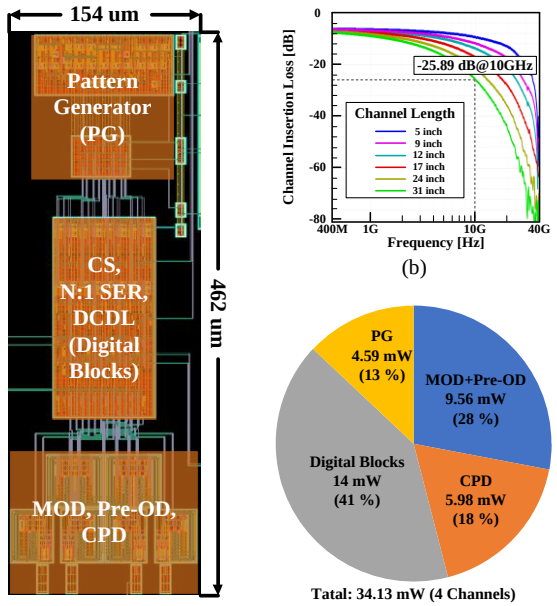

Fig. 5. (a) Chip layout of the proposed transmitter, (b) channel insertion loss characteristics for different channel lengths, and (c) measured power breakdown of the proposed transmitter for four channels

transmitter occupies 0.07 mm^2 and integrates the PG, digital blocks including the serializers, DCDLs, and the pre- and main- driver stages with CPD circuits. Fig. 5(b) represents the channel insertion loss profiles used in the simulations for multiple channel lengths. Fig. 5(c) shows the power breakdown aggregated over four channels, with a total power consumption of 34.13 mW. The distribution indicates that the compensation circuitry incurs modest power overhead and does not require highest-rate replica paths or additional high-speed analog blocks.

A performance comparison with high-speed transmitter designs is provided in Table I. Although implemented in a 65-nm CMOS process, the proposed transmitter achieves a 20-Gb/s/pin data rate with a 0.62-UI eye opening. The energy efficiency of this work is derived from post-layout simulation results by normalizing the total four-channel power to per-channel operation, yielding 0.43 pJ/b. These results demonstrate that the proposed architecture achieves competitive signal integrity and energy efficiency compared with prior work, while maintaining modest area and power consumption through timing-aligned crosstalk suppression and CPD-based ISI mitigation.

TABLE I. Performance Comparison of High-Speed Transmitters

	2022 [1]	2023 [2]	2019 [5]	2024 [7]	2020 [9]	**#This Work**
Tech. [nm]	65	65	-	28	8	**65**
Signaling Style	Duo binary	NRZ	NRZ	Dicode	NRZ	**NRZ**
Data rate [Gb/s/pin]	5	10	18	11	18	**20**
Supply Voltage [V]	0.6 / 0.3	0.7 / 0.3	1.35	1 / 0.5	1.35	**1**
Area [mm^2]	0.0008 /1pin	0.0025 /1pin	4.79 /1Ch.	0.0046 /1Ch.	4.15 /1Ch.	**0.07 /4Ch. TX-only**
Eye opening [UI]	*0.69	0.79	0.7	0.42	0.5	**0.62**
Energy Efficiency [pJ/b]	0.37	0.18	-	0.38	-	***0.43**

This work is based on post-layout simulation results
* Estimated from the simulation/measurement results and figures

V. CONCLUSIONS

This work demonstrates that signal disturbances caused by crosstalk and ISI in high-speed single-ended transmitters can be effectively mitigated through timing alignment and shaping, rather than by introducing additional high-speed circuitry. By generating a zero-latency compensation signal from low-rate data of adjacent lanes, the proposed architecture aligns the compensation window directly with the time interval in which adjacent-lane activity affects the victim signal, thereby suppressing crosstalk without increasing the complexity of the highest-rate data path. In addition, discrete delay control enables the capacitive peaking driver (CPD) to adjust the timing of pre-emphasis, providing effective ISI shaping across a wide range of channel-loss conditions. Because both crosstalk and ISI mitigation are achieved through timing-aligned shaping rather than structural duplication, the proposed transmitter remains compact and energy-efficient while maintaining robust transition quality under varying routing offsets. The simulation results confirm that combining zero-latency, timing-aligned crosstalk suppression with CPD-based ISI shaping provides an efficient and scalable solution for enhancing signal integrity in high-bandwidth memory interfaces and other multi-gigabit single-ended communication systems.

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REFERENCES

[1] J. -Y. Kim et al., "A 5 Gb/s Time-Interleaved Voltage-Mode Duobinary Encoding Scheme for 3-D-Stacked IC," *IEEE J. Solid State Circuits*, vol. 57, no. 6, pp. 1913–1923, Jun. 2022, doi: 10.1109/JSSC.2022.3153666.

[2] J. -Y. Kim et al., "An Energy-Efficient Design of TSV I/O for HBM With a Data Rate up to 10 Gb/s," *IEEE J. Solid State Circuits*, vol. 58, no. 11, pp. 3242–3252, Nov. 2023, doi: 10.1109/JSSC.2023.3285896.

[3] D. Foley and J. Danskin, "Ultra-Performance Pascal GPU and NVLink Interconnect," *IEEE Micro*, vol.37, no. 7-17, Mar. 2017, doi: 10.1109/MM.2017.37.

[4] K.-D. Hwang et al., "A 16Gb/s/pin 8Gb GDDR6 DRAM with bandwidth extension techniques for high-speed applications," in *IEEE Int. Solid State Circuits*

Conf. (ISSCC) Dig. Tech. Papers, Feb. 2018, pp. 210–212, doi: 10.1109/ISSCC.2018.8310258.

[5] Y.-J. Kim et al., "A 16-Gb, 18-Gb/s/pin GDDR6 DRAM With Per-Bit Trainable Single-Ended DFE and PLL-Less Clocking," *IEEE J. Solid State Circuits*, vol. 54, no. 1, pp. 197–209, Jan. 2019, doi: 10.1109/JSSC.2018.2883395.

[6] J. Song et al., "10 Gbits/s/pin DFE-Less Graphics DRAM Interface With Adaptive-Bandwidth PLL for Avoiding Noise Interference and CIJ Reduction Technique," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 1, pp. 344-353, Jan. 2017, doi: 10.1109/TVLSI.2016.2580713.

[7] H. Park, S.-M. Yu, and J. Song, "An 11 Gb/s 0.376 pJ/Bit Capacitor-Less Dicode Transceiver With Pattern-Dependent Equalizations TIA Termination for Parallel DRAM Interfaces," *IEEE Access*, vol. 12, pp. 145934-145943, 2024, doi: 10.1109/ACCESS.2024.3432784.

[8] Partovi et al., "Single-ended transceiver design techniques for 5.33Gb/s graphics applications," in *IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 136-137, doi: 10.1109/ISSCC.2009.4977345.

[9] S.-M. Lee et al., "An 8nm 18Gb/s/pin GDDR6 PHY with TX Bandwidth Extension and RX Training Technique," in *IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2020, pp. 338–340, doi: 10.1109/ISSCC19947.2020.9062937.

[10] H. Crit and J. Loinaz, "A 10Gb/s half-UI IIR-tap transmitter in 40nm CMOS," in *IEEE Int. Solid State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2011, pp. 448–450, doi: 10.1109/ISSCC.2011.5746392.

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