A 100-MHz Multi-Step Pulse-Width Modulator for Low-Power Signal Isolation in Gate Drivers for Wide-Bandgap Devices

Donghyun Kim and Minseob Shim [a]
Department of Electronic Engineering, Gyeongsang National University
E-mail : sms8520@gnu.ac.kr

***Abstract* – High-performance and high-reliability gate drivers are essential for fully exploiting the switching capability of wide-bandgap (WBG) power devices. Due to the large voltage differences inherent to high-voltage power stages, robust signal isolation is required to reliably transfer control commands across domains. Inductive or capacitive coupling techniques are typically employed to achieve low-latency isolation, among which inductive coupling offers improved immunity to common-mode transient noise compared with capacitive counterparts. However, when the transmitted pulse width becomes excessively long, conventional inductive-coupling isolators suffer from substantial static current consumption, leading to increased power dissipation and thermal stress. To address these challenges, this work introduces a multi-step pulse-width modulator optimized for low-power isolators. Implemented in a 0.18-µm CMOS process, the proposed scheme conveys data through a short sequence of narrow, adjustable pulses rather than continuous current flow, enabling event-driven operation that substantially reduces average DC current. Post-layout simulations using a highly realistic transformer model with a 105 nH primary inductance and parasitic elements show that the isolator current can be tuned from 5.563 mA to 11.48 mA, significantly lower than the 20.86 mA required by the conventional approach. By lowering power consumption while preserving robust signal transfer, the proposed method supports higher system integration and improved long-term reliability.**

***Keywords*— Gate Driver, WBG Devices, Pulse Width Modulation, Signal Isolator.**

I. INTRODUCTION

In power conversion systems, high-voltage and high-current switching devices play a central role, and silicon insulated gate bipolar transistors (Si-IGBTs) have long been widely adopted for this purpose. Although Si-IGBTs are well suited for handling large power levels, their inherently slow switching behavior results in substantial switching losses and the need for bulky passive components, which in turn limits achievable power density and constrains efforts toward system miniaturization and efficiency improvement [1]. Wide-Bandgap (WBG) semiconductor devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have recently gained widespread adoption due to their advantages in switching performance and efficiency. SiC MOSFETs provide higher breakdown voltage and superior thermal conductivity compared to silicon devices, enabling high-speed operation at several hundred kilohertz or more [2], and are increasingly used in high-voltage systems such as electric-vehicle inverters. GaN FETs, with even faster switching capability extending into the megahertz range [2], allow substantial reduction of passive component size, making them attractive for data-center power supplies and compact consumer adapters.

As next-generation WBG devices operate at very high switching frequencies, gate drivers (Fig. 1(a)) and signal isolators (Fig. 1(b)) are required to provide high-speed operation, low propagation delay, and strong Common-Mode Transient Immunity (CMTI) [3]. Traditional optocouplers, once widely used for isolation, have become unsuitable for modern WBG-based power systems due to their long propagation delay, bulky packaging, and high power consumption [4]. In contrast, capacitive and inductive isolators implemented in standard CMOS processes have emerged as more viable solutions, offering data rates exceeding several hundred megabits per second [4], [5]. Among these approaches, inductive coupling is particularly advantageous because of its robust immunity to external noise [6] and superior signal integrity. However, despite these benefits, reducing power consumption remains a key challenge due to the intrinsic behavior of the isolation transformer [7].

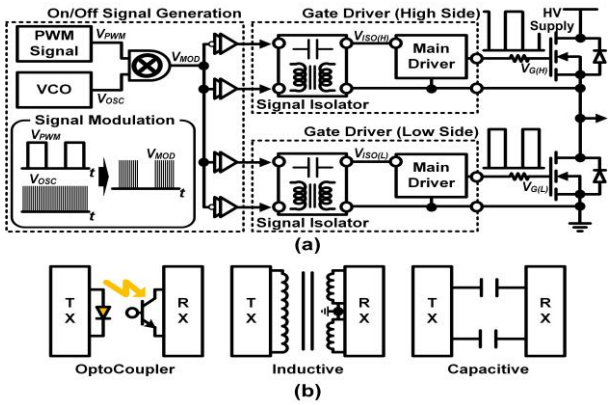

Fig. 1. (a) Overall structure of a gate driver for WBG drivers, highlighting the signal modulation and isolation stages. (b) Comparison of typical signal isolation methods: optocoupler, inductive and capacitive coupling

a. Minseob Shim; sms8520@gnu.ac.kr

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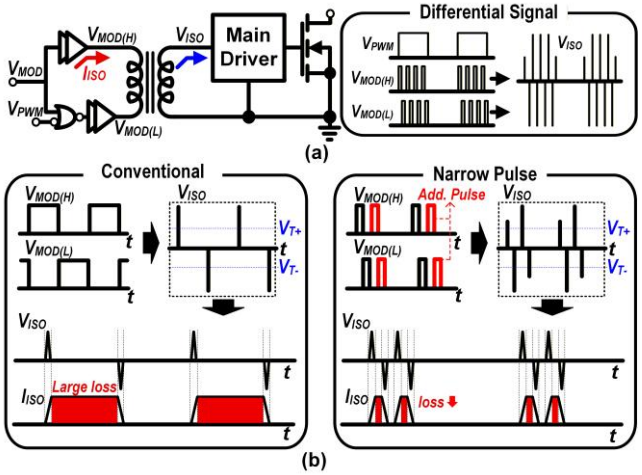

Fig. 2. (a) Transmission differences after the isolator due to attenuation. (b) Difference in current consumption between wide and narrow pulse.

In high-performance systems employing inductive coupling, each transmit pulse induces a ramp in the transformer's magnetizing current. As a result, the pulse width directly determines the current swing and its RMS value, which ultimately dictates the isolator's power dissipation. To alleviate this limitation, this work introduces a multi-step pulse-width modulator (MPWM) technique that adaptively adjusts the pulse width applied to the transformer, thereby reducing the magnetizing current and lowering overall power consumption. By controlling the pulse duration in accordance with the required data transmission behavior, the proposed approach mitigates unnecessary current buildup and effectively suppresses heat generation within the isolator.

II. MODULATOR FOR THE SIGNAL ISOLATION

A. Power Loss Caused by Wide Pulse Width Signal on Inductive Isolator

As shown in Fig. 1(a), the gate-driver signal path begins with a PWM control signal that is modulated at the transmitter (TX), transmitted across a galvanically isolated channel, and recovered by the receiver (RX) before being applied to the gate of the power semiconductor [8]. During high-side operation, the switch-node voltage causes a large common-mode swing between TX and RX, making a robust signal-isolation stage essential. Among various isolation methods, transformer-based inductive coupling, illustrated in Fig. 1(b), is widely adopted due to its strong noise immunity and suitability for high-speed WBG gate-driver systems.

In a transformer-coupled isolator, each transmit pulse drives the primary coil and produces a corresponding current ramp governed by the magnetizing inductance. The resulting secondary-side voltage is primarily determined by the rising and falling edges of this current, meaning that correct data transfer depends on edge timing rather than the absolute pulse width. This current behavior forms the basis of the isolator's power-loss mechanism.

Fig. 2 highlights how the pulse width influences both signal transfer and transformer current. Although an

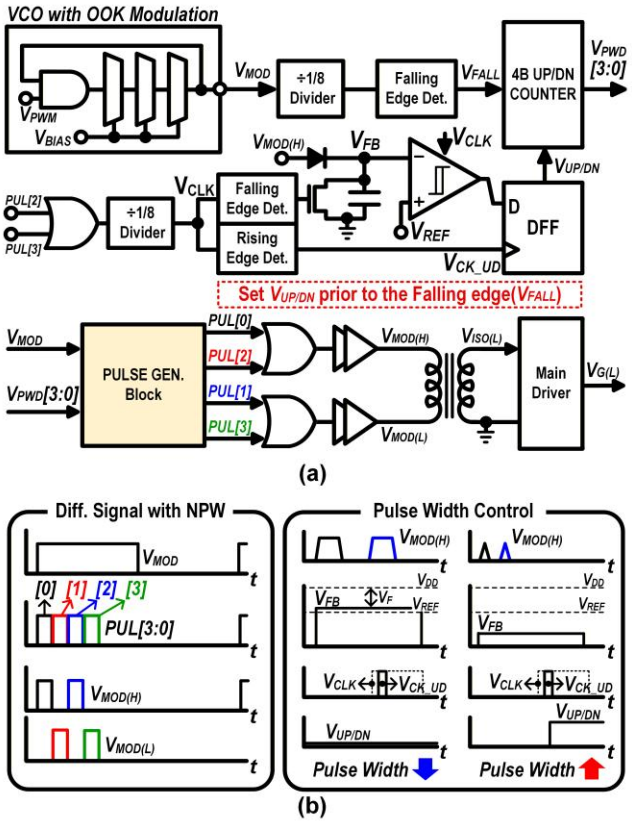

Fig. 3. (a) Overall architecture of the proposed multi-step pulse-width modulator (MPWM) including the pulse generation block and closed-loop feedback. (b) Timing diagram illustrating the counter up/down control mechanism based on the feedback voltage (V_{FB}) and reference voltage (V_{REF}).

inverted-PWM drive maintains volt–second balance and prevents long-term flux drift, an excessively long ON interval within a switching period enlarges the magnetizing-current swing. As the on-time increases, the RMS current rises accordingly, causing the source to deliver more real power even when the cycle-averaged volt-seconds are zero. This unnecessary current buildup leads to increased power loss and self-heating, which degrade sustained operational stability.

For systems in which extended ON durations may occur, it is therefore desirable to limit the pulse width to the minimum required to convey the intended information while suppressing the remainder of the drive interval. Narrowing the pulse width preserves the edge-based signal of the isolator but significantly reduces magnetizing/RMS current and overall power consumption. Before analyzing these relationships quantitatively, we first review the fundamental operating characteristics of the inductor that dictate this behavior.

$$V_L = L\frac{di(t)}{dt} \tag{1}$$

Integrating over a time interval $[t0, t0 + \Delta t]$ yields,

$$\Delta i = \frac{1}{L}\int_{t_0}^{t_0+\Delta t} v_L(\tau)d\tau \tag{2}$$

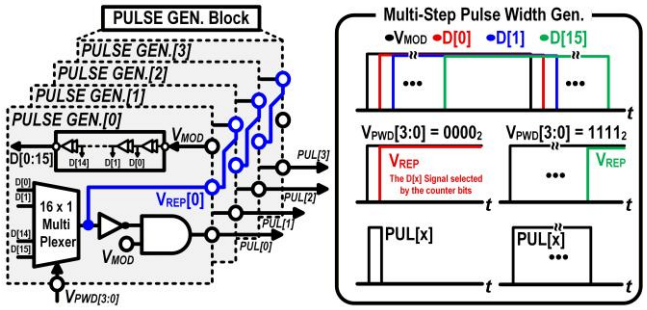

Fig. 4. (a) Detailed schematic of the pulse generation block featuring a 16-stage delay chain and a 16 x 1 multiplexer for pulse width selection. (b) Timing diagram of the multi-step pulse generation showing the relationship between V_{MOD}, V_{REP}, and the resulting *PUL[x]* signal for different V_{PWD}[3:0] codes.

For a constant applied voltage V_L, simplifies to $\Delta i = (\frac{V_L}{L})\,\Delta t$, showing that the current increment is proportional to the pulse width (application time). Even with volt-second balance that prevents DC drift, increasing t_{on} raised the magnetizing-current peak and stored energy, sharply increasing I^2R loss and driver stress; therefore, the design should use the minimum t_{on} that delivers the required transfer energy [9] .

B. Proposed MPWM for reducing the power consumption

Fig. 3 illustrates the overall architecture of the proposed multi-step pulse-width modulator (MPWM). The circuit consists of a pulse generation block that produces four sequential Narrow Pulse Width (*NPW*) signals for differential signal driving, and a closed-loop feedback control block. For timing control, the V_{MOD} signal is divided by 8 to ensure a sufficient period, and the falling edge of this signal serves as the main clock (V_{FALL}) for the counter. In the feedback loop, the peak voltage of the inductor node ($V_{MOD(H)}$) is detected as V_{FB} and compared with a threshold voltage V_{REF} to verify if sufficient power is delivered to the isolated output ($V_{ISO(L)}$). This comparison result is sampled at the rising edge (V_{CK_UD}), which is derived from the output pulses *PUL[3:2]* and precedes V_{FALL} in phase. This sampling determines the direction of the 4-bit up/down counter. If V_{FB} exceeds V_{REF}, the counter decrements to reduce the pulse width for minimizing power consumption. Conversely, if V_{FB} is lower than V_{REF}, the counter increments to extend the pulse width, ensuring robust signal transmission.

Fig. 4 details the schematic and timing diagram of the pulse generation block. This block consists of four identical sub-blocks (PULSE GEN.[0]~[3]) connected in a cascaded configuration to generate differential signals. Each sub-block is based on an adjustable delay Rising Edge Detector (RED) architecture for precise pulse width control. Internally, each pulse generation block contains a delay chain with 16 serially connected buffers. The 4-bit control signal V_{PWD}*[3:0]*, determined by the feedback loop, controls a 16×1 multiplexer to select one of the 16 delay paths. The signal denoted as V_{REP} is the exact D[x] signal selected according to these counter bits, and it serves as the trigger input for the subsequent stage. This ensures that the next pulse is generated immediately after the preceding pulse completes, creating a seamless sequence. By combining V_{REP} with the original input via an AND gate, a pulse is generated with a width corresponding to the delay time. As shown in Fig. 4(b), as the V_{PWD} code increases from 0000_2 to 1111_2, a longer delay path is selected, resulting in a wider output pulse PUL[x]. This process operates sequentially across the four blocks, ultimately generating four consecutive NPW signals (*PUL[0:3]*).

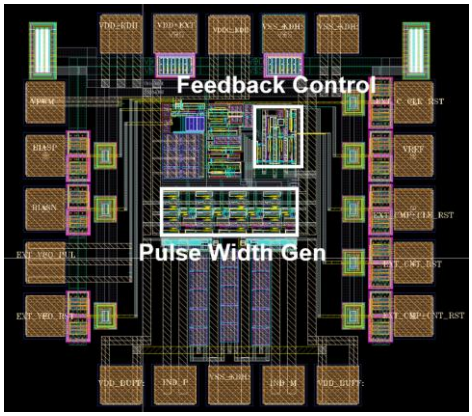

Fig. 5. Layout of the proposed multi-step pulse-width modulator.

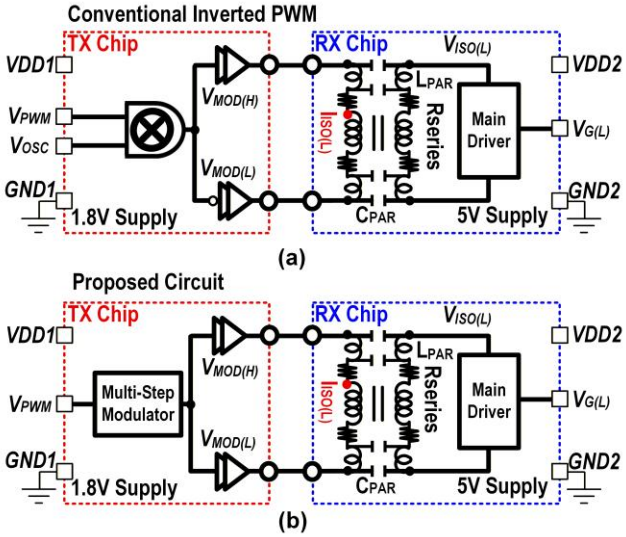

Fig. 6. Simulation test bench incorporating realistic parasitic elements (C_{PAR}, R_{series}, L_{PAR}): (a) Conventional inverted PWM method, and (b) Proposed circuit with the multi-step modulator.

III. RESULTS AND DISCUSSIONS

A. Chip layout of the proposed IC and simulation setup

Fig. 5 shows the layout of the proposed circuit, fabricated in the 0.18-μm CMOS process. The overall layout measures 759 μm x 735 μm, while the core itself occupies only 320 μm x 277 μm. The pulse-generator block occupies 250 μm x 83 μm, and the closed-loop feedback-control counter occupies 114 μm x 80 μm. Post-layout simulations were carried out for both the conventional and the proposed architectures using the simulation testbench shown in Fig. 6 and the same transformer R_{series} /L_{PAR}/C_{PAR} model listed in Table I. Due to the excessively large silicon area required for

TABLE I. Design Parameters for Post - Layout Simulation

Parameter	Value
$R_{Series}(\Omega)$	1
L_{PAR}(nH)	1
C_{PAR}(fF)	200
K(Coupling Coefficient)	0.94

a 105 nH inductance, the coupled inductor is not integrated into the core IC; instead, an external coupling inductor is used. The structural design of this inductive isolator is based on the approach introduced in [5]. To ensure a highly realistic evaluation, the simulation parameters (Table I) were explicitly derived from a commercial miniature SMD RF transformer, the Abracon ATL-1Z110611SR10LT[10]. This specific model provides a nominal primary inductance of 105 nH and a typical leakage inductance of 12 nH, which translates to a realistic coupling coefficient K of approximately 0.94. Furthermore, to thoroughly account for the additional parasitic effects introduced by wire bonding and PCB traces, these intrinsic component characteristics were intentionally combined with full R + C + CC extraction. To ensure a robust evaluation, off-chip parasitics were intentionally set to a worst – case scenario, incorporating a 1 nH parasitic inductance (L_{PAR}), 1 Ω series resistance (R_{series}), and a 200 fF parasitic capacitance (C_{PAR}). A primary inductance of 105 nH was selected to optimize the trade-off between signal integrity and power consumption. Given the operating frequency of 100 MHz and the minimum pulse width of approximately 1 ~ 2.5 ns, this inductance value ensures sufficient current slope ($\frac{di}{dt}$) for reliable signal transfer while limiting peak current to minimize resistive losses in the transformer driver.

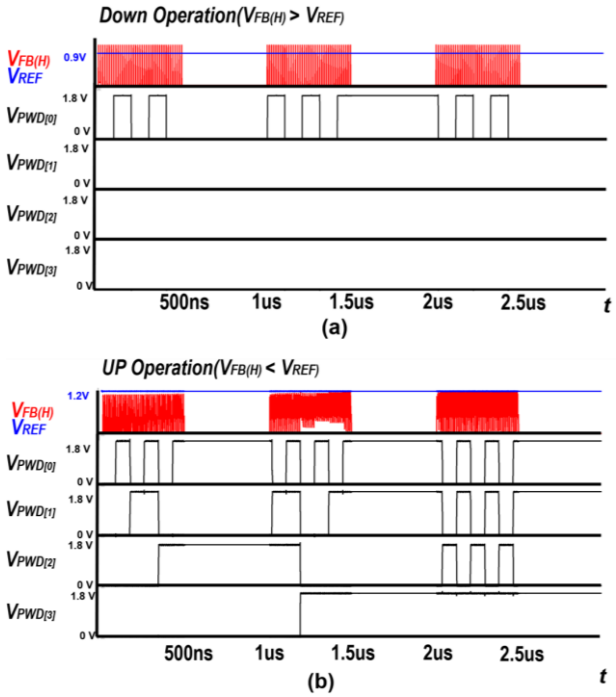

Fig. 6. Post-layout simulation waveforms of the counter operation driven by the feedback loop. (a) Down operation when V_{FB} exceeds V_{REF}, reducing the pulse width. (b) Up operation when V_{FB} is lower than V_{REF}, extending the pulse width.

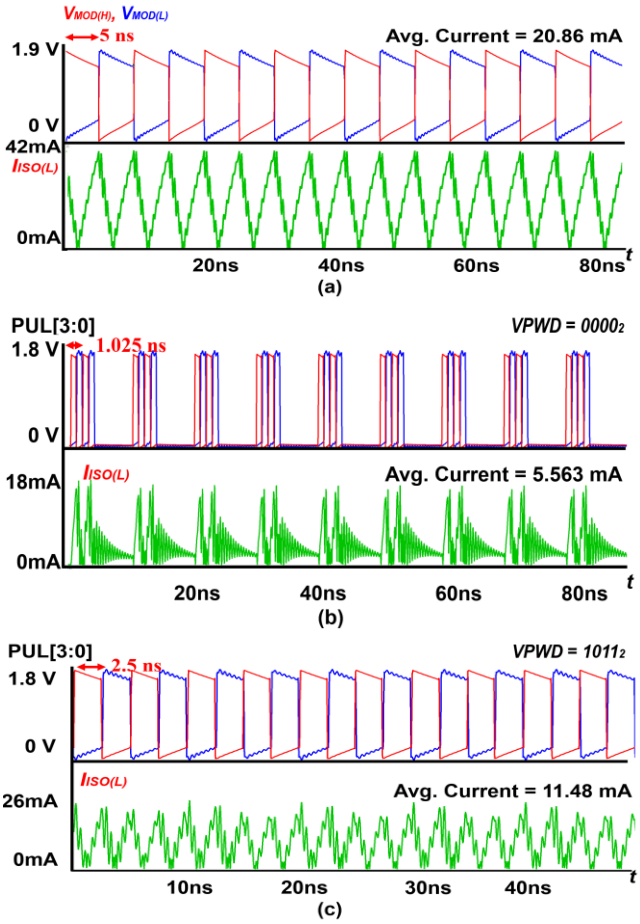

Fig. 8. Post-layout simulation waveforms comparing the isolator current (I_{ISO}) at 100 MHz. (a) Conventional inverted PWM method showing a high average current of 20.86 mA. (b) Proposed MPWM at the minimum pulse width condition (V_{PWD} = 0000_2) achieving 5.563 mA. (c) Proposed MPWM at the maximum-tested code (V_{PWD} = 1011_2) showing 11.48 mA.

selected to optimize the trade-off between signal integrity and power consumption. Given the operating frequency of 100 MHz and the minimum pulse width of approximately 1~2.5 ns, this inductance value ensures sufficient current slope ($\frac{di}{dt}$) for reliable signal transfer while limiting peak current to minimize resistive losses in the transformer driver.

B. Results of post layout simulation

Fig. 7 illustrates the counter operation waveforms driven by the feedback loop control described in Fig. 3. The V_{PWD} code dynamically adjusts step-by-step until V_{FB} reaches the target V_{REF}. The simulation results for the conventional scheme in Fig. 6(a) are presented in Fig. 8(a). The operating conditions were set to V_{PWM} = 1 MHz and V_{OSC} = 100 MHz, both with a 50% duty cycle. Under these conditions, the conventional architecture consumes an average current of 20.86 mA. In contrast, for the proposed rising-edge-detection-based multi-step pulse modulator shown in Fig. 6(b), Fig. 8(b) indicates that the minimum single-pulse width (V_{PWD} = 0000_2) is approximately 1.025 ns and increases by about 150 ps per counter step. At this minimum pulse width condition, the average current is 5.563 mA. Furthermore, for the maximum code V_{PWD} = 1011_2 where the effective multi-pulse width is 2.5 ns, the average current increases to

TABLE II. Performance Summary and Comparison with Previous Works

	This work	JSSC 2012 [5]	ADuM1100[11]	Unit
Process	0.18	0.54	-	μm
Modulation Frequency	100	-	-	MHz
Modulation scheme	OOK	Pulse polarity	Pulse polarity	-
Isolation barrier	Inductive	Inductive	Inductive	-
Current consumption	5.563 ~ 11.48	12.3	16.8	mA
Data rate	100	250	100	Mbps
Implementation Complexity	Low (Digital – intensive)	Medium (Analog – intensive)	Medium (Analog – intensive)	-
CMTI*	High (OOK – based)	Moderate (Pulse polarity)	Moderate (Pulse polarity)	-

* CMTI is qualitatively compared based on the inherent noise-robustness of the modulation schemes

approximately 11.48 mA (see Fig. 8(c)). Under these conditions, the conventional architecture consumes an average current of 20.86 mA. These results are consistent with the inductor current equation and accurately verify the impact of pulse width on the transformer's average current even under non-ideal parasitic conditions.

C. Discussion on Experimental Validation

To empirically validate the proposed MPWM, the IC was fabricated using a 0.18-µm CMOS process. Although the die has been wire-bonded to a test PCB, comprehensive measurement results are currently unavailable due to unexpected technical difficulties in the measurement setup during the initial testing phase. To ensure the validity of the proposed architecture despite this limitation, we rigorously verified the design through the comprehensive post-layout simulations defined in Section III.A. Our investigation shows that the non-ideal parasitic elements and imperfect coupling induce severe ringing on the secondary side (Rx) due to the high di/dt of nanosecond-scale pulses. While this Rx-side ringing can be mitigated by a typical snubber circuit in practice, more importantly, the primary-side (Tx) closed-loop feedback remains highly stable even under these conditions. This confirms that the proposed MPWM robustly achieves its core objective of drastically reducing current consumption while maintaining operational stability.

IV. CONCLUSION

This work demonstrates through post-layout simulations that the proposed MPWM can significantly reduce the power consumption of transformer-based signal isolators. The circuit implementation and post-layout simulation results are summarized in Table II. As detailed in Table II, the proposed MPWM is compared with a conventional pulse-polarity method [5]. While the architecture in [5] relies on edge-based transitions, the proposed work employs an OOK modulation scheme. Due to its continuous nature which allows for constant logic state verification, this OOK scheme inherently achieves a more robust CMTI compared to noise-sensitive pulse-polarity methods. The proposed MPWM effectively overcomes the traditional OOK's drawback of high static power consumption by utilizing narrow, multi-step pulses. Furthermore, the MPWM is highly digital-intensive, utilizing standard logic gates and delay chains, resulting in lower implementation complexity compared to conventional methods that require precise and power-hungry analog comparators at the receiver. By multi-step trimming the pulse to the minimum required width, the MPWM suppresses unnecessary volt-seconds *(V·s)* and DC magnetizing current, thereby lowering drive current and self-heating while improving energy efficiency. The approach readily scales to high-frequency, high-density applications, such as automotive and industrial power electronics, where thermal performance is critical. Future work will focus on debugging the hardware and performing a full experimental characterization with a commercial 1:1 RF transformer to fully verify the isolation performance and power savings in a real-world gate driver environment.

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Donghyun Kim He received the B.S. degree from Gyeongsang National University, Jinju, South Korea, in 2025. He is currently pursuing the M.S. degree at the same university. His current research interests include gate drivers for Wide Bandgap (WBG) semiconductors.

Minseob Shim (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2012 and 2018, respectively. From 2015 to 2016, he was a Visiting Researcher with the University of Michigan, Ann Arbor, MI, USA. From 2018 to 2022, he was with the Korea Electrotechnology Research Institute (KERI), Changwon, South Korea, as a Senior Researcher. Since 2022, he has been an assistant professor of Gyeongsang National University, Jinju, South Korea. His research interests include integrated power management systems, gate driver integrated circuit for wide bandgap devices, low voltage analog and mixed-signal integrated circuits, and analog-to-digital converter designs.