Design of Adaptive On-Time GaN DC-DC Converter with Active Gate Driving for Automotive System

Seulmin Ahn, Sunrae Roh and Jeongjin Roh
Department of Electrical Engineering, Hanyang University
E-mail : dkstmfals@hanyang.ac.kr

***Abstract* – The proposed paper introduces a single-stage Gallium Nitride (GaN) DC-DC converter employing adaptive on-time (AOT) hysteresis control including an active gate driving bootstrap (BST) gate driver. To achieve optimal one-cycle transient response during load variations, it incorporates a sample and hold-based load detecting transient enhancer for precise detection of load changes and accurate control of on-time extension. Additionally, an active gate driver utilizing a dv/dt detector is designed and applied to independently control dv/dt and di/dt, mitigating the trade-off between electromagnetic interference (EMI) and switching loss. The converter was fabricated using a 0.18-μm HV BCD 1P6M process with a total chip area of 1.05 × 0.80 mm. It converts up to 60-V input down to 3-V and operates in the frequency range of 0.95–9.5 MHz. Designed to support a wide automotive battery voltage range from 7 to 60 V, post-layout simulations show the output voltage ripple is as low as 2.9 mV at 12 to 3 V conversion and 4.2 MHz switching frequency, achieving a maximum efficiency of 91.3%.**

***Keywords*— GaN, Adaptive On-Time (AoT) Control, high-voltage (HV) gate driver, automotive**

I. INTRODUCTION

Recent developments in electric vehicles (EVs) and autonomous driving technologies have increased the significance of power systems in the automotive industry. In particular, DC-DC converters now play a key role in reliably supplying power to a wide variety of electronic subsystems within vehicles. Automotive batteries are subject to extreme conditions, such as starter surges and load dump events, resulting in wide voltage fluctuations from 7 V to 60 V [1], [2]. Therefore, DC-DC converters with a high step-down ratio are required to support this broad input voltage range while stably providing the output voltages required by each subsystem. Although cascade buck converters can achieve high step-down ratios, their use of dual inductors increases the total system area and exacerbates electromagnetic interference (EMI) issues [3]. To address these problems, single-stage DC-DC converters based on constant on-time (COT) hysteresis control are preferred. Additionally, to prevent malfunction or blackout of core components such as application processors (APs) and minimize system latency, the output voltage must remain stable even under abrupt load current transients. Compared to fixed-frequency current-mode control, COT hysteresis control offers faster transient response. However, under severe load step-up conditions, the fixed on-time (T_{ON}) and mandatory minimum off-time (T_{OFF}) can introduce response delays [4]. In particular, delays in logic circuits and gate drivers may restrict the minimum achievable T_{OFF}, leading to significant output voltage droop. Existing mechanisms for T_{ON} extension and load-change detection have been proposed, but they often suffer from increased silicon area and reduced accuracy. With the continuous increase in power density in automotive power systems, conventional silicon-based power switches are reaching their performance limits. As an alternative, gallium nitride (GaN) power devices have recently attracted considerable attention in automotive power electronics [5]. GaN switches exhibit much smaller parasitic capacitance at comparable breakdown voltage and ON-resistance (R_{ON}), supporting much higher switching frequencies at similar power conversion efficiencies than silicon devices [6]. Although low gate and output capacitance in GaN devices enables fast switching, it also leads to high dv/dt and di/dt

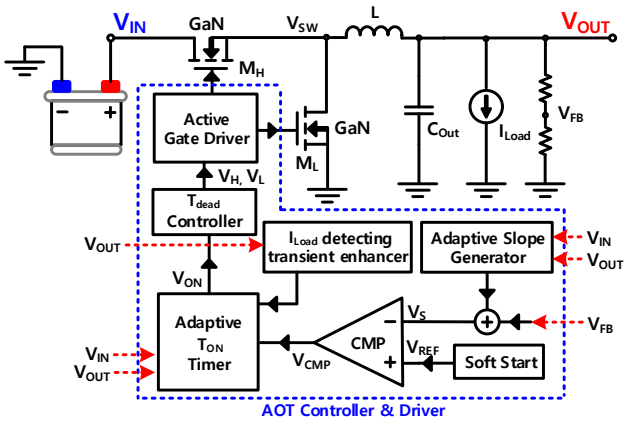

Fig. 1. Block diagram of the proposed GaN DC-DC converter

a. Corresponding author; jroh@hanyang.ac.kr

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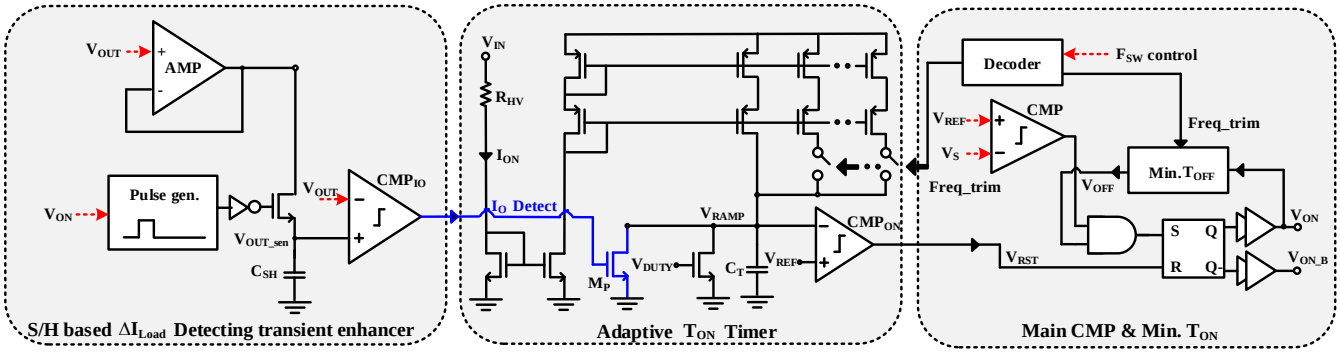

Fig. 2. Block diagram of proposed AOT controller

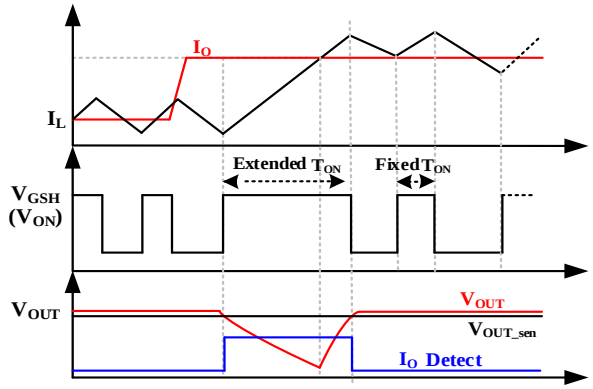

Fig. 3. Key waveform of transient enhancer

values, worsening EMI issues. Thus, filtering and noise suppression strategies must be considered in the design stage, particularly for automotive and high-frequency applications [7]. Furthermore, reducing dv/dt and di/dt to mitigate EMI inevitably increases switching losses, presenting a trade-off that must be optimally balanced. This paper proposes a single-stage GaN DC-DC converter employing adaptive on-time (AoT) hysteresis control and an active bootstrap (BST) gate driver. To achieve optimal one-cycle transient response during load variation, a sample-and-hold-based Load detecting transient enhancer is introduced for precise T_{ON} extension. In addition, to alleviate the trade-off between EMI and switching loss, an active gate driver featuring independent control of dv/dt and di/dt using a dv/dt detector is presented. The remainder of this paper is organized as follows: the system architecture and operation are introduced first, followed by the design of key circuit modules. The proposed concepts are validated by full transistor-level post-layout simulations, and conclusions are drawn at the end.

II. DESIGN METHODOLOGY

A. Proposed AOT Controller

Fig. 1 illustrates the overall block structure of the proposed circuit as well as the automotive battery voltage range. The system consists of a step-down power stage utilizing GaN switches, together with an AOT-based controller and an active gate driver circuit. Within the controller, the adaptive on-time timer, main comparator (CMP), load detecting transient enhancer, adaptive slope generator, and soft start block operate in close coordination. Integration of the active gate driver and dead-time (t_{dead}) controller provides optimal duty cycle operation for each switching device and enables efficient adaptation to both load transients and input voltage variations. All control and signal blocks are tightly interlinked, allowing rapid transient response and stable voltage conversion throughout the system. Fig. 2 shows the circuit diagram of the sample-and-hold (S/H)-based load detecting transient enhancer, AOT timer, and AOT controller including the main comparator and minimum T_{OFF} timer. Fig. 3 presents the node voltages for the gate-source voltage of M_H (V_{GSH}), V_{OUT}, and the transient enhancer under varying load conditions. The proposed transient enhancer enables precise one-cycle T_{ON} extension by monitoring dV_O/dt to detect load transients. At each switching period, the S/H circuit samples and stores V_{OUT} on a capacitor C_{SH}. When a variation in dV_O/dt occurs, the stored voltage in C_{SH} is compared with real-time V_{OUT}; upon detection of a discrepancy, the I_O detect signal transitions high. During this transient event, activation of M_P drives V_{RAMP} low and maintains V_{GSH} at a high level, thereby prolonging T_{ON} and increasing I_L. To maintain a near-constant switching frequency (f_{SW}), T_{ON} is generated by a current (I_{ON}) proportional to V_{IN}, charging C_T until a reference voltage is reached. Once I_L matches the load current I_O, the output voltage drop halts and voltage recovery begins. At this point, the I_O detect signal returns low and M_P deactivates promptly. The adaptive T_{ON} timer then resumes generating a fixed T_{ON} interval. Thus, the integration of the transient enhancer with T_{ON} extension minimizes output voltage undershoot during load transients, contributing to rapid settling and stable system operation.

B. Proposed active gate driver

Fig. 4 presents the block diagram of the proposed gate driver for a half-bridge power converter, including the multi-slew rate (MSR) driver and the dv/dt detector circuit. The driver is capable of controlling both the high-side and low-side n-channel GaN HEMTs (M_H and M_L). To maximize the floating DC supply rail (V_{BST}) and prevent overcharging, a bootstrap charging control (BCC) scheme is employed. The high-side gate driver integrates an up-level shifter to adaptively select the fast or slow gate drive path according to the switching stage, thereby achieving low EMI and high efficiency. By providing the appropriate gate current in fast and slow paths across the switching cycle, the high-side buffer simultaneously optimizes switching loss and EMI.

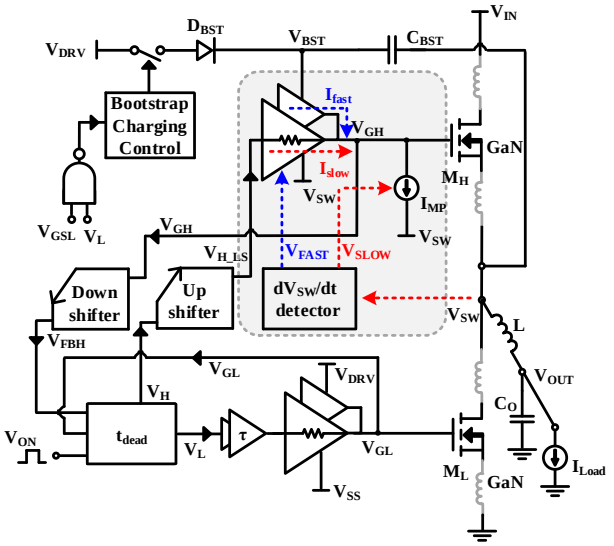

Fig. 4. Block diagram of proposed active gate driver

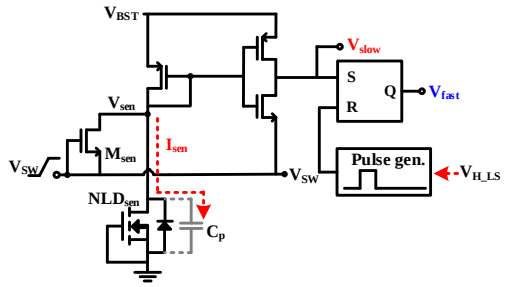

Fig. 5. Schematic of dV_{SW}/dt detector

Additionally, switching transition timings between M_H and M_L are managed by active dead time control, which ensure shoot-through prevention and minimizes the reverse conduction period during dead time.

Fig. 5 shows the circuit diagram of the dV/dt detector. The dv/dt detector senses the voltage slew rate at the switching node (V_{SW}) via the sensing transistor M_{sen} and the parasitic capacitance C_p inherent in LDMOS devices. When a rapid voltage transition occurs at V_{SW}, a transient current pulse is generated across C_p. This pulse is conveyed to an inverter and latch circuit, producing the V_{SLOW} and V_{FAST} signals. At the beginning of the Miller plateau (MP), the V_{SLOW} signal activates the slow path in the high-side driver to suppress EMI and voltage overshoot caused by excessive di/dt. Upon exiting the Miller plateau, the V_{FAST} signal drives the fast path, accelerating V_{GSH} rise and reducing propagation delay. The gate current is controlled in distinct regions, including the pre-switching ($V_{GSH} < V_{TH}$), drain current (I_{DS}) rise, Miller plateau, and post-switching ($I_{DS} = I_L$). Conventional gate resistor (R_G) techniques maintain a uniformly low gate current, resulting in slow V_{GSH} rise, greater propagation delay, and increased switching loss. In contrast, the proposed approach utilizes V_{SLOW} to restrict gate current only during switching, thereby mitigating EMI. After switching, V_{FAST} along with the standard buffer enables a rapid V_{GSH} rise and reduced switching loss. This design effectively decreases propagation delay while maintaining a comparable dv/dt profile to traditional methods.

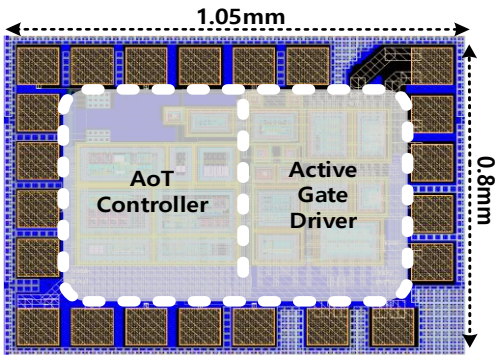

Fig. 6. Chip layout

TABLE I. Experimental Specifications

Symbol	Quantity
Input Voltage V_{IN}	7~60 V
Output Voltage V_{OUT}	3-12 V
Maximum I_{Load}	2A
Switching Frequency F_{SW}	0.98-9.5 MHz
Peak Efficiency	91.3%
Power Switches	EPC8002
Power Inductor L	2 μH
Output Capacitor C_F	22 μF

III. PERFORMANCE VERIFICATION

The proposed design is implemented using a 0.18-μm HV BCD 1P6M process, and Fig. 6 presents the chip layout. The die size is 0.88 mm². The converter employs a 2-μH inductor, a 22-μF output capacitor, and an EPC8002 GaN power switch to support a maximum I_O of 2 A. It operates over f_{SW} ranging from 0.95 to 9.5 MHz and achieves a maximum conversion ratio (CR) by stepping down 60 V to 3 V. The entire design has been verified through post-layout simulations at the transistor level.

Fig. 7 shows the post-layout simulation waveforms of the converter at steady-state for V_{OUT} = 3V. Under V_{IN} =12V and f_{SW} = 4.2MHz, the on-time and off-time of V_{SW} are 80 ns and 238.5 ns, respectively. At V_{IN} = 60V and f_{SW} =1.9MHz, they change to 21 ns and 378.2 ns. The output voltage ripple increases from 2.9 mV to 5.9 mV as the input voltage rises, while the inductor current also varies with operating conditions.

Fig. 8 illustrates the steady-state waveforms of the proposed active gate driver and dv/dt detector at V_{IN} =12V. When a rapid voltage transition of 16V/ns occurs at V_{SW}, the dv/dt detector generates a V_{SLOW} signal, activating the slow gate path during the Miller plateau. Afterward, the V_{FAST} signal restores the fast gate drive, enabling the gate voltage (V_{GSH}) to rise within 3.8 ns and minimizing turn-on delay. Gate drive current (I_G) modulation is clearly observed, confirming segment-wise dynamic control.

Fig. 9 shows the post-layout simulation waveforms of the converter at load transient.

Finally, Table I summarizes the main specifications and operating conditions of the proposed GaN DC-DC converter.

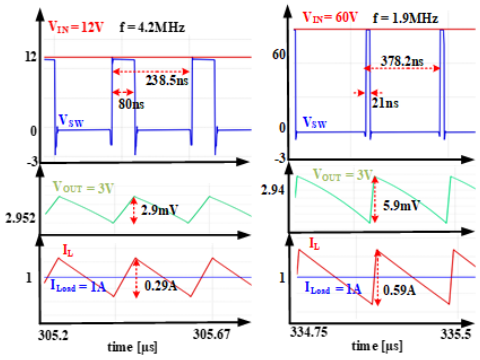

Fig. 7. Simulation result of steady state operation

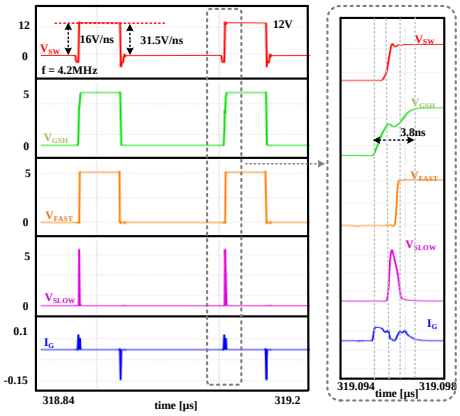

Fig. 8. Simulation result of proposed active gate driver

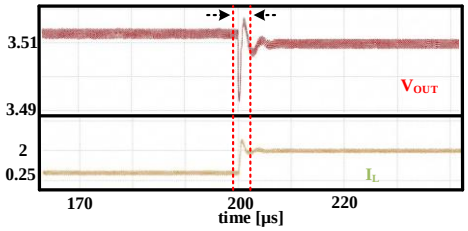

Fig. 9. Simulation result of load transient response

IV. CONCLUSION

An integrated, single-stage GaN DC-DC converter using adaptive on-time hysteresis control and an active gate driver has been demonstrated. The proposed sample-and-hold-based transient enhancer enables precise one-cycle T_{ON} extension, while the dv/dt detector-based gate driver achieves simultaneous EMI reduction and fast switching. Post-layout simulation results confirm stable operation over a wide 60V to 3V input range, effective transient response, and minimized output ripple. The design provides significant improvements in efficiency and reliability for automotive power applications.

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Seulmin Ahn received the B.S. degree in electronic engineering from Hanyang University, Ansan, Korea, in 2024. He is currently working toward the M.S. degree in electronic engineering at Hanyang University, Ansan, Korea. His current research interests include integrated power managements ICs design and high-performance DC-DC Converter design.

Sunrae Roh received the B.S. degree in electronic engineering from Hanyang University, Ansan, Korea, in 2025. He is currently working toward the M.S. degree in electronic engineering at Hanyang University, Ansan, Korea. His current research interests include integrated power managements ICs design and high-performance DC-DC Converter design.

Jeongjin Roh (Senior Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 1990, the M.S. degree in electrical engineering from Pennsylvania State University, in 1998, and the Ph.D. degree in computer engineering from The University of Texas at Austin, in 2001. From 1990 to 1996, he was as a Senior Circuit Designer for mixed-signal products with Samsung Electronics, Giheung, South Korea. From 2000 to 2001, he was a Senior Analog Designer for delta-sigma data converters with Intel Corporation, Austin, TX, USA. He joined the Faculty of Hanyang University, Ansan, South Korea, in 2001. His research interests include power management circuits and oversampled delta-sigma converters.