Design of a 2nd-Order Noise-Shaping SAR ADC Using Cascaded Floating Inverter Amplifiers

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Abstract - **This paper presents a 2nd-order noise-shaping successive approximation register (NS-SAR) ADC employing cascaded floating inverter amplifier (FIA) integrators. Key design considerations for the cascaded FIA-based loop filter are systematically analyzed and incorporated into the proposed architecture. The ADC is designed to achieve stable loop dynamics and enhanced noise-shaping efficiency while maintaining low power consumption. The chip was designed in a TSMC 0.18 µm standard CMOS process and achieves 83.98 dB SNDR, 89.15 dB SFDR, and a dynamic range of 83.04 dB while consuming 81.13 µW at a 2-MHz sampling rate with an oversampling ratio of 256, corresponding to a Schreier figure-of-merit of 160.80 dB.**

***Keywords*— Noise-shaping SAR ADC, cascaded floating inverter amplifier (FIA), low-power ADC, asynchronous SAR logic, switched-capacitor integrator.**

I. INTRODUCTION

With the advancement of communication technologies, sensor applications, and healthcare systems, the development of Internet-of-Things (IoT) systems has been rapidly increasing every year. Such systems, which are powered by battery-operated or energy-harvesting techniques, require miniaturization and low-power operation while also demanding high-resolution hardware to ensure accurate sensing [1]–[3]. Accordingly, the need for low-power and high-resolution analog-to-digital converters (ADCs) continues to grow. In IoT-based sensing applications, successive-approximation-register (SAR) ADCs are predominantly used because their excellent power efficiency, simple circuit structure, and high operating speed make them highly suitable for battery-powered IoT sensor systems [4], [5]. However, SAR ADCs suffer from limited scalability and area efficiency when achieving resolutions above 12 bits due to the nonlinearity and capacitance growth of the capacitor digital-to-analog converter (C-DAC).

For high-resolution conversion of low-frequency signals, delta-sigma (ΔΣ) ADCs are widely adopted. They employ noise-shaping (NS) and oversampling techniques to push the quantization noise in the low-frequency band toward higher frequencies through a loop filter, achieving higher resolution after digital filtering. However, achieving a high oversampling ratio (OSR) within a given signal bandwidth requires a high sampling frequency, which in turn increases the high-speed operation and power consumption requirements of the quantizer and the loop filter. Furthermore, although the linearity requirement is relaxed by using low-resolution DACs and quantizers, the active integrators in the loop filter still require high gain and wide bandwidth to maintain accurate filtering and fast settling. Therefore, balancing gain, bandwidth, and power consumption in the operational transconductance amplifier (OTA) design becomes crucial.

To overcome these limitations, noise-shaping SAR (NS-SAR) ADC architectures have been proposed. An NS-SAR ADC combines the fast conversion speed and power efficiency of SAR ADCs with the high-resolution noise-shaping capability of ΔΣ ADCs. By employing a low-resolution SAR quantizer, linearity constraints are mitigated while achieving both low-power and high-resolution characteristics. This architecture is particularly effective for readout integrated circuits (ROICs) used in biosensors and gas sensors, which require a wide dynamic range and compact area while operating with slow response characteristics in the tens-of-hertz to kilohertz range [6], [7]. However, even in active loop-filter implementations, the power consumption associated with OTAs remains a major limitation. Therefore, this work analyzes a second-order NS-SAR ADC employing a cascaded floating-inverter-amplifier (FIA)-based loop filter. In particular, the gain, pole locations, load capacitance, and time-varying device parameters are examined to investigate the stability–bandwidth trade-off of the switched-capacitor integrator loop.

II. ARCHITECTURE OF THE SECOND-ORDER NS SAR-ADC

Fig. 1 illustrates the block diagram of the conventional FIR-IIR loop filter based NS-SAR ADC architecture. The overall system consists of a C-DAC, a loop filter, a comparator, and SAR logic. The input voltage V_{IN} is sampled through bottom-plate sampling together with the reference voltages V_{REFP} and V_{REFN}, and the residue voltage V_{RES} is generated based on the comparison result of the SAR operation. The residue voltage is accumulated and filtered through a loop filter composed of both finite-impulse-response (FIR) and infinite-impulse-response (IIR) integrator stages. The loop filter shifts the quantization noise, which is uniformly

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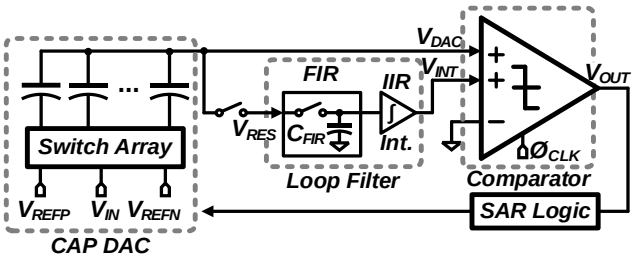

Fig.1. Conventional FIR-IIR loop filter based NS SAR ADC architecture.

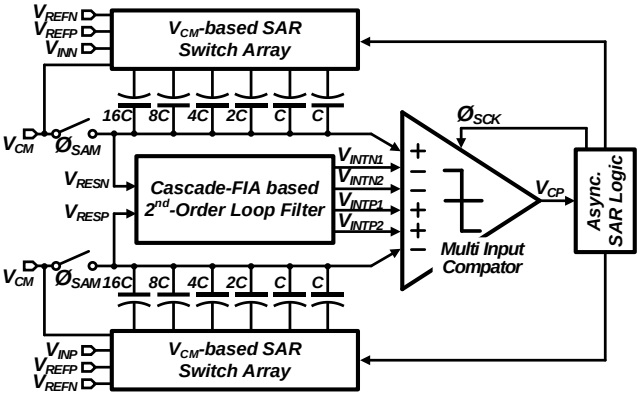

Fig.2. Top level schematic of the proposed NS SAR ADC.

distributed over the entire frequency band, to the high-frequency region. The output voltage of the loop filter, V_{INT}, participates in the quantization-noise feedback process along with the DAC output voltage V_{DAC} and the digital output code generated by the dynamic comparator. The SAR logic determines the digital bit for the next conversion cycle and updates the switching configuration of the C-DAC based on the comparison result, generating the control signals required for both SAR conversion and quantization-noise feedback. In this NS-SAR ADC architecture, key design considerations include the linearity of the multi-bit C-DAC, parasitic capacitances that cause coefficient variations in the loop filter, and the power consumption and stability of the FIA-based integrators. A detailed analysis of these factors is essential for achieving optimal performance.

Fig. 2 shows the top-level schematic of the proposed second-order noise-shaping SAR ADC. To enhance energy efficiency, a VCM based SAR ADC structure is employed. The SAR conversion operates under asynchronous SAR logic and consists of a 5-bit SAR conversion controlled by the asynchronous SAR clock $Ø_{SCK}$, followed by a residue sampling phase using a dummy capacitor to define the SAR residue for subsequent integration. The C-DAC is implemented using MoM(Metal-Oxide-Metal) capacitors, where the unit capacitance is 12.57 fF and the total capacitance is 0.4 pF. The input signal is applied in differential form and sampled at the bottom plates of the C-DAC. Three differential signal pairs are compared using a multi-input dynamic comparator assisted by a pre-amplifier based strong-arm latch [8]. These signal pairs consist of the differential residue voltages V_{RESP} and V_{RESN}, the differential output voltages of the first integrator V_{INTP1} and V_{INTN1}, and

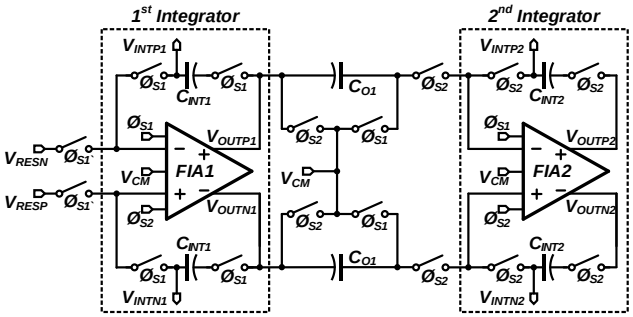

Fig.3. Designed second-order loop filter employing cascaded FIA-based integrators.

the differential output voltages of the second integrator V_{INTP2} and V_{INTN2}.

Fig. 3 shows the loop-filter circuit of the proposed second-order NS-SAR ADC based on a cascaded FIA structure. The loop filter consists of two switched-capacitor (SC) integrators. After the SAR ADC conversion is completed, the residue voltages V_{RESN} and V_{RESP} are generated and applied to the first integrator, where the integration is performed and the resulting voltages are sampled onto the integrating capacitors C_{INTP1} and C_{INTN1}. In the following sampling phase, the output voltages of the first integrator, V_{OUTP1} and V_{OUTN1}, are transferred to the input of the second integrator through the coupling capacitor C_{O1}, where the second integration is carried out, thereby realizing second-order noise-shaping within the loop.

The integrating capacitor C_{INT1} is selected to be 0.4 pF, which is equal to the total capacitance of the C-DAC, while C_{O1} and C_{INT2} are each chosen as 0.2 pF considering the settling behavior of the first-stage integrator. Each stage of the loop filter employs a cascaded FIA structure, which operates without static bias current and therefore achieves higher energy efficiency compared to a conventional OTA-based integrator. Furthermore, compared with a single-stage FIA, the cascaded FIA provides higher gain and a wider bandwidth, enabling high-speed operation.

III. Cascaded FIA-Based Loop Filter Design and Analysis

Fig. 4 presents the schematic of the two cascaded FIA structures corresponding to those shown in Fig. 3. Each stage is implemented with a single inverter-based amplifier and operates according to the switching phases controlled by the $Ø_{S1}$ and $Ø_{S2}$ switches in Fig. 3. Although the FIA architecture provides a wide output swing, high power efficiency, and stable common-mode behavior, making it suitable for NS-SAR ADC applications, the conventional single-stage FIA suffers from low output resistance, which limits its ability to achieve high gain. To address this limitation, a cascode FIA structure, in which a cascode transistor is stacked on top of the original FIA to increase gain, has been proposed [9]. However, this cascode structure inherently reduces the output swing and slows down the settling behavior, which in turn decreases the bandwidth and makes high-speed operation difficult. In contrast, the cascaded FIA structure connects two FIA stages in series, enabling the achievement of both higher gain and a wide

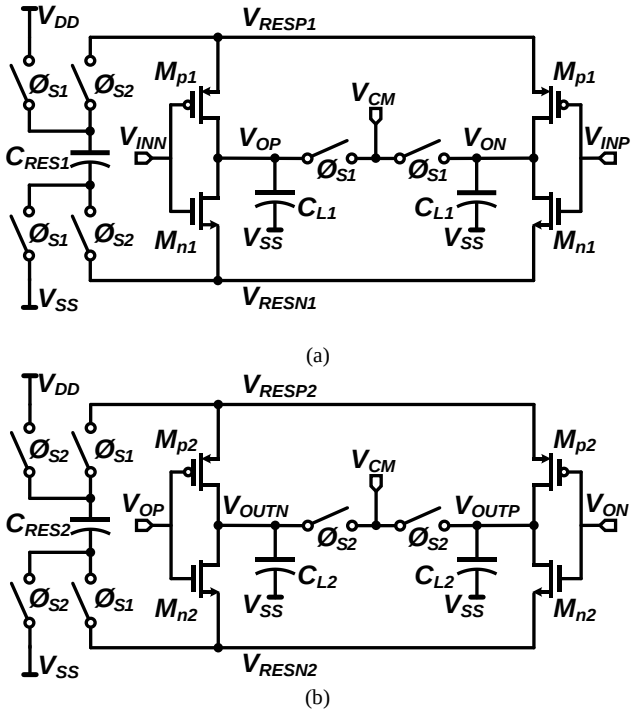

Fig.4. Cascaded FIA structures in each stage of the integrator, (a) First stage, (b) Second stage.

output swing simultaneously. This structure maintains power efficiency comparable to that of a single FIA because it uses only dynamic current due to the current-reuse characteristic of the FIA. However, in the cascaded configuration, the two FIA stages form a feedback loop, making it essential to consider loop stability in the design [10], [11]. The stability of the cascaded FIA is determined by the pole frequencies formed at the output nodes of each stage. Since the second-stage output drives a larger load capacitance, the pole ω_{p2} becomes the dominant pole of the cascaded FIA. Therefore, an analysis of pole locations based on the output load and output impedance of both the first- and second-stage integrators is required.

Based on the initial amplification phase, the pole frequencies at the output nodes of the first and second stages can be approximated as follows.

$$\omega_{int1,p1} \cong \frac{1}{R_{out1}C_{int1,eff1}}, \omega_{int1,p2} \cong \frac{1}{R_{out2}C_{int1,eff2}} \quad (1)$$

$$\omega_{int2,p1} \cong \frac{1}{R_{out1}C_{int2,eff1}}, \omega_{int2,p2} \cong \frac{1}{R_{out2}C_{int2,eff2}} \quad (2)$$

R_{out1} and R_{out2} represent the output impedances of the first-stage and second-stage FIAs, respectively.

C_{int1_eff1} and C_{int1_eff2} denote the effective output capacitances of each stage within the first integrator FIA, while C_{int2_eff1} and C_{int2_eff2} represent the corresponding effective output capacitances of the second integrator FIA. C_{int1_eff1} and C_{int2_eff1} include C_{L1} and the parasitic input capacitances of the second-stage transistors, whereas C_{int1_eff2} and C_{int2_eff2} are determined by C_{L2} and the output loading of the integrator, including the coupling capacitor C_{O1} and the parasitic capacitance at the comparator input node.

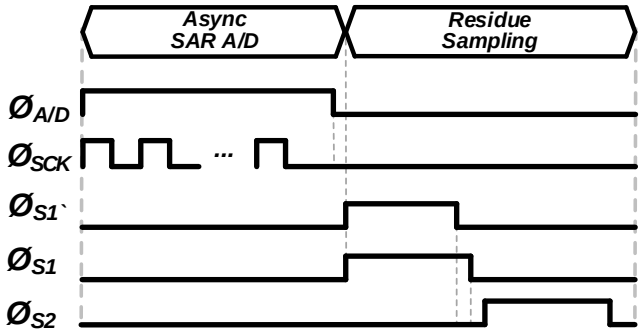

Fig.5. Timing diagram of the proposed NS SAR ADC operation.

When the two poles in the cascaded structure become close to each other, the loop exhibits a sharp roll-off of 40 dB per decade in its frequency response, and the phase response rapidly approaches -180 degrees, resulting in a reduced phase margin. Therefore, it is essential to ensure that ω_{p2} acts as the dominant pole during the initial amplification interval, while ω_{p1} is placed at a sufficiently higher frequency to maintain adequate pole separation. To achieve this, the parameters R_{out2}, and C_{int2_eff2} of the second stage were adjusted so that ω_{p2} is positioned at a lower frequency, while the first-stage pole is placed at a relatively higher frequency, thereby widening the spacing between the two poles and securing sufficient phase margin. Furthermore, because the FIA operates using the charge stored in the reservoir capacitor, the transistor parameters exhibit time-varying behavior in which $g_m(t)$ decreases and $r_o(t)$ increases as the amplification phase progresses. As a result, $\omega_{p1}(t)$ and $\omega_{p2}(t)$ gradually move toward lower frequencies over time, with the second-stage pole $\omega_{p2}(t)$ shifting more inward due to the reduction in current. Accordingly, the circuit was designed so that the initial bandwidth is sufficiently wide to guarantee fast settling, and as time progresses, ω_{p1} shifts faster than ω_{p2}, thereby increasing the phase margin. Based on this design strategy, the widths and lengths of each stage in the cascaded FIA were adjusted so that the rate of current reduction differs between stages. C_{L1} and C_{L2} determine not only the pole frequencies but also the output noise magnitude and settling time of the FIA; therefore, their values were selected by jointly considering pole placement, noise characteristics, and settling behavior. In general, the load capacitance and coupling capacitance of the second stage were not excessively increased to prevent C_{eff2} from becoming unnecessarily large, and the capacitances were chosen considering the load of each stage. Finally, because C_{O1} is larger than C_{COMP_IN}, C_{L2} of the second integrator was selected to be larger than C_{L1} of the first integrator. The reservoir capacitor of the first-stage integrator, which affects $g_m(t)$, response speed, and noise characteristics, was chosen by considering the required bandwidth, settling time, and area during the initial amplification interval; as a result, C_{RES2} was selected to be smaller than C_{RES1}, and the final values were set to 12 pF and 4 pF, respectively.

Fig. 5 shows the timing diagram of the second-order cascaded-FIA-based NS-SAR ADC corresponding to Fig. 2 to 4. During the Asynchronous SAR Conversion Phase, the input-voltage sampling and inversion are performed in synchronization with the enable signal $Ø_{A/D}$ generated by the

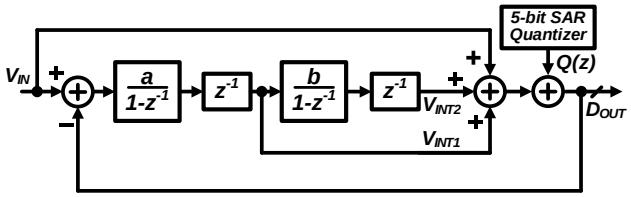

Fig.6. Equivalent z-domain model of proposed NS SAR ADC.

SAR logic, while the SAR conversion clock $Ø_{SCK}$ is activated to execute the 5-bit SAR ADC operation and store the resulting digital output code. In the first-stage integrator's Residue Integration Phase, after the 5-bit SAR operation is completed, the residue voltage V_{RES} is stored on the top plate of the C-DAC and then delivered to the first integrator through the integrator input switch $Ø_{S1'}$. During this period, the first-stage integrator operates according to the switching phase $Ø_{S1}$ and performs integration using the charge stored in the reservoir capacitor, generating the voltages V_{INTP1} and V_{INTN1}, while simultaneously storing charge into the reservoir capacitor of the second-stage FIA. In the second-stage integrator's Residue Integration Phase, the integrator operates according to the switching phase $Ø_{S2}$. Based on the sampled voltages from the first-stage integrator and the charge stored during the $Ø_{S1}$ phase, the second-stage integrator performs integration and generates V_{INTP2} and V_{INTN2}, during which the reservoir capacitor of the first-stage FIA is charged. Through this sequential operation, the integrators and reservoir capacitors of each stage alternately undergo charging and discharging depending on the switching phases. As a result, the residue voltage is accumulated step-by-step throughout the loop, enabling second-order noise-shaping operation.

Fig 6. shows the z-domain equivalent model block diagram of the proposed 2nd-order noise-shaping SAR ADC. The designed architecture is based on a 2nd-order CIFF (cascaded-of-integrators feedforward) structure. By referring to Fig. 2 and Fig. 3, the loop filter transfer function H(z) for the two integrators with coefficients a and b is given as follows:

$$H(z) = \frac{az^{-1}}{1-z^{-1}} + \frac{abz^{-2}}{(1-z^{-1})^2} \tag{3}$$

In the transfer function, the coefficients a and b correspond to the first and second integrators, respectively. The loop filter was designed such that the capacitors are selected to ideally achieve a = 1 and b = 1. Accordingly, the ideal 2nd-order noise transfer function (NTF) is given as follows:

$$NTF_{ideal}(z) = (1-z^{-1})^2 \tag{4}$$

This results in a second-order high-pass noise-shaping characteristic, where a zero is located at z = 1. However, in the actual circuit implementation, the gain coefficients become smaller than their ideal values due to the parasitic capacitances at the integrator output nodes, wiring parasitics, switch and transistor input capacitances, as well as PVT variations of the capacitors. This deviation can be expressed as follows:

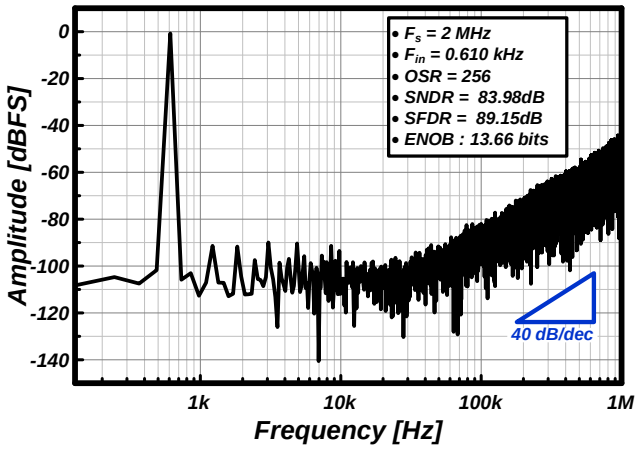

Fig.7. Post-simulation PSD results of NS SAR ADC at 2MHz f_s.

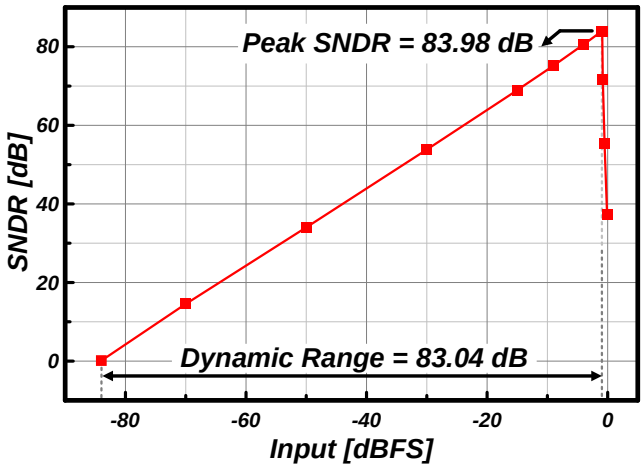

Fig.8. Post-simulation results of input amplitude vs SNDR.

$$a_{eff} = a \cdot \frac{C_{DAC}}{C_{INT1} + C_{par1}},\ b_{eff} = b \cdot \frac{C_{O1}}{C_{INT2} + C_{par2}} \tag{5}$$

The terms c_{par1} and c_{par2} represent the parasitic capacitances at the inputs of the first and second integrators, respectively. Due to the influence of these parasitic components, the effective coefficients a_{eff} and b_{eff} become smaller than their ideal values (a_{eff}, b_{eff} < 1), which reduces the NTF slope in the frequency region and consequently leads to degraded performance compared to the theoretical expectation. Although variations in the effective coefficients occur due to parasitic capacitances in practical circuit implementations, such coefficient variation can be mitigated by increasing the input transistor size of the integrator or by enlarging the CDAC capacitance. However, such choices incur additional chip area and power consumption, resulting in a design trade-off. Considering these factors, the design was optimized in this work, and the final implementation achieves effective coefficients of a_{eff} = 0.91 and b_{eff} = 0.94.

IV. SIMULATION RESULTS

Fig. 7 presents the post-simulation results of the designed ADC. The simulation was performed with a sampling frequency of f_s = 2 MHz, and a sinusoidal input with a frequency of f_{in} = 0.610 kHz was applied. The oversampling

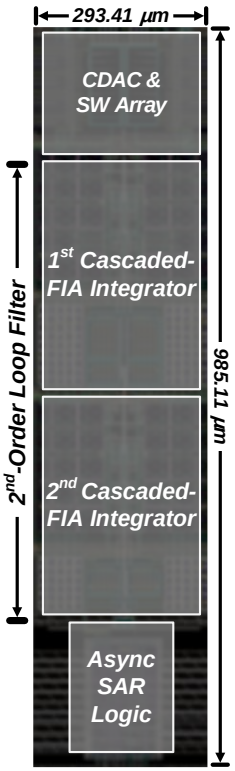

Fig.9. Chip layout

ratio (OSR) was set to 256. According to the post-simulation results, when the input amplitude was set to –0.94 dBFS, the proposed ADC achieved an SNDR of approximately 83.98 dB and an SFDR of 89.15 dB, corresponding to an ENOB of about 13.66 bits. The ADC consumes 81.13 μW of power. These results indicate that the proposed loop filter provides sufficiently stable gain and operating bandwidth for both integrators, enabling high-resolution conversion of low-frequency signals in the kHz range.

Fig. 8 shows the post-simulated SNDR performance with respect to input amplitude. The conditions were selected to be identical to those used in Fig 7. The maximum SNDR was achieved when the input amplitude was set to –0.94 dBFS. When the input amplitude exceeded this value, distortion occurred due to saturation of the SAR ADC quantizer. The proposed ADC achieves dynamic range of 83.04 dB.

Fig. 9 illustrates the core layout of the designed second-order NS-SAR ADC. The proposed circuit was implemented in the TSMC 1-Poly 6-Metal 0.18 μm standard CMOS process, and the core circuit occupies an area of 0.289 mm². The reference voltage required for ADC operation is supplied externally, and the clock provided from off-chip is applied through the asynchronous SAR logic to operate the internal ADC circuitry. Table I presents the performance results of the proposed NS-SAR ADC.

V. CONCLUSION

This paper presents the design of a 2nd-order noise-shaping SAR ADC employing a loop filter based on cascaded floating-inverter amplifiers (FIAs). The proposed circuit was implemented using the TSMC 0.18 μm 1P6M standard CMOS process. It achieves second-order noise shaping through a 5-bit asynchronous SAR ADC combined with a cascaded FIA-based second-order loop filter. The ADC consumes 81.13 μW of power and, under a 2-MHz sampling frequency, and an OSR of 256, it achieves an SNDR of 83.98 dB, a dynamic range of 83.04 dB, and an SFDR of 89.15 dB, resulting in a figure-of-merit (FoM) of 160.80 dB.

TABLE I. Performance Table

Parameter	Value
Technology	TSMC 0.18μm CMOS Process
Supply Voltages	1.5 V
Power Consumption	81.13 μW
Sampling Frequency	2 MHz
OSR	256
SNDR	83.98 dB
SFDR	89.15 dB
Dynamic Range	83.04 dB
*FoM	160.80 dB

$^{*}FoM = SNDR + 10log\frac{Bandwidth}{Power}$ (dB)

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