7.5-GHz Low Local Oscillator Pumping Cryo-CMOS Parametric Amplifier for Quantum Computing

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***Abstract* - This paper presents the design of a cryo-CMOS parametric amplifier suitable for operation at 4K and mK temperatures within the readout chain of quantum computers. It was experimentally verified that thermal noise introduced through the LO input path degrades the noise performance of the circuit. A parametric amplifier design capable of functioning with low local oscillator (LO) pumping power was proposed to mitigate this problem, providing a significant attenuation margin to safeguard against external noise. By optimizing the core parasitic resistance and adjusting the matching point, the parametric amplifier was measured 0 dB gain with 20 dBm LO power at 300K, and 15.2 dB gain with 0dBm LO power at 4K.**

***Keywords*—Cryogenic, CMOS, parametric amplification, low noise, low power**

I. INTRODUCTION

Quantum computing, unlike conventional binary-based computers, leverages quantum mechanical phenomena such as superposition and entanglement to perform computations. This advanced technology enables the rapid simulation of material structures and chemical reactions, thereby contributing to drug discovery [1]. Furthermore, quantum cryptographic techniques facilitate the establishment of enhanced security systems [2]. Recent studies have also indicated that quantum machine learning algorithms can achieve superior learning performance compared to classical machine learning approaches [3]. Notably, IBM has recently succeeded in implementing a 127-qubit quantum processor, solidifying its leadership in the field of quantum computing [4]. As the scalability of qubits increases, the development of circuit technologies capable of controlling and reading these qubits becomes imperative.

The transmon qubit has been actively investigated as a scalable solution for quantum computing. To read out the qubit state, a test signal is applied to the qubit at sub-millikelvin (mK) temperatures, and the reflected signal carries information about the qubit state. Since the power level of the reflected signal is extremely low, approximately -125 dBm, the noise characteristics of the receiving system

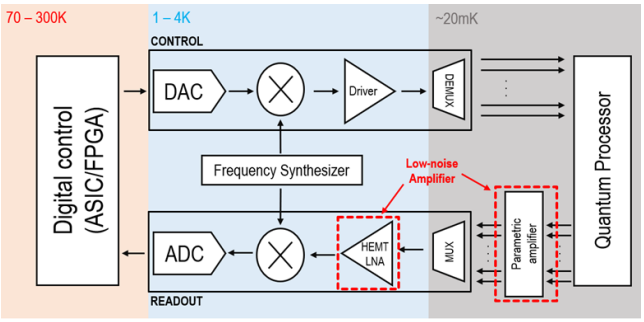

Fig. 1. RF reflectometry qubit readout block diagram.

are a critical specification in the overall system design as shown in Fig. 1. Additionally, maintaining sub-mK temperatures is crucial for the operation of transmon qubits, which imposes constraints on heat capacity. Consequently, conventional low-noise amplifiers (LNAs) that consume substantial DC power are unsuitable for this application. To address this limitation, the Josephson Parametric Amplifier (JPA), which operates without DC power consumption, is commonly utilized in the first stage of the readout chain as shown in Fig. 1. While JPAs offer excellent noise and gain performance, their reliance on off-chip components poses scalability challenges. As a result, there is growing interest in implementing parametric amplifiers using CMOS technology [5].

This study proposes a parametric amplifier circuit implemented using CMOS processes. By employing a single-balanced mixer-type parametric amplifier along with a diplexer, this design presents a low-power, compact-area system compared to conventional double-balanced architectures. This approach aims to improve scalability and efficiency, addressing critical challenges in the practical realization of quantum computing hardware.

II. PARAMETRIC AMPLIFIER DESIGN

The structure of the proposed parametric amplifier is illustrated in Fig. 2. This circuit is designed in a single-balanced mixer configuration, comprising a diplexer, a varactor core, and an RF matching network. A 7.5 GHz signal, reflected from the qubit, is applied to the RF port, while a 15 GHz LO signal is generated and applied via a signal generator. The diplexer converts these signals into differential signals and delivers them to the varactor core. Due to the nonlinear reactance of the varactor, the combined signals undergo amplification and are subsequently reflected.

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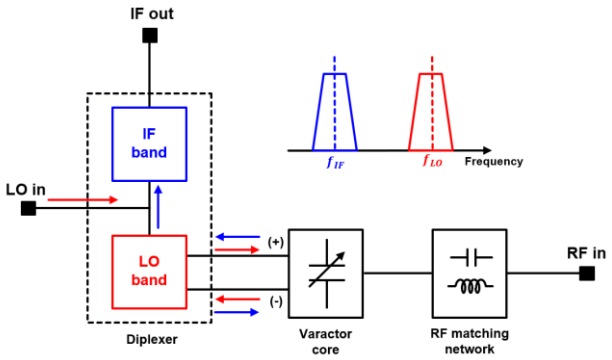


Fig. 2. Proposed parametric amplifier structure.

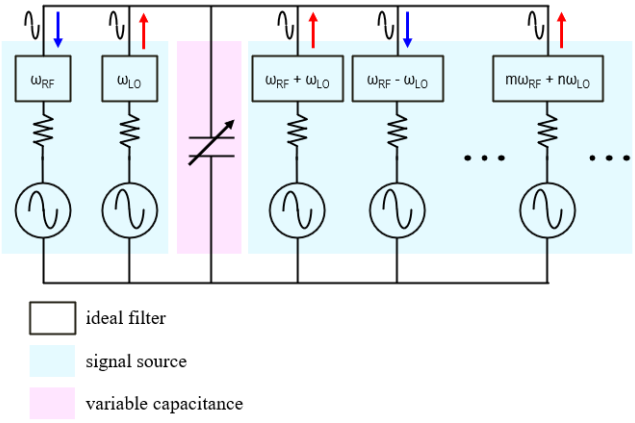


Fig. 3. Ideal parametric amplifier.

The amplified signal is then separated and extracted through the IF port via the diplexer.

A. Parametric amplifier gain/noise

The gain and noise equations of the parametric amplifier are derived under the assumption of an ideal filter, as illustrated in Fig. 3. The RF and LO frequency sources are applied around the variable capacitor, and due to the nonlinear variation of the capacitance, frequency mixing occurs. The energy of the mixed frequency components satisfies the following relationship [6], [7].

$$\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\frac{mP_{m,n}}{mf_{\mathrm{LO}}+nf_{\mathrm{RF}}}=0 \quad (1)$$

$$\sum_{m=-\infty}^{\infty}\sum_{n=0}^{\infty}\frac{nP_{m,n}}{mf_{\mathrm{LO}}+nf_{\mathrm{RF}}}=0 \quad (2)$$

When the mixed frequencies satisfy the condition $\omega_{\mathrm{RF}} < \omega_{LO}$, resulting in an inverted frequency band, the power applied from the LO signal source is converted into RF and IF frequency power components, leading to amplification, as described by Equations (1) and (2). Here, $P_{m,n}$ denotes the power at $mf_{\mathrm{LO}} + nf_{\mathrm{RF}}$. When a high-power LO signal is applied to the variable capacitor, its capacitance varies over time according to Equation (3). This variation, combined with the applied RF signal, results in frequency mixing, which can be modeled using the conversion matrix described in Equation (4). Here, R_p represents the parasitic resistance of the variable capacitor, C_0 represents fixed capacitance, V_{LO} denotes LO voltage amplitude, and C′ denotes the slope of the C-V curve. In this work, a C_0 value of 1.2 pF was used.

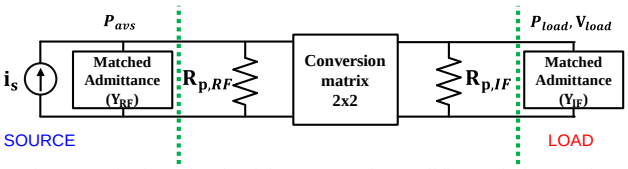


Fig. 4. Equivalent circuit of the parametric amplifier to derive a gain.

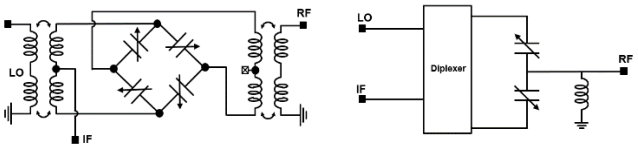


Fig. 5. (a)Conventional double-balanced parametric amp, (b)proposed single-balanced structure parametric amp.

$$C(t) = C_0 + C'V_{LO}cos\omega_{LO}t \quad (3)$$

$$\begin{bmatrix} I_{RF} \\ I_{IF}^* \end{bmatrix} = \begin{bmatrix} j\omega_{RF}C_0 + \frac{1}{R_p} & j\omega_{RF}C_1 \\ -j\omega_{IF}C_1^* & -j\omega_{IF}C_0 + \frac{1}{R_p} \end{bmatrix} \begin{bmatrix} V_{RF} \\ V_{IF}^* \end{bmatrix} \quad (4)$$

R_p: *equivalent parallel resistance*, C_0 = *fixed capacitance*, $C_1 = C'V_{LO}$

Subsequently, when the impedance of the source and load is matched, as illustrated in Fig. 4, the resulting gain (G_{T}) and noise (F) equations are given by Equations (5) and (6), respectively. Here, G_{RF}, G_{IF} represent the conductance of the matching network, Y_{s} denotes source admittance, while Q_{IF} and Q_{RF} denote the quality factors of the matching network. Achieving high gain and low noise requires careful consideration of the conductance seen by the core through the matching network, as well as the amplitude of the voltage swing applied from the external LO source. At lower temperatures, reduced thermal carrier dispersion enhances the sensitivity of the CMOS varactor depletion region to gate voltage, thereby increasing the slope C_1. This increase in C_1 leads, according to Equations (5) and (6), to higher gain and lower noise performance at reduced temperatures.

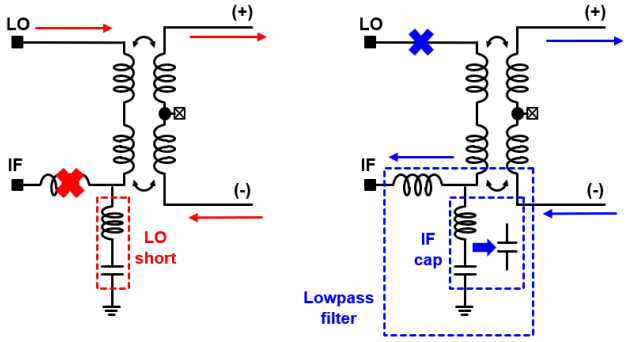
$$G_t = 4\cdot\frac{G_{\mathrm{RF}}}{G_{\mathrm{RF}}+1/R_{p,\mathrm{RF}}}\cdot\frac{G_{\mathrm{IF}}}{G_{\mathrm{IF}}+1/R_{p,\mathrm{IF}}}\cdot\frac{Q_{\mathrm{RF}}Q_{\mathrm{IF}}\left(\frac{C_1}{2C_0}\right)^2}{\left|1-Q_{\mathrm{RF}}Q_{IF}\left(\frac{C_1}{2C_0}\right)^2\right|^2}\cdot\frac{\omega_{\mathrm{IF}}}{\omega_{\mathrm{RF}}} \quad (5)$$

$$F|_{Y_s=Y_{\mathrm{opt}}} = F_{min} = 1 + m\cdot\left(\frac{4}{\omega_{IF}C_1}\cdot\frac{1}{\sqrt{R_{p,RF}R_{p,IF}}}\right) \quad (6)$$

$$Y_{opt}: \frac{\omega_{IF}C_1}{2}\cdot\sqrt{\frac{R_{p,IF}}{R_{p,RF}}} - jw_{RF}C_0$$

B. Varactor core structure

Excluding the effects of impedance matching, the dominant parameter determined by the variable capacitor structure is the parasitic resistance $R_{p,\mathrm{RF}}$, and minimizing this resistance is crucial for optimizing the noise and gain performance of the amplifier. Fig. 5 compares the conventional double-balanced structure with the proposed design. A double-balanced ring core configuration is commonly used to facilitate impedance matching and



(a) (b)

Fig. 6. Diplexer structure of (a) high frequency operation and (b) low frequency operation.

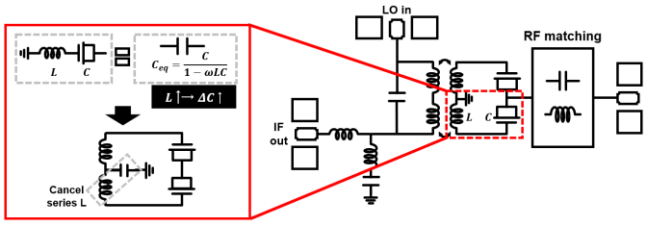


Fig. 7. Effect of a single-ended series inductor of diplexer

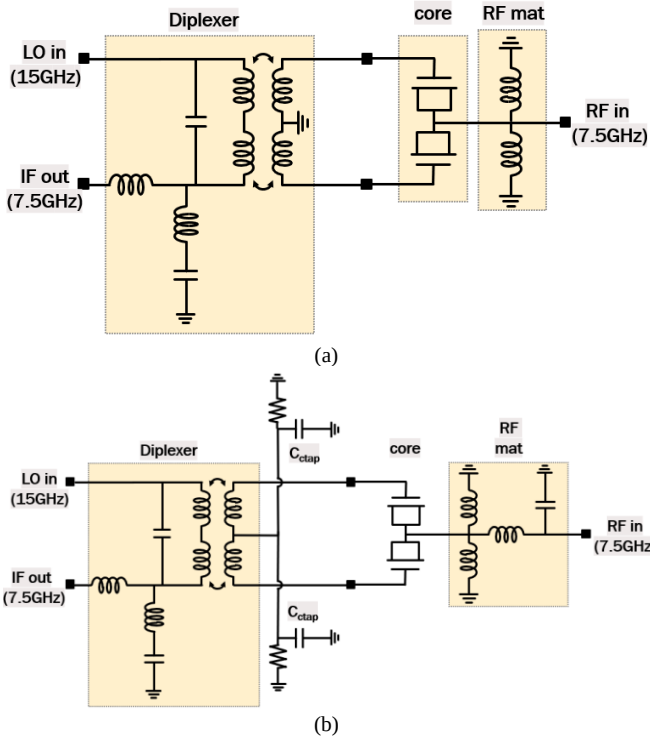


Fig. 8. Schematic of (a) high gain version and (b) low noise version

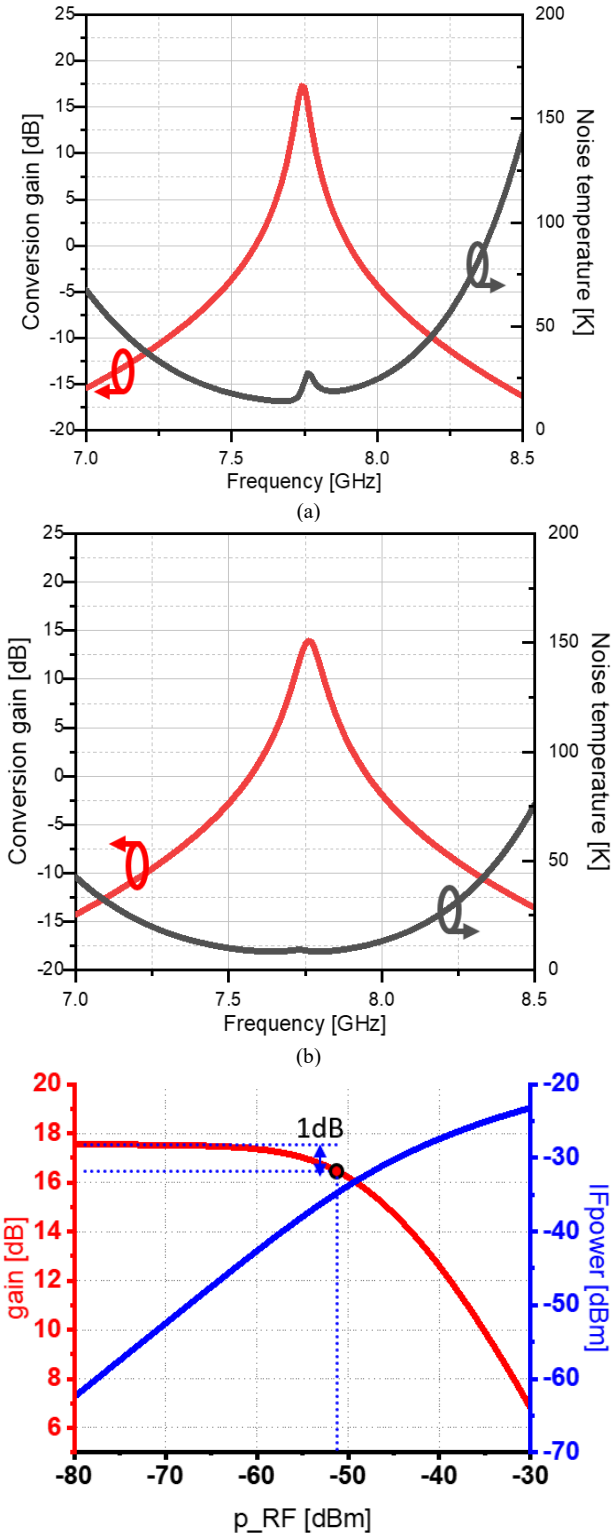


Fig. 9. Simulated conversion gain and noise performance at 4K of (a) high gain version with -10 dBm LO power (b) low noise version with -6 dBm LO power and (c) IP1dB of amplifier.

maintain port isolation. However, when utilizing four identical variable capacitors, the design suffers from increased parasitic resistance and requires a relatively larger chip area. In contrast, by employing a single-balanced structure where two variable capacitors are connected in series, the equivalent parasitic resistance modeled in parallel effectively doubles, while C_0 is reduced by half. This modification leads to improvements in both gain and noise performance.

To maintain isolation between ports, a diplexer was incorporated into the design. A diplexer is a frequency-selective device used to separate signals in different frequency bands [8]. Unlike conventional balanced structures, where isolation is achieved through symmetry, the single-balanced topology requires explicit separation of the

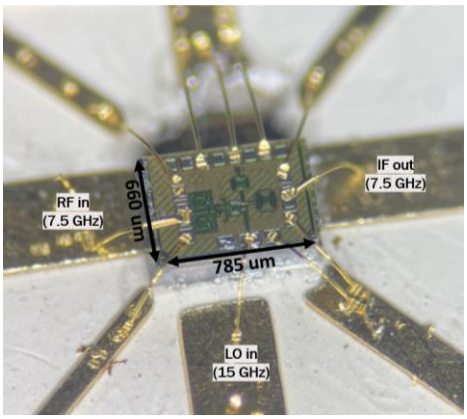


Fig. 10. A photograph of high gain version parametric amplifier

TABLE1. Comparison Table

Published	This work (simulation)		[9] VLSI 2022	[5] SSCL 2020	[10] TMTT 2021	[11] IMS 2024
	Low power matching	Noise matching				
Technology	65-nm CMOS		65-nm CMOS	40-nm CMOS	PCB	130-nm SiGe BiCMOS
Environment temp [K]	4		0.08	8.5	RT	RT
Gain [dB]	17.3	14	17	9	10	14
Noise temp [K]	19.6	8.4	13	100	330	NA
LO power [dBm]	-10	-6	-4.5	NA	27	6.3
Dimension [mm²]	0.52	0.56	0.6	0.23	NA	0.361

IF signal, which is generated by mixing with the high-frequency LO signal. As shown in Fig. 6, a series LC short circuit resonating at the LO frequency is employed to maintain isolation between the LO and IF ports. This configuration ensures that LO power is efficiently delivered to the core while preventing interference between the LO and IF signals. Additionally, since this LC short appears capacitive at lower frequencies, it forms a low-pass filter in conjunction with the series inductor at the IF frequency. This design facilitates the transmission of the reflected IF signal while further filtering the LO signal. For the fundamental matching structure, a second-order doubly tuned transformer matching network was employed [12]. Since the diplexer simultaneously performs both impedance matching and signal separation, it contributes to area efficiency. Moreover, by reducing the number of variable capacitors in the core by half, the proposed design achieves a more compact layout.

C. RF matching structure

The design considerations for the RF matching network primarily involve maximizing C' while minimizing G_{RF}. The variation in C' within the RF matching circuit structure arises from the presence of a series inductor in the diplexer configuration, as illustrated in Fig. 7. Given that the RF matching network is single-ended, the series inductor within the diplexer transformer induces resonance, leading to an increase in the effective capacitance and a more pronounced variation. This characteristic is beneficial for achieving higher gain at lower LO power levels. However, this also results in an expanded unstable region, making the system more susceptible to variations in the matching network, thereby introducing a trade-off between stability and performance.

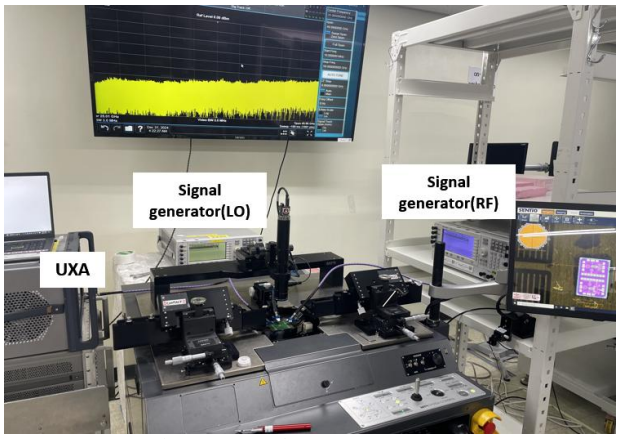


Fig. 11. On-wafer measurement setup

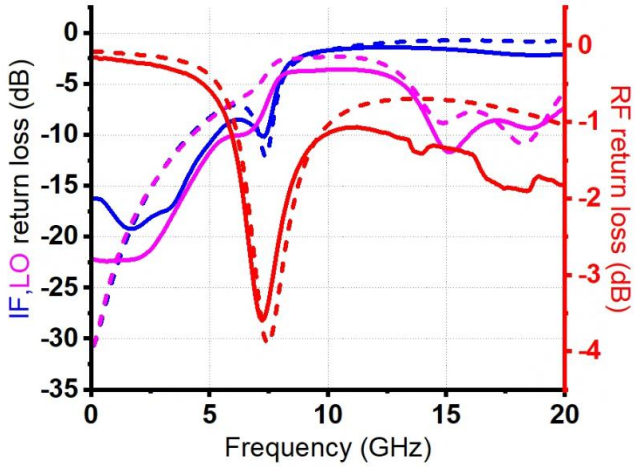


Fig. 12. Measured RF,IF,LO return loss vs frequency at 300K on wafer measurement

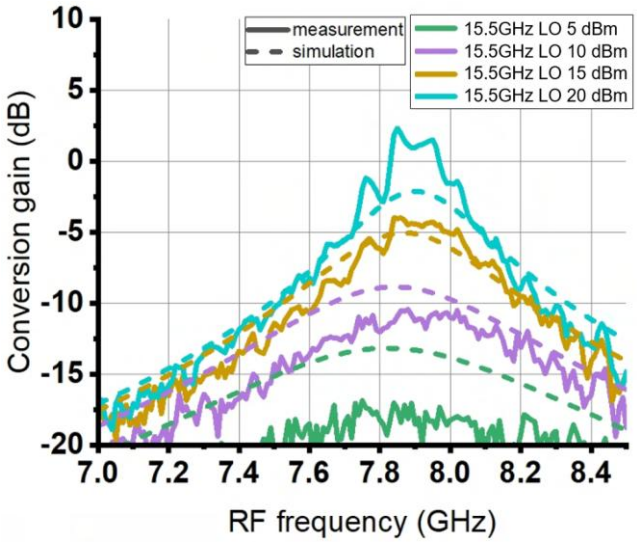
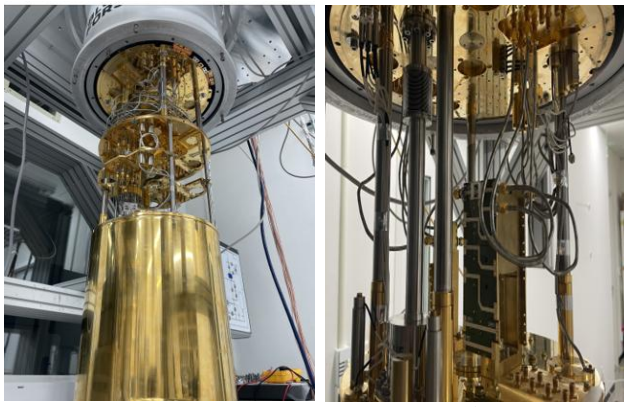


Fig. 13. Measured conversion gain vs RF frequency at 300K on wafer measurement

To mitigate this issue, two distinct design methodologies were implemented. The first approach, tailored for low LO power applications, involved grounding the center tap of the diplexer to preserve the influence of the series inductor and enhance, thereby facilitating higher gain at reduced power levels. The second approach, optimized for low-noise



(a) (b)

Fig. 14. 4K measurement (a) setup, (b) mounted PCB

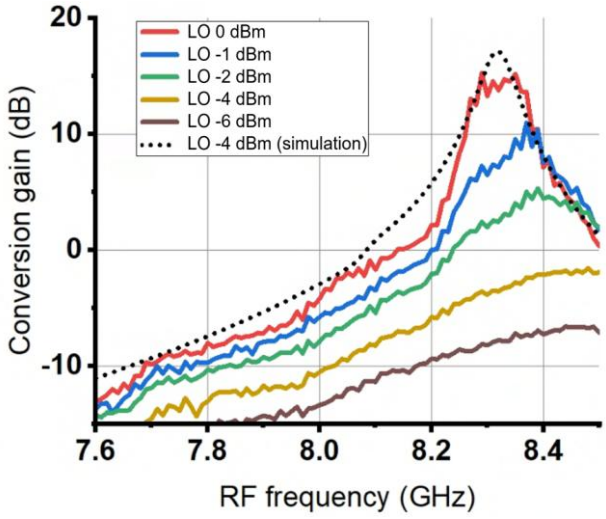


Fig. 15. Measured conversion gain vs RF frequency at 4K PCB measurement

performance, incorporated a series capacitor at the center tap of the diplexer (C_{ctap}). This capacitor resonates with the series inductor, yielding a matching circuit that exhibits reduced sensitivity to variations in both the matching network and LO power, ultimately optimizing the design for minimal noise.

The schematic of the fully designed chip is shown in Fig. 8, and the simulated performance is presented in Fig. 9 and TABLE 1. The low-LO-power version achieved a gain of 17.3 dB with an LO power of −10 dBm, while the corresponding noise temperature was 19.6 K and -51dBm IP1dB. In addition, the low-noise version exhibited a noise temperature of 8.8 K at an LO power of −6 dBm, with a corresponding gain of 14 dB. The low-power-matching version demonstrates a reduction of approximately 6 dB in required LO power relative to previous studies, while maintaining comparable gain and noise performance. Meanwhile, the low-noise-matching version achieves simulated single-digit noise temperature performance. The area efficiency afforded by CMOS implementation is also preserved.

III. MEASUREMENT RESULTS

The parametric amp was fabricated using a 65-nm bulk CMOS process, and Fig. 10 presents the chip photograph (0.66 mm × 0.785 mm). Due to issues related to sawing and wire bonding, chip measurements were conducted only for the high-gain version of the parametric amplifier.

A. On-wafer measurement

As shown in Figure 11, on-wafer measurements were first conducted in a 300K environment. Fig. 12 presents the return loss measured at each RF, IF, and LO port. It was observed that the RF and IF ports, matched at 7.5 GHz, and the LO port, matched at 15 GHz, exhibited measurement results consistent with the simulation.

Next, the measurement results of the conversion gain through amplifier operation are presented in Fig. 13. The conversion gain was determined by measuring the power of the mixed IF frequency using a UXA, with a 7.5 GHz RF signal and a 15.5 GHz LO signal applied via a signal generator. The measurement results demonstrated that the gain increased as the amplitude of the applied LO signal increased, which was consistent with the simulation. Additionally, in the 300K environment, the presence of large parasitic resistance led to a negative conversion gain.

B. 4K PCB measurement

Fig. 14 is the measurement setup in the refrigerator. For the experiment in a 4K environment, a dilution refrigerator from Bluefors was used to mount the PCB and perform cooldown. The measured conversion gain is presented in Fig. 15. When a 16.4GHz LO power of 0 dBm was applied to the chip, a conversion gain of 15.2 dB was obtained. This gain level corresponds to the simulated value when an LO signal of -4 dBm was applied; however, the actual measurement required a stronger LO power. The discrepancy between simulation and measurement is attributed to the uncertainty in 4K environment simulations. As shown in Figs. 12 and 13, the return loss and conversion gain measured at room temperature (300 K) exhibit trends that closely match the simulation results. However, under the 4 K environment, since the data provided in the PDK documentation and EMX simulation process files are only guaranteed for temperatures above -40°C, it is challenging to predict trends of the variation of the varactor C–V characteristics in a 4K environment. Consequently, while debugging with previous measurements allowed the frequency of the gain peak to match, the required input power still exhibited uncertainty. Additionally, this discrepancy may also stem from errors in the LO pattern observed during the process of measuring LO path loss in the dilution refrigerator.

IV. CONCLUSIONS

In this paper, a cryogenic CMOS parametric amplifier was designed for superconducting qubit-based quantum computing. To enhance the scalability of quantum computers, a compact design is required, while achieving high fidelity necessitates high gain and low noise performance. To overcome the limitations of previous research, a single-balanced architecture was adopted to minimize the impact of

parasitic components. Additionally, simultaneous implementation of impedance matching and port isolation enabled a compact design. Furthermore, an appropriate matching structure for the RF port was selected to facilitate the design of a high-gain, low-noise amplifier. The measured gain in a 4K environment exhibited a conversion gain of 15.2 dB when a 0 dBm LO signal at 16.4 GHz was applied. Although this result was obtained with an LO power 4 dBm higher than the simulated value, it was consistent with the frequency response predicted by simulation. Also, reducing core parasitics and selecting a relaxed matching point enabled the improvement of noise performance in the single-digit Kelvin range.

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REFERENCES

[1] Boyn, Jan-Niklas, et al. "Quantum-classical hybrid algorithm for the simulation of all-electron correlation." The Journal of Chemical Physics 155.24 (2021): 244106.

[2] Deutsch, David, et al. "Quantum privacy amplification and the security of quantum cryptography over noisy channels." Physical review letters 77.13 (1996): 2818.

[3] Biamonte, Jacob, et al. "Quantum machine learning." Nature 549.7671 (2017): 195-202.

[4] Ball, Philip. "First 100-QUBIT quantum computer enters crowded race." Nature 599 (2021): 542.

[5] M. Mehrpoo, F. Sebastiano, E. Charbon and M. Babaie, "A Cryogenic CMOS Parametric Amplifier," in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 5-8, 2020

[6] J. M. Manley and H. E. Rowe, "Some General Properties of Nonlinear Elements-Part I. General Energy Relations," in *Proceedings of the IRE*, vol. 44, no. 7, pp. 904-913, July 1956

[7] H. Rowe, "Some general properties of nonlinear elements. II. Small signal theory," Proceedings of the IRE, vol. 46, no. 5, pp. 850-860, 1958.

[8] K. Choi, H. Park, M. Kim, J. Kim and Y. Kwon, "A 6–18-GHz Switchless Reconfigurable Dual-Band Dual-Mode PA MMIC Using Coupled-Line-Based Diplexer," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 12, pp. 5685-5695, Dec. 2018

[9] G. Baek et al., "13-KT noise Cryo-CMOS Parametric Amplifier at 80 mK for Quantum Computers," in 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), 2022: IEEE, pp. 236-237.

[10] M. Hedayati, L. K. Yeung, M. Panahi, X. Zou and Y. E. Wang, "Parametric Downconverter for Mixer-First Receiver Front Ends," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 5, pp. 2712-2721, May 2021

[11] P. Palacios, M. Saeed and R. Negra, "57-GHz Low-Power Subharmonic Parametric Downconverter Exploiting Capacitance Nonlinearity in SiGe BiCMOS," 2024 IEEE/MTT-S International Microwave Symposium - IMS 2024, Washington, DC, USA, 2024, pp. 678-681

[12] A. Mazzanti and A. Bevilacqua, "Second-Order Equivalent Circuits for the Design of Doubly-Tuned Transformer Matching Networks," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 12, pp. 4157-4168, Dec. 2018

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