Design of a High-Gain Amplifier Using Negative-Resistance-Assisted Technique

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Abstract **- This paper proposes an impedance-splitting, negative-resistance-assisted architecture to improve feedback amplifier performance by implementing a negative resistance at the feedback nodes. This technique cancels non-ideal virtual ground (ΔV_{VGND}), thereby increasing the effective loop gain. Simulations show a low-frequency gain increase of 43.6 dB and at least 39.8 dB improvements in both power-supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR).**

Keywords**—high performance amplifier, negative resistance assisted technique, non-ideal virtual ground, loop-gain enhancement technique.**

I. INTRODUCTION

Amplifiers are fundamental building blocks in analog and mixed-signal circuits, including analog-to-digital converters (ADCs) and power management integrated circuits (PMICs). To ensure reliable operation, they must maintain stability under variations in process, supply voltage, and temperature (PVT), and designs that consistently meet these constraints are highly regarded. For precision applications, a high power-supply rejection ratio (PSRR) is required to suppress supply ripple and noise, while a high common-mode rejection ratio (CMRR) is essential to attenuate input common-mode disturbances. In conventional negative-feedback amplifiers, the assumption of an ideal virtual ground is often violated when the loop gain is insufficient.

This non-ideality appears as a non-ideal virtual ground (ΔV_{VGND}), which induces undesired loss currents through the feedback network [1], [2]. Ideally, ΔV_{VGND} remains at zero, resulting in zero loss current. In practice, however, the finite loop gain causes ΔV_{VGND} to induce a loss current through the feedback network. As shown in Fig. 1, currents I_{Loss1} and I_{Loss2} flow through the equivalent resistance of the feedback network at the V_{OUT} node, thereby degrading PSRR and CMRR. Consequently, even well-compensated designs may exhibit reduced immunity to supply and common-mode perturbations in the presence of finite loop gain.

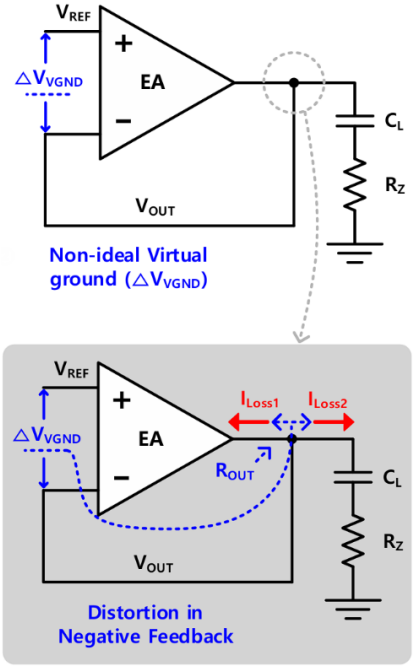

Fig. 1 Effect of ΔV_{VGND} in the negative feedback loop on the conventional amplifier.

Several loop gain enhancement techniques have been reported in the literature [1]-[9]. However, many of these approaches introduce significant power consumption and added design complexity due to elaborate biasing schemes, auxiliary regulation paths, or additional gain stages. Such approaches can be prohibitive in power- and area-constrained systems.

This technique adopts a simple yet effective technique that improves loop gain by combining impedance splitting with a negative-resistance-assisted approach [2]. The method reshapes the impedance at the feedback nodes to reduce virtual-ground distortion and limit loss currents, thereby increasing the effective loop gain without resorting to heavy compensation networks or power-intensive auxiliary blocks. Consequently, loop-gain performance improves markedly, along with PSRR and CMRR.

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II. PROPOSED IMPEDANCE-SPLITTING, NEGATIVE-RESISTANCE-ASSISTED AMPLIFIER TECHNIQUE

Conventional negative-resistance-assisted loop-gain enhancement techniques can largely be classified into two groups [1], [10]. First, a cross-coupled inverter is employed to realize a negative resistance, the magnitude of which is determined by its transconductance (g_m). This approach, however, requires close matching between the NMOS and PMOS g_m values, which is difficult to guarantee across PVT variations. The second technique relies on bipolar source degeneration, where the effective negative resistance is set by the degeneration resistors (R_D), allowing the resistance mismatch to be maintained within a few percent [1]. Nevertheless, the transconductance must exceed $1/R_D$, which dramatically increases the quiescent current. Furthermore, to suppress ΔV_{VGND}, the equivalent resistance at the feedback node (R_{EQ}) must be well matched to the negative resistance ($-1/G_m$), a requirement that is sensitive to PVT.

The proposed impedance-splitting inverter architecture employs a buffer (source follower) and a pair of cross- coupled PMOS transistors, which present an output resistance of $1/g_m$ at the input node of the error amplifier (EA).

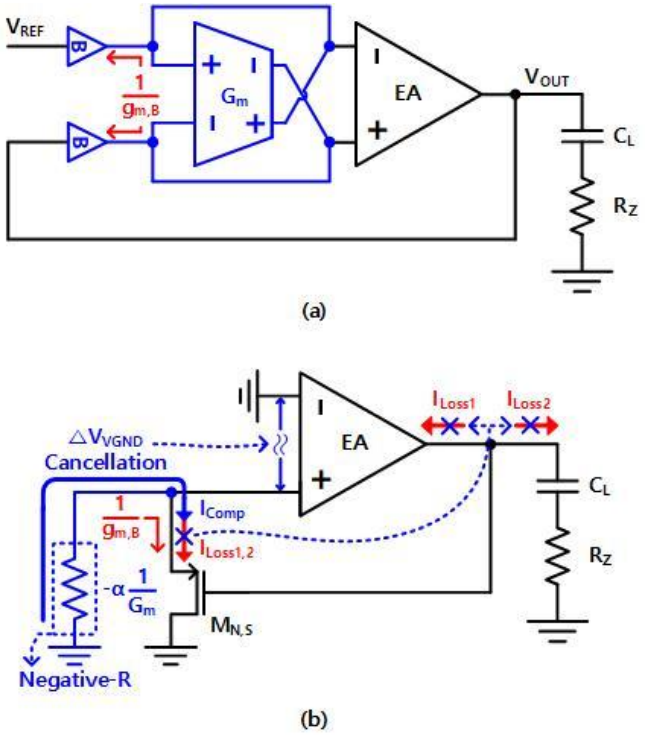


Fig. 2 (a) Conceptual block diagram of the proposed impedance-splitting negative-resistance-assisted amplifier. (b) Low frequency, small-signal model: ΔV_{VGND} cancellation.

In particular, the proposed negative-resistance circuit formed by a cross-coupled, diode-connected PMOS pair provides an equivalent output resistance of $1/g_m$, whereas the source follower presents an equivalent input resistance of approximately $1/g_m$ at the EA input; because both are realized with PMOS devices, these resistances can be closely matched. As a result, the equivalent resistances at the EA input and at the feedback node are decoupled by the buffer, effectively splitting the impedance. This arrangement matches the negative resistance to the equivalent resistance at the EA input, thereby achieving a stable reduction in ΔV_{VGND} even under PVT variations.

As depicted in Fig. 2(a), the method presented in this paper employs a negative-resistance circuit with impedance splitting along the negative-feedback path. By inserting a buffer (source follower) to partition the connection between the feedback nodes and the EA input nodes, the approach integrates the design parameters necessary for canceling ΔV_{VGND}. As shown in Fig. 2(b), when a negative resistance ($-1/G_m$) is applied at the EA input, a compensation current (I_{Comp}) flows through the negative-resistance circuit to compensate for $I_{Loss1,2}$. Consequently, the virtual ground can be maintained near ideal ($\Delta V_{VGND} = 0$), which in turn enhances the loop gain. This mechanism improves the amplifier's overall performance while maintaining robustness under PVT variations.

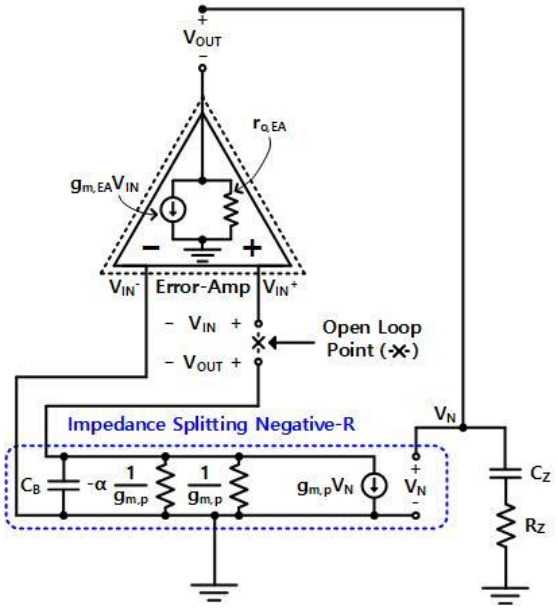


Fig. 3 The small-signal model for the proposed impedance-splitting negative-resistance amplifier with negative feedback.

III. STABILITY ANALYSIS

To analyze stability and loop-gain enhancement, the small-signal model of the proposed negative-resistance amplifier is shown in Fig. 3, where $g_{m,EA}$, and $r_{o,EA}$ denote the EA of transconductance and small-signal output resistance. Where $g_{m,p}$ and C_B denote impedance-splitting- negative-resistance transconductance and lumped output parasitic capacitance. The terms C_Z, R_Z, and α represent the zero-compensation capacitor, the zero-compensation resistor, and the gain-improvement factor provided by the negative-R-assisted circuit, respectively [1], [2], [10]. The transfer function derived from Fig. 3 is open at the inverting input of EA and given by (1) [1].

$$T(s) = \frac{V_{IN}}{V_{OUT}} = \alpha T(0)\frac{(1 + s/z_c)}{(1 + s/p_d)(1 + s/p_{1nd})} \quad (1)$$

As shown in (1), where p_d, p_{1nd}, and z_c denote the dominant pole, the first non-dominant pole, and the compensation zero, respectively, these two poles and one compensation zero are explicitly demonstrated in (2).

$$z_C = \frac{1}{C_Z R_Z r_{o,EA}} \quad p_d = \frac{1}{C_Z(R_Z + r_{o,EA})}$$
$$p_{1nd} = \frac{1}{C_B(1/g_{m,p} || - 1/\alpha g_{m,p})} \quad (2)$$

The dominant pole, p_d, is located at the V_{OUT} node due to the large $r_{o,EA}$ and the zero-compensation capacitor C_Z. Furthermore, the first non-dominant pole, p_{1nd}, is due to the gain-improvement factor α, because the equivalent resistance at the impedance-splitting node increases due to the parallel combination of the negative resistance and the buffer ($-Gm \parallel g_{m,B}$). Consequently, p_{1nd} is shifted to low frequencies and requires compensation. A series connection of C_Z and R_Z is employed to place a compensation zero (z_c) for p_{1nd}. Meanwhile, additional poles lie beyond the bandwidth because their locations are set by the small parasitic capacitances.

Equation (1) presents the enhanced DC open-loop gain αT(0), where αT(0) equals the EA gain multiplied by the loop gain T(0) and the gain-improvement factor α. The αT(0) derived from Fig. 3 can be obtained as shown in (3).

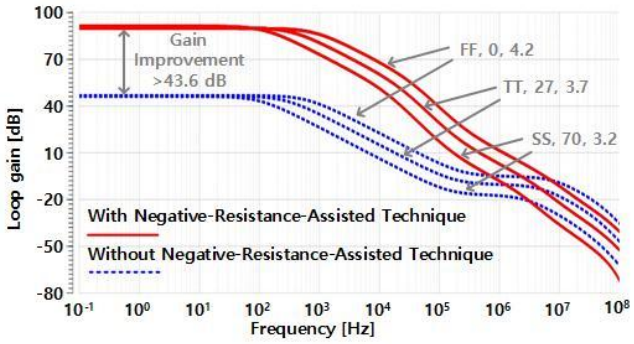
$$\alpha T(0) = -\alpha g_{m,EA} r_{o,EA} \quad (3)$$

As a result, the amplifier's overall loop-gain transfer function is defined in (4), and its three poles and two zeros are listed in (2).

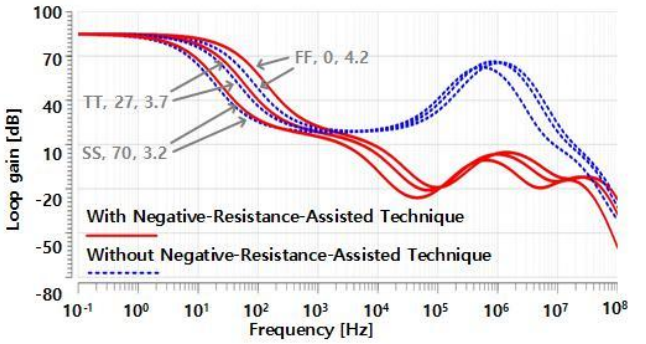
To analyze loop stability, T(s), an open-loop AC analysis was performed by opening the loop between the output stage and the inverting input of the negative-feedback amplifier.

$$T(s) = \frac{V_{IN}}{V_{OUT}} = \frac{-\alpha g_{m,EA} r_{o,EA}(1 + sC_Z R_Z r_{o,EA})}{(1 + sC_Z(R_Z + r_{o,EA}))(1 + sC_B(1/g_{m,p} || - 1/\alpha g_{m,p}))} \quad (4)$$

Fig. 4 (a) and (b) present post-layout AC simulation results demonstrating the stability of the amplifier, showing the loop-gain and phase responses of T(s) under PVT variations and comparing the phase and loop-gain responses of the negative-resistance-assisted and conventional amplifiers as functions of frequency across PVT variations.



(a)



(b)

Fig. 4 Comparison of simulated AC post-layout results between the conventional and proposed negative-resistance-assisted amplifiers: (a) loop gain and (b) phase margin versus frequency across process corners, supply voltages, and temperatures.

The phase margins for the cases (FF, 0°C, 4.2 V), (TT, 27°C, 3.7 V), and (SS, 70°C, 3.2 V) were 69.0°, 70.2°, and 60.0°, respectively. The worst-case phase margin was 60.0°, demonstrating the robust stability of the negative-resistance-assisted amplifier; this meets the commercial temperature range (0–70°C). In addition, αT(0) can be derived as given in (5) [1], [2], [10].

$$\alpha = \frac{K}{K - 1} \quad (5)$$

The impedance-splitting, negative-resistance–assisted technique enhances the loop gain, denoted by α in Fig. 2(b). The factor α is determined by the transconductance matching between $g_{m,B}$ and G_m, as defined in (5) [1], [2], [10]. Let $K = g_{m,B}/G_m$ denote the matching coefficient; under perfect matching (K = 1), the loop gain becomes infinite. In this design, the DC gain-improvement factor is K = 1.00665. The matching between $g_{m,B}$ and G_m is defined as shown in (5) [1], [2], [10]. Moreover, as illustrated in Fig. 4(a), the proposed negative-R circuit achieves a gain increase of 43.6 dB at low frequency under PVT variations.

I V. SIMULATION RESULTS

In this paper, the impedance-splitting negative-resistance-assisted technique is employed to enhance the amplifier's PSRR and CMRR. For performance comparison, simulation results for the conventional amplifier and the impedance-splitting negative-resistance-assisted amplifier are presented in Figs. 5 and 6.

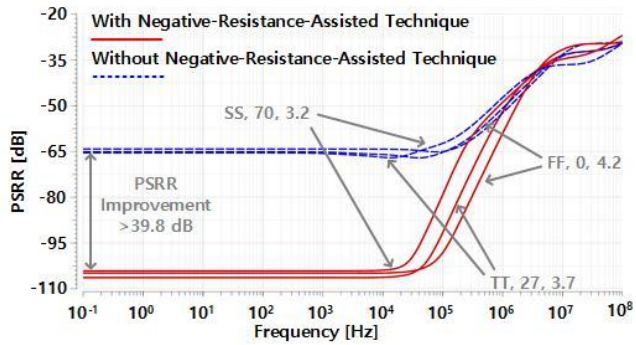


Fig. 5 Comparison of simulated post-layout PSRR results between the conventional and proposed negative-resistance-assisted amplifiers: PSRR versus frequency across process corners, supply voltages, and temperatures.

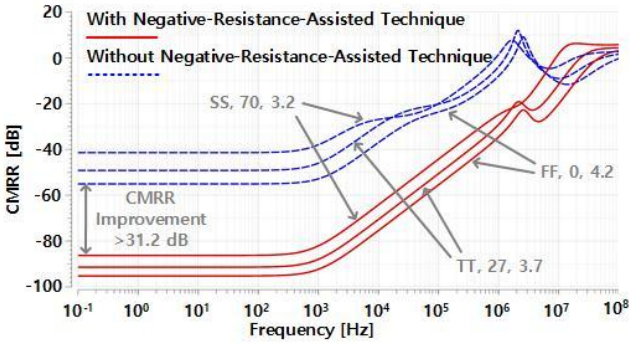


Fig. 6 Comparison of simulated post-layout CMRR results between the conventional and proposed negative-resistance-assisted amplifiers: CMRR versus frequency across process corners, supply voltages, and temperatures.

Fig. 5 presents post-layout PSRR simulation results, showing the amplifier's PSRR under PVT variations and comparing the PSRR of the impedance-splitting negative-resistance-assisted amplifier with that of the conventional architecture as functions of frequency across PVT variations.

The minimum PSRR improvement for the cases (FF, 0°C, 4.2 V), (TT, 27°C, 3.7 V), and (SS, 70°C, 3.2 V) was 39.8 dB, demonstrating the robust PSRR improvement of the impedance-splitting negative-resistance-assisted amplifier.

Fig. 6 presents post-layout CMRR simulation results, showing the amplifier's CMRR under PVT variations and comparing the CMRR of the impedance-splitting negative-resistance-assisted amplifier with that of the conventional architecture as functions of frequency across PVT variations.

The minimum CMRR improvement for the cases (FF, 0°C, 4.2 V), (TT, 27°C, 3.7 V), and (SS, 70°C, 3.2 V) was 39.8 dB, demonstrating the robust CMRR improvement of the impedance-splitting negative-resistance-assisted amplifier.

As shown in Fig. 8, the Monte Carlo simulation results for the loop gain of the conventional and proposed amplifiers show means (μ) of 46.6 dB and 90.19 dB, with standard deviations (σ) of 1.02 dB and 1.06 dB, respectively. Comparing the mean values in Fig. 8, a DC gain improvement factor of K = 1.0067 is achieved.

The detailed transistor-level implementation of the proposed impedance-splitting negative-resistance-assisted amplifier is shown in Fig. 7.

TABLE I. Post-Layout Simulation Results

Performance	Quantity
Input Voltage [V]	3.2 ~ 4.2
Output Voltage [V]	0.6
PSRR. [dB]	-104 ~ -106
CMRR [dB]	-86 ~ -95
Quiescent Current. [μA]	5.3 ~ 26.0

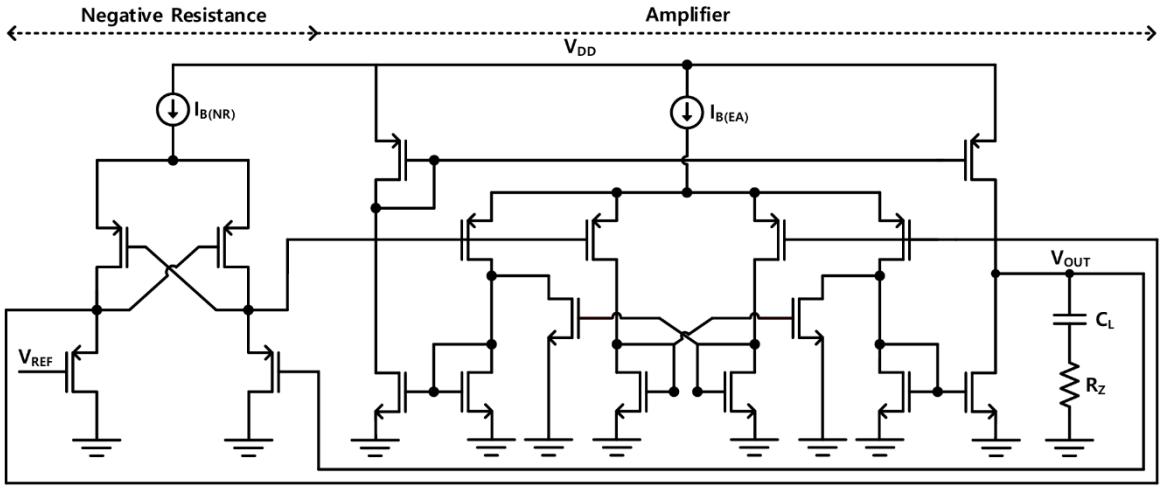
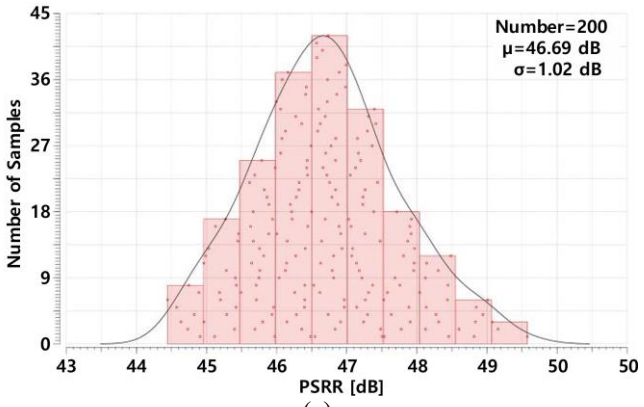
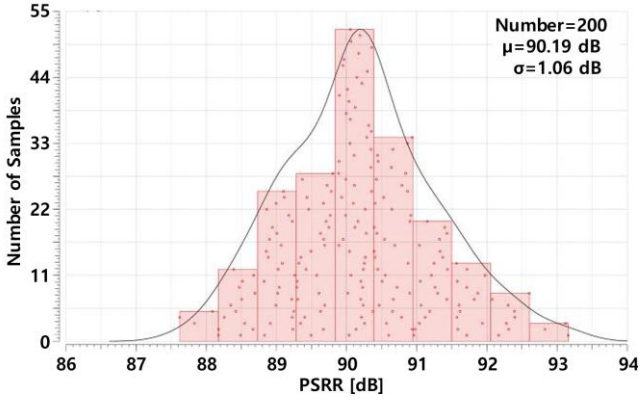


Fig. 7 Transistor-level circuit implementation of the proposed negative-resistance-assisted amplifier



(a)



(b)

Fig. 8. Simulated Monte Carlo distributions of the loop gain: (a) conventional amplifier and (b) proposed negative-resistance-assisted amplifier.

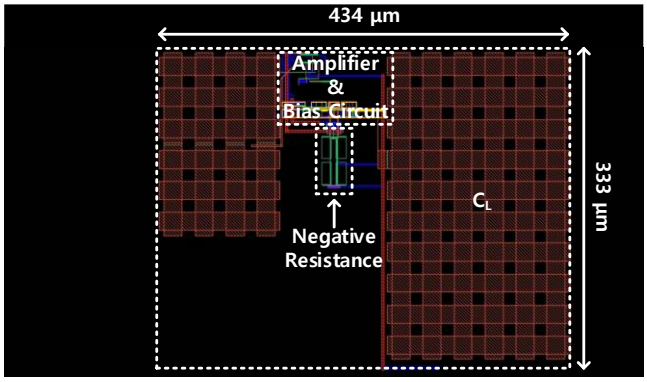


Fig. 9 Layout of the proposed amplifier.

The proposed amplifier is classified into two blocks: an impedance-splitting negative resistance block and a high-gain class-AB amplifier [11]. The impedance-splitting negative-resistance configuration consists of PMOS transistors for $1/g_m$ matching to effectively increase the loop gain.

V. CONCLUSION

In this paper, an impedance-splitting negative-resistance-assisted technique was introduced to mitigate the non-ideal virtual ground of an amplifier. The effectiveness of this technique was validated by simulations: the proposed amplifier achieved an improvement in PSRR of 39.8 dB and in CMRR of 31.2 dB. These simulation results, together with the high PSRR and CMRR summarized in Table I and shown in Figs. 5 and 6, confirm that the proposed impedance-splitting negative-resistance -assisted amplifier effectively mitigates the non-ideal virtual ground issue while providing robust noise suppression. As shown in Fig. 9, the proposed amplifier is designed using a 0.18-μm CMOS process, with a total active area of 144,522 μm^2.

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