Fast-Response Low-Voltage NMOS Low-Dropout Regulator Using Coarse and Fine Charge Pumps with Double Driving and High-Frequency Internal Oscillator

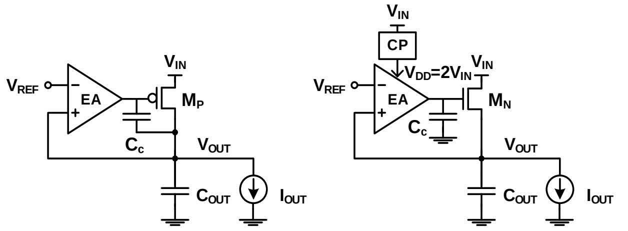
Yunsu Kim[1], Minwoo Kim, Hyuntak Jeon and Byungdo Yang[a]
School of Semiconductor Engineering, Chungbuk National University
E-mail : [1]yst7706@naver.com

***Abstract* – A fast-response low-voltage NMOS low-dropout regulator (LDO) with coarse-fine charge pumps and a double driving-high frequency internal oscillator is proposed. It regulates the gate voltage of the power transistor through coarse and fine charge pumps with three comparators for detecting coarse-fine modes. It achieves fast response time and low quiescent power loss. It has a low undershoot voltage with a fast settling time, employing a high-speed internal ring oscillator driving the coarse and fine charge pumps. The LDO circuit is implemented with a 65 nm CMOS process. It generates 0.45 V output voltage from 0.5 V supply voltage. It has the simulation results of an overshoot of 34 mV, an undershoot of 69 mV, and a settling time of 28 ns under the load transient from 15 mA to 45 mA with a 1 ns edge.**

***Keywords*—Charge-pump circuit, coarse-fine, low dropout regulator (LDO)**

I. INTRODUCTION

Recently, as the circuits with multiple supply voltages have been increasingly integrated into a single semiconductor chip, various on-chip voltage domains are generated to improve overall power efficiency. The conventional analog PMOS low-dropout regulator (LDO) shown in Fig. 1(a) is widely used. However, it suffers from large overshoot and undershoot voltages as well as a slow transient response because the error amplifier operates very slowly at a low supply voltage (V_{IN}). The conventional analog NMOS LDO in Fig. 1(b) reduces the overshoot and undershoot voltages by increasing the supply voltage of the error amplifier (V_{DD}) with a charge pump (CP) to two times the supply voltage ($2V_{IN}$). But, since the NMOS power transistor (M_N) requires a higher gate voltage than V_{IN}, the CP must remain active continuously, resulting in significant power consumption. The charge-pump-based NMOS LDO (CP-LDO) shown in Fig. 2 replaces the amplifier in Fig. 1(b) with a comparator and a coarse-fine up-down charge pump. It needs only dynamic power consumption. It greatly reduces power consumption by eliminating the static bias current in the amplifier. The coarse-fine charge pump improves the load transient response time of the CP-LDO by using coarse and fine charge-pumps with large and small gate driving capacitors when high and low load current transitions occur, respectively [1]. However, the CP-LDO still suffers from slow response because it uses an external clock with a relatively low clock frequency, and the charge pump operates only once per clock cycle.



(a) (b)

Fig. 1. Conventional analog LDOs using (a) PMOS (b) NMOS.

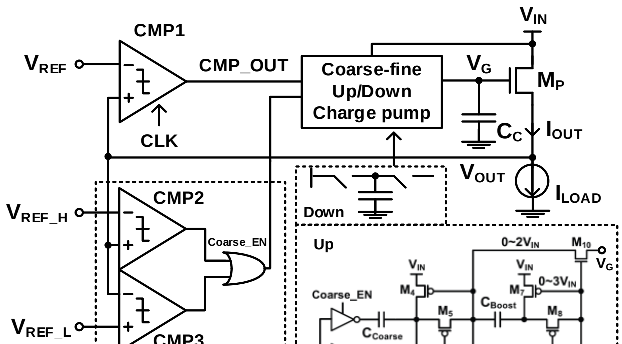


Fig. 2. Conventional CP-LDO [1].

To support operation in low-voltage conditions, the digital low-dropout regulators (D-LDOs) have been widely explored as alternatives to analog LDOs, offering both higher power efficiency and faster transient response [2], [3], [4]. A typical PMOS-based D-LDO is composed of a comparator, a bidirectional shift register, and an array of PMOS switches. In this scheme, the comparator monitors the difference between the output voltage (V_{OUT}) and the

---

a. Corresponding author; bdyang@cbnu.ac.kr

Manuscript Received Oct. 14, 2025, Revised Dec. 30, 2025, Accepted Jan. 11, 2026

reference voltage (V_{REF}). Based on the comparison, the shift register turns individual PMOS transistors on or off at each clock cycle, thereby adjusting the output voltage. However, the D-LDO needs large dynamic power consumption in the larger-bit bidirectional shift register. The dynamic power consumption significantly increases as the higher frequency clock is used to improve the faster transient response. Therefore, the clock frequency is limited.

In this paper, a fast-response low-voltage NMOS low-dropout regulator with coarse and fine charge pumps is proposed. It regulates the gate voltage of the power transistor with coarse-fine charge pumps and a double driving-high frequency internal oscillator is proposed. It achieves fast response time and low quiescent power loss. It has a low undershoot voltage with a fast settling time, employing a high-speed internal ring oscillator driving the coarse and fine charge pumps.

II. ARCHITECTURE

A. Proposed Coarse-Fine Charge-Pump Circuit

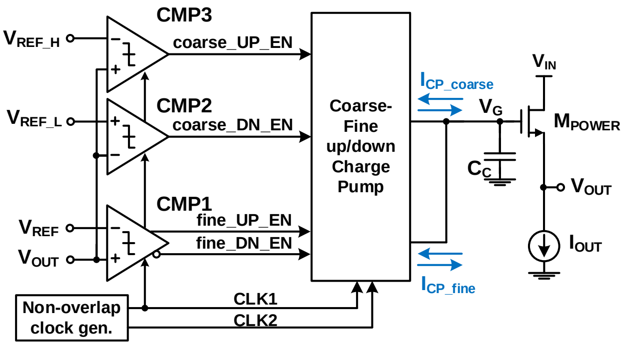


Fig. 3. Proposed charge-pump low-dropout regulator (CP-LDO).

Fig. 3 shows the proposed charge-pump low-dropout regulator (CP-LDO). The proposed CP-LDO extends the conventional CP-NMOS LDO [1] by integrating a high-speed internal ring oscillator that provides a significantly higher clock frequency and a cross-coupled charge-pump architecture that enhances the transient charging and discharging capability of the gate node. With these improvements, the proposed LDO achieves a faster response during load transients while maintaining low quiescent power consumption. Nevertheless, the overall regulation mechanism remains consistent with the previously reported CP-NMOS LDO in [1], ensuring compatibility with existing coarse–fine operation schemes. As shown in Fig. 3, three comparators continuously sense the output voltage (V_{OUT}) relative to the reference levels (V_{REF}, V_{REF_H}, and V_{REF_L}). The comparators generate mode-selection signals that determine whether the regulator should operate in coarse or fine mode. Specifically, when V_{OUT} exceeds V_{REF_H} due to the overshoot or falls below V_{REF_L} during the undershoot, the regulator transitions into the coarse mode, where the coarse-fine up/down charge pump in Fig. 3 supplies large charge steps to correct the deviation rapidly. Conversely, when V_{OUT} remains within the reference window between V_{REF_H} and V_{REF_L}, the regulator reverts to fine mode, where the charge pump supplies smaller voltage steps to ensure stable and precise regulation.

The charge pump adjusts the gate voltage (V_G) within the range of 0 to $2V_{IN}$. Thereby it controls the conduction of the NMOS power transistor and stabilizes V_{OUT} at the target value of V_{REF}. To further suppress unwanted fluctuations, a compensation capacitor (C_C) is connected at the gate node. This capacitor prevents V_G from being disturbed by abrupt V_{OUT} transitions coupled through the intrinsic gate capacitance (C_{GS}). This maintains the stable regulation during fast load current changes.

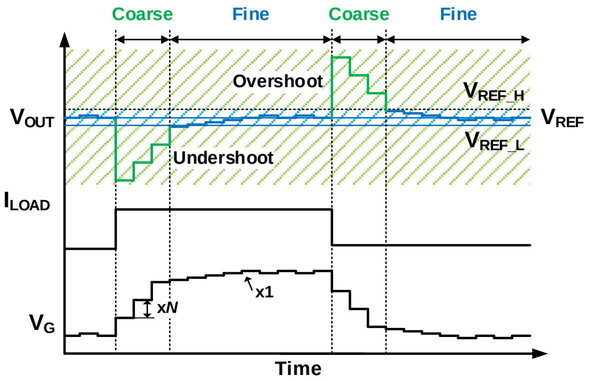


Fig. 4. Transient waveforms of the proposed CP-LDO.

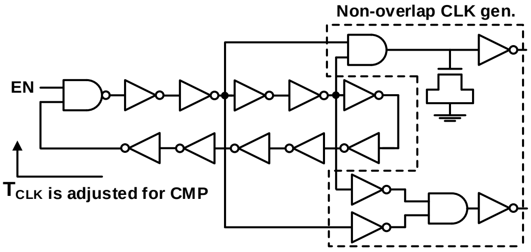
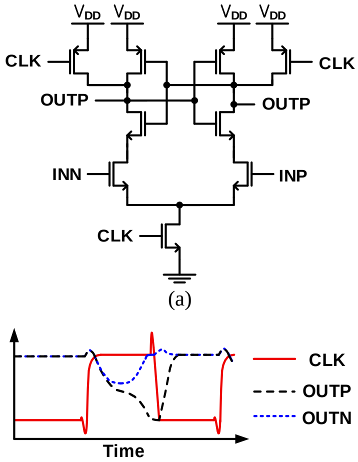


Fig. 5. Ring oscillator for non-overlap clocks



(a)

(b)

Fig. 6. (a) Circuit schematic and (b) transient waveform of the conventional dynamic comparator.

The ring oscillator in Fig. 5 is designed as an inverter-based structure to generate fast and robust non-overlap clocks. Its frequency is optimized to match the maximum operating speed required by the comparators in Fig. 6. By aligning the oscillator speed with comparator requirements, the proposed regulator avoids unnecessary delays and achieves faster dynamic operation compared to designs relying on an external clock source. Moreover, the integration of the non-overlap clock generator guarantees that the up and down charge-pump switches do not turn on simultaneously, which prevents short-circuit current and enhances power efficiency.

Figs. 7 and 8 show the coarse-fine up and down charge pumps, respectively. The upcharge pump in Fig. 7 adopts two cross-coupled charge pumps, so that the times larger charge from the twin capacitors are transferred per cycle. As a result, it boosts the gate voltage close to $2V_{IN}$ with faster and more efficient charge delivery. The down charge pump in Fig. 8 employs the conventional flying-capacitor switching scheme, where one terminal of the capacitor is alternately connected to GND and V_G. This structure is retained for simplicity and robustness while still providing reliable gate voltage reduction when needed. Furthermore, in the coarse mode, the sizes of the capacitance and transistor in the charge-pump circuits are scaled up for the fast charge and discharge of V_G. This sizing strategy significantly enhances transient performance, enabling the regulator to quickly suppress sudden overshoot or undershoot events and restore V_{OUT} to its nominal reference level.

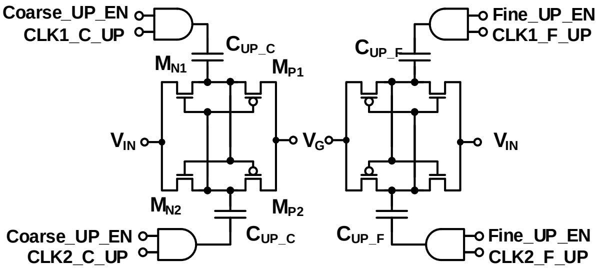


Fig. 7. Coarse-fine upcharge pump

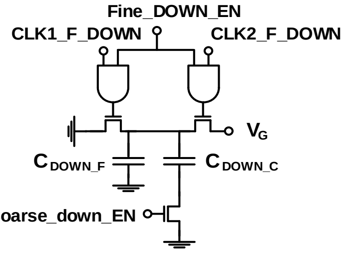


Fig. 8. Coarse-fine down charge pump

Ⅲ. SIMULATION RESULTS

The proposed CP-LDO was implemented in a 65 nm CMOS process. Fig. 9 shows the chip layout of the prototype. The active core area is 12 μm^2 including the on-chip capacitor. The power transistor area is 7.9 μm^2. The total integrated capacitance is 7.5 pF, where two coarse-up capacitors ($2\times C_{UP\_C}$) are 5 pF, two fine-up capacitors ($2\times C_{UP\_F}$) are 0.4 pF, a coarse-down capacitor (C_{DOWN_C}) is 0.5 pF, a fine-up capacitor (C_{UP_F}) is 0.1 pF, and a compensation capacitor (C_C) is 0.5 pF. Also, the proposed CP-LDO is a capless-type LDO circuit without any output capacitor (C_{OUT}). However, the PADs and PCB circuit have the parasitic capacitances, which are modeled in the output capacitor (C_{OUT}) of 1 pF for the simulation.

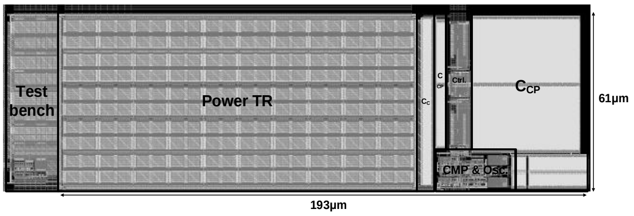


Fig. 9. Chip layout

Fig. 10 shows the simulation environment for the proposed regulator in both transient response and steady-state operation. Fig. 11 shows the simulation transient response when the load current (I_{LOAD}) changes from 15 mA to 45 mA with the edge times of 1 ns at V_{IN} = 0.5 V and V_{OUT} = 0.45 V. When I_{LOAD} changes, the proposed CP-LDO has the undershoot voltage of 69 mV with a settling time of 28 ns. Fig. 12 shows the simulation transient response when I_{LOAD} changes from 25 mA to 100 mA with the edge times of 1ns at V_{IN} = 0.6 V and V_{OUT} = 0.55 V. When I_{LOAD} changes, the proposed CP-LDO has the undershoot voltage of 94 mV with a settling time of 11 ns. Fig. 13 presents the simulated load regulation characteristics with the fixed dropout voltage of 50 mV when the supply voltage (V_{IN}) is 1.0 V, 0.8 V, and 0.5 V. The output voltage (V_{OUT}) remains stable across the full load current range, confirming the regulation capability of the proposed architecture. Fig. 14 shows the current efficiency characteristics versus load current under the same test conditions. The current efficiency is maintained close to the theoretical maximum value, and the peak efficiency reaches 99.96 %, because the quiescent current overhead is negligible. Fig. 14 illustrates the line regulation with the dropout voltage of 50 mV. The output voltage tracks the variation of the input supply while maintaining accurate regulation. These simulation results confirm that the proposed CP-LDO achieves both stable regulation and high current efficiency across a wide operating range.

Table I summarizes the performance comparison of the proposed CP-LDO with recently reported designs. The proposed regulator achieves the fastest transient response, showing a 28 ns settling time at V_{IN} = 0.5 V. The settling time is much shorter than the microsecond-level values reported in the conventional CP-LDO [5] and CFCP-LDO [1]. These results show the effectiveness of the proposed architecture for fast load regulation under low-voltage operation.

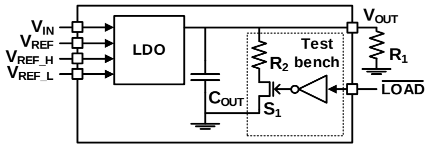


Fig. 10. Simulation setup

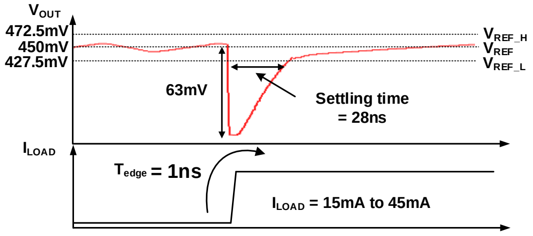


Fig. 11. Simulated transient response when I_{LOAD} changes from 15 mA to 45 mA at VIN = 0.5 V, VOUT = 0.45 V

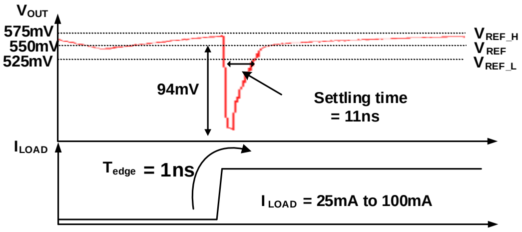


Fig. 12. Simulated transient response when I_{LOAD} changes from 25 mA to 100 mA at VIN = 0.6 V, VOUT = 0.55 V

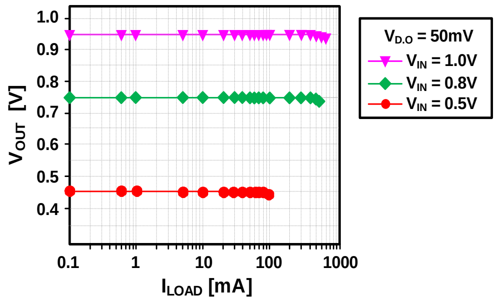


Fig. 13. Simulated load regulation

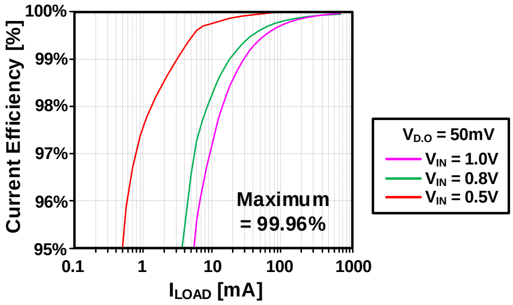


Fig. 14. Simulated current efficiency

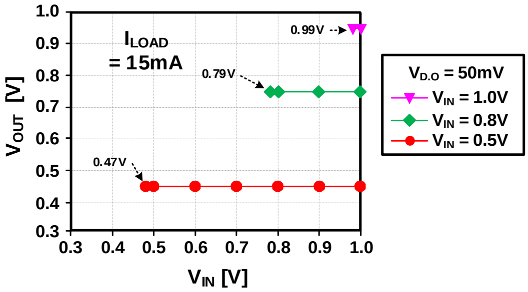


Fig. 15. Simulated current efficiency

TABLE I. Comparison with State-of-the-Art Charge Pump Based LDOs

	This Work		TCAS-2 2021 [5]	TCAS-2 2020 [1]
Technology [nm]	65		65	65
Type	CP-LDO		CP-LDO	CFCP-LDO
Area [mm^2]	0.012		0.045	0.01
V_{IN} [V]	0.4-1		0.6-1.2	0.35-0.55
V_{OUT} [V]	0.35-0.95		0.5-1.15	0.3-0.5
$I_{OUT.MAX}$ [mA]	600		60	N.R.
I_Q [uA]	4.5-627		0.1-10	0.16
Peak current efficiency [%]	99.96		99.99	99.99
C_{Total} [pF]	7.5		10	7.6
ΔV_{OUT} [mV] @ ΔI_{LOAD}, V_{IN}	63 @ 30mA, 0.5V	94 @ 75mA, 0.6V	158 @ 28mA, 0.5V	108 @ 10mA, 0.5V
Edge time [ns]	1	1	1	1
T_{settle} [ns]	**28**	**11**	**9600**	**4000**

IV. CONCLUSION

A fast-response low-voltage NMOS low-dropout regulator (LDO) with coarse-fine charge pumps and a double driving-high frequency internal oscillator is proposed. It regulates the gate voltage of the power transistor through coarse and fine charge pumps with three comparators for detecting coarse-fine modes. It achieves fast response time and low quiescent power loss. It has a low undershoot voltage with a fast settling time, employing a 330 MHz high-speed internal ring oscillator driving the coarse and fine charge pumps. The LDO circuit is implemented with a 65 nm CMOS process. It generates 0.45 V output voltage from 0.5 V supply voltage. It has the simulation results of an overshoot of 34 mV, an undershoot of 63 mV, and a settling time of 28 ns under the load transient from 15 mA to 45 mA with a 1 ns edge. It achieves significantly shorter recovery time. It provides both low-voltage operation and fast transient performance. It is suitable for low-power and fine-grained power management applications.

ACKNOWLEDGMENT

The chip fabrication and EDA tools were supported by the IC Design Education Center (IDEC), Korea. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. NRF-2023R1A2C1004954).

REFERENCES

[1] K. C. Woo and B. D. Yang, *A 0.35 V 90nA quiescent current output capacitor-less NMOS low-dropout regulator using a coarse-fine charge-pump circuit, IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 3118–3122, Dec. 2020.

[2] M. Huang, Y. Lu, U. Seng-Pan, and R. P. Martins, *An analog-assisted tri-loop digital low-dropout regulator, IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 20–34, Jan. 2018.

[3] D. Kim and M. Seok, *A fully integrated digital low-dropout regulator based on event-driven explicit time-coding architecture, IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3071–3080, Nov. 2017.

[4] Y.-J. Lee *et al.*, *A 200mA digital low-drop-out regulator with coarse-fine dual loop in mobile application processors, IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, Jan. 2017.

[5] K. Shin, D. W. Jee, and D. Jeon, *A 65 nm 0.6-1.2 V low-dropout regulator using voltage-difference-to-time converter with direct output feedback, IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol 68, no. 1, pp. 67–71, Jan. 2021.

Yun-Su Kim received the B.S. degree in electronic engineering from Chungbuk National University, Cheongju, South Korea, in 2024, where he is currently pursuing the M.S. degree in semiconductor engineering.

Min-Woo Kim received the B.S. and M.S. degree in Electronics Engineering from Chungbuk National University, Rep. of Korea, in 2023 and 2025, respectively. where he is currently pursuing the Ph.D. degree in Semiconductor of Chungbuk National University, Rep. of Korea. His research interests include analog circuits, display driver ICs.

Hyun-Tak Jeon received the B.S. degree in electronic and electrical engineering from Hongik University, Seoul, South Korea, in 2015, and the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2017 and 2021, respectively. He was a Senior Researcher with the Agency for Defense Development (ADD), Daejeon, from 2021 to 2022. He was an Assistant Professor with the School of Electrical and Electronic Engineering, Chungbuk National University (CBNU), Cheongju, South Korea, from 2022 to 2023. He is currently an Assistant Professor with the School of Semiconductor Engineering, CBNU. His research interests include mixed-signal circuit design for sensor interface IC and electrical system design for guided ballistic missile systems.

Byung-Do Yang received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea, in 1999, 2001, and 2005, respectively.

He was a senior engineer at the Memory Division, Samsung Electronics, Kyungki- Do, Republic of Korea, in 2005, where he was involved in the design of DRAM. In 2006, he joined the School of Semiconductor Engineering, Chungbuk National University, Republic of Korea, where he is currently a Full Professor. His research interests are analog circuit, digital circuit, memory circuit, and power IC designs.