Comparison of 3T2C Embedded DRAM in 28nm FD-SOI and Low Power Plus for Energy-Efficient Computing in Memory Architecture

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***Abstract* - This paper presents a comparative analysis of a 3T 2C Embedded DRAM (eDRAM) bitcell fabricated in 28-nm LPP and FD-SOI processes for energy-efficient Computing-in-Memory (CIM) applications. eDRAM provides dense charge domain storage that is directly exploited for compact analog Multiply-And-Computation (MAC) operation in CIM arrays. The proposed cell employs a metal-oxide-metal (MOM) capacitor to achieve high capacitance density without additional process steps. Post-layout simulations and Monte Carlo analyses were conducted to evaluate the effects of the process and temperature variations and capacitive coupling on data retention and analog compute accuracy. Results show that the FD-SOI process provides enhanced retention characteristics and larger voltage margins owing to stronger capacitive coupling and reduced substrate leakage enabled by the buried oxide (BOX) layer.**

***Keywords*— Coupling Effect, Computing-in-Memory, Embedded DRAM, FD-SOI, MOM Capacitor**

I. INTRODUCTION

Conventional computing systems face the memory wall problem, where the cost of data movement between memory and processor dominates both performance and energy consumption. Computing-in-Memory (CIM) has emerged as a promising paradigm to address this issue by enabling computation near or within the memory array [1]-[3].

In CIM architectures, the memory bitcell is commonly based on Static RAM (SRAM) or Dynamic RAM (DRAM), each offering specific trade-offs in area, power, and performance. SRAM provides fast access and stable operation without refresh, but the multi-transistor structure of SRAM cells induces significant area cost and increased static power consumption. In contrast, DRAM stores data in a capacitor-based cell, which significantly reduces the cell area and enables much higher integration density. As a result, DRAM offers better scalability for large memory arrays and low power consumption compared to SRAM. Nevertheless, the volatile nature of DRAM makes it susceptible to leakage currents, causing the stored charge to dissipate over time.

As a result, DRAM requires frequent refresh operations to sustain adequate retention time, which limits its efficiency in low-power applications.

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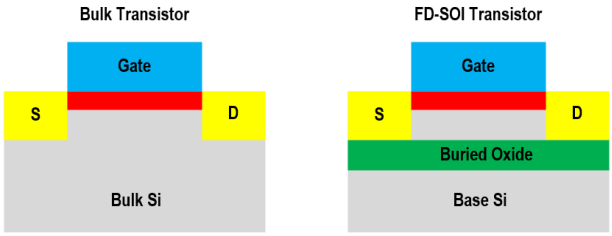


Fig. 1. Structure of Bulk Transistor and FD-SOI Transistor.

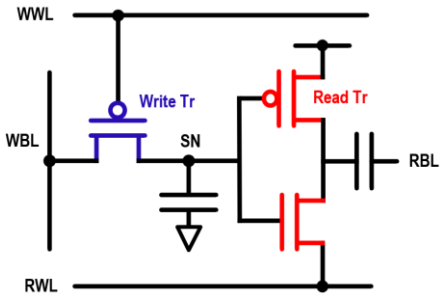


Fig. 2. Schematic of 3-Transistors and 2-Capacitor eDRAM.

The storage node is implemented with a Metal-Oxide-Metal (MOM) capacitor, which necessitates frequent refresh operations to preserve data integrity. This refresh overhead limits its efficiency in low-power applications. To mitigate the refresh overhead and improve the retention characteristics of DRAM-based cells, process-level solutions are essential. Fig. 1 shows bulk and FD-SOI transistor structures. The buried oxide (BOX) layer suppresses junction leakage by physically isolating the channel from the substrate, while wide-range body-bias control allows dynamic adjustment of the threshold voltage. These features enable significant improvement in retention time, variability tolerance, and ultra-low-voltage operation.

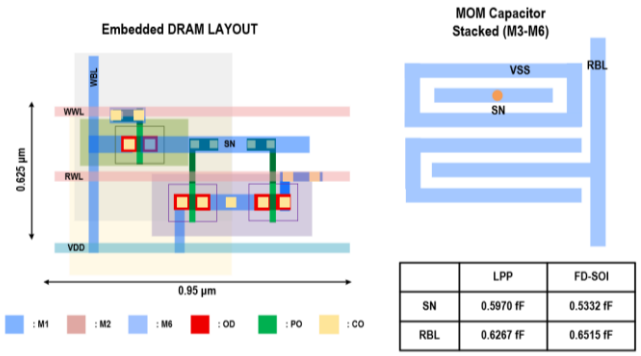
Therefore, FD-SOI is particularly promising for eDRAM applications targeting energy efficient in-memory computing.

II. COMPARISON OF 28-NM LPP AND FD-SOI

A. Coupling Effect of MOM Capacitor

The design challenges of the eDRAM macro are mainly associated with leakage-induced refresh overhead, limited retention time, and variability across process corners.

Fig. 2 shows the schematic of an eDRAM bit-cell based 3-Transistors 2-Capacitor (3T 2C) Structure [4]. To address the retention limitation, this work follows the approach in prior work [5]-[6].



	LPP	FD-SOI
SN	0.5970 fF	0.5332 fF
RBL	0.6267 fF	0.6515 fF

Fig. 3. Layout of 3T 2C eDRAM.

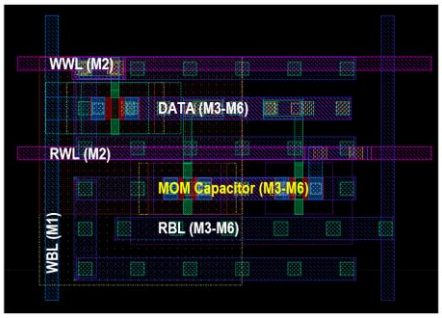


Fig. 4. Top-view layout of 3T 2C eDRAM bitcell.

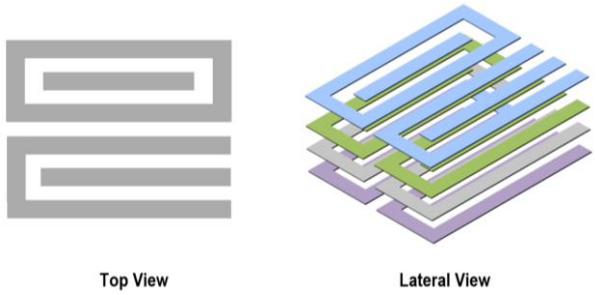


Fig. 5. Top and lateral views of the MOM capacitor structure implemented with stacked metal layers (M3-M6).

In this work, the 3T 2C eDRAM cell was designed in both the 28-nm LPP process and the FD-SOI process to evaluate retention characteristics. The storage node utilizes a MOM capacitor, which exploits the vertical inter-metal dielectric layers to provide high capacitance density without additional process steps.

Fig. 5. shows the MOM capacitor consists of integrated fingers stacked across multiple metal layers (M3-M6), where the effective capacitance can be expressed as

$$C \approx \varepsilon_{eff} \frac{A}{d} + C_{fringe} \quad (1)$$

with ε_{eff} denoting the effective dielectric constant of the IMD stack, A the electrode area, and d the inter-layer spacing.

In addition to the parallel-plate capacitance, fringe capacitance arises from electric fields extending beyond the electrode edges. To analyze its impact, identical 3T 2C eDRAM cells were fabricated in both 28-nm LPP and FD-SOI processes using the same MOM capacitor geometry (M3-M6 stack). Fig. 6. shows transient post-layout simulations performed to observe capacitive coupling at the storage node (SN) during the write operation.

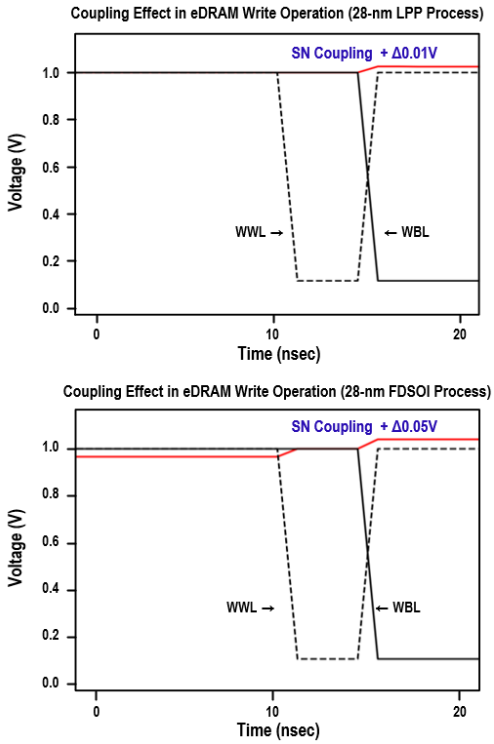


Fig. 6. Comparison of coupling effects during eDRAM write operation in LPP and FD-SOI processes.

The voltage variation at the SN was more pronounced in the FD-SOI process (~0.05 V) than in the LPP process (~0.01 V), indicating stronger capacitive coupling.

This behavior is mainly attributed to the reduced inter-metal dielectric spacing and electric-field confinement by the BOX layer in FD-SOI, which together increase the effective capacitance and enhance charge retention characteristics. The larger voltage transient variation observed in the FD-SOI process indicates stronger capacitive coupling between the storage node and the access lines (WWL and WBL). While this coupling increases the transient voltage swing at the storage node, it also effectively enlarges the total capacitance seen by the storage node.

As a result, stored charge Q = C_{eff} V becomes less sensitive to leakage and process variation. In contrast, the LPP process, which relies on a conductive substrate, exhibits weaker coupling due to partial electric-field dispersion into the bulk silicon. This reduces both the plate and fringe components of the MOM capacitor, resulting in smaller effective capacitance and a narrower voltage margin.

The BOX layer in FD-SOI, however, confines the electric field within the inter-metal dielectric stack, minimizing field leakage to the substrate and reinforcing lateral coupling paths among the stacked metal layers. This confinement explains both the higher coupling amplitude during write transistors and the improved static retention time observed in the FD-SOI implementation.

B. Comparison of Retention Characteristics

To evaluate the retention characteristics under statistical process variations, post-layout Monte Carlo simulations (1000 runs) were conducted for the 3T 2C eDRAM bitcell in both 28-nm LPP and FD-SOI processes at 25°C and 125°C.

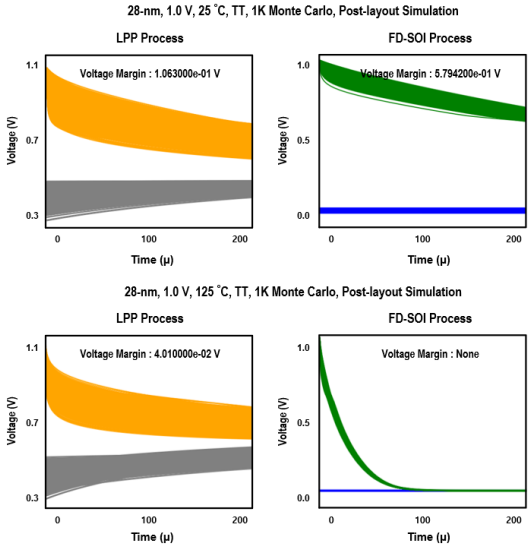


Fig. 7. Retention simulation of 3T 2C eDRAM in 28-nm LPP and FD-SOI at 25˚C and 125˚C..

Each Monte Carlo run includes statistical variations in threshold voltage, effective channel dimensions, and oxide thickness to reflect process variability. The extracted parasitic resistance and capacitance from the layout were included to accurately capture leakage and capacitive coupling effects. During each Monte Carlo run, V_{SN} was monitored over a 200 μs retention window after write and erase operations.

The voltage margin was defined as the voltage difference between the stored '1' and stored '0' states of the SN voltage, representing the effective sensing window of the cell. The voltage margin was measured at 200 μs, which represents a typical retention interval in eDRAM operation. This time point allows for assessing the stability of the stored data after sufficient charge leakage and process-induced variation have accumulated. A larger voltage margin corresponds to improved retention robustness and stronger data separability under process and temperature variations.

As shown in Fig. 7, the FD-SOI process exhibited a substantially larger voltage margin than the 28-nm LPP counterpart at 25 ˚C. This improvement is attributed to the smaller inter-metal dielectric spacing and stronger electric-field concentration enabled by the BOX layer, which enhances the effective capacitance and suppresses leakage to the substrate, resulting in superior retention stability across temperature corners. However, at elevated temperature (125 ˚C), the FD-SOI device shows a severe degradation in voltage margin, while the LPP cell maintains limited but stable retention. This degradation is primarily caused by the self-heating effect and interface-trap generation near the BOX-channel interface in FD-SOI, which increases leakage and disturbs the stored charge over time.

C. *Multiply and Accumulate (MAC) Simulation*

Fig. 8 shows the 3T 2C eDRAM bitcell structure adopted in this work—originally reported by Yoo et al. [4]—which supports logic-compatible in-memory operations via charge sharing and bitline sensing.

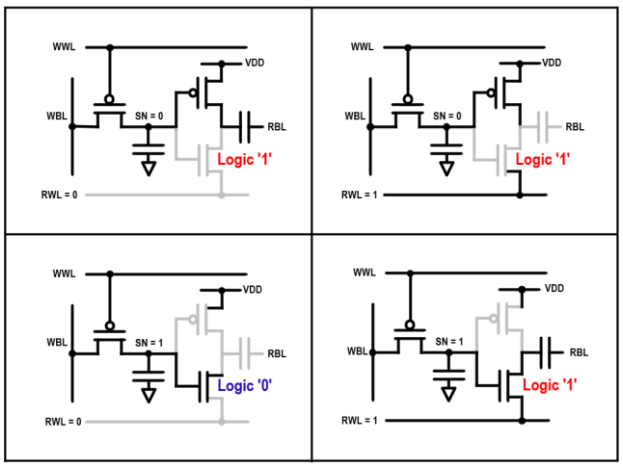


Fig. 8. Write/Read operation mapping of the modified 3T 2C eDRAM cell under different weight and activation inputs.

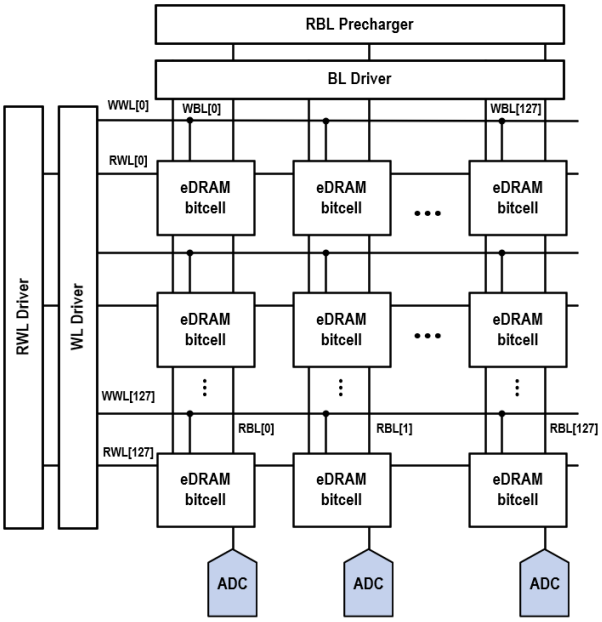


Fig. 9. DRAM bitcell-based CIM array and column-wise MAC operation.

In this work, the same cell topology was modeled and simulated to evaluate its functionality for logic-based accumulation within the memory array. Fig. 9 illustrates the CIM macro based on a 3T 2C eDRAM bitcell array. Each bitcell performs a logic operation between the stored weight and the applied activation from the bitline driver. The resulting voltage change at the storage node determines the output level on the read bitline (RBL), which represents the computed logic result. The bitline outputs from multiple cells within a column are accumulated in the charge domain, allowing the macro to implement multi-bit dot-product computations directly inside the memory array [7].

This architecture inherently supports parallel vector-matrix multiplication, where each column performs accumulation across rows corresponding to input activation. The accumulated analog result is subsequently digitized by a column-parallel ADC, enabling seamless integration with digital processing stages. Through this configuration, the proposed macro achieves both logic-level computation and analog accumulation, combining the benefits of digital robustness and analog efficiency.

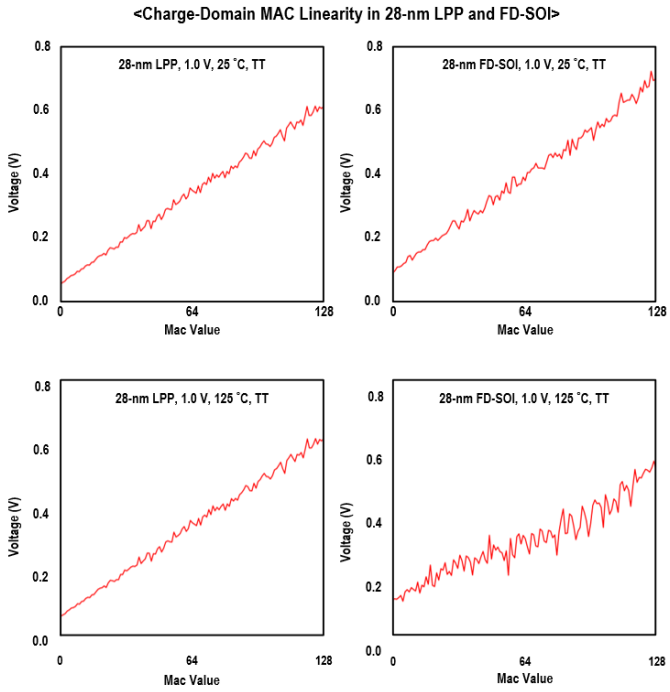


Fig. 10. Linearity of charge – domain MAC transfer in 28-nm LPP vs. FD-SOI process (VDD = 1.0; 25 °C and 125 °C).

To verify the charge-domain behavior of the proposed CIM array, a transient simulation was conducted for both 28-nm LPP and FD-SOI processes under the typical-typical (TT) corner at a 1.0 V supply. In this simulation, the multiply-and-accumulate (MAC) operation was emulated by sequentially accumulating charge from multiple bitcells onto the shared RBL capacitor. Each binary-weighted input pair contributes a quantized charge packet, and the resulting voltage level on the RBL represents the analog MAC output. By sweeping the digital MAC value from 0 to 128, the simulated voltage was mapped to the corresponding MAC result, allowing evaluation of the linearity between the accumulated charge and the expected sum.

As shown in Fig. 10, both processes exhibit a nearly linear relationship between MAC value and the output voltage, validating the accuracy of charge-domain accumulation. At nominal temperature (25 ˚C), the FD-SOI process achieves a slightly wider output-voltage range compared to the LPP process, indicating a higher charge-storage efficiency on the bitline capacitor. This enhancement is primarily attributed to the stronger electric-field confinement and reduced effective capacitance and suppressed leakage to the substrate.

However, when the temperature rises to 125 ˚C, the FD-SOI implementation shows more severe degradation in linearity and output range than its LPP process. This deterioration is mainly caused by self-heating and interface-trap generation near the BOX interface, which perturbs the stored charge and compromises the consistency of analog accumulation. Therefore, while the FD-SOI process provides higher charge efficiency and low-leakage behavior under nominal conditions, its thermal sensitivity imposes reliability limitations under high-temperature operation.

III. RESULTS AND DISCUSSION

To compare the effectiveness of the LPP and FD-SOI processes, post-layout simulations were performed in both 28-nm LPP and FD-SOI processes using an identical MOM capacitor structure. As shown in Fig. 6, the FD-SOI process exhibits a significantly larger voltage margin at 25 °C due to enhanced electric-field confinement and reduced substrate leakage by the BOX layer. However, at 125 °C, severe degradation occurs owing to self-heating and interface-trap formation near the BOX, while the LPP device maintains a relatively stable margin. Coupling analysis in Fig. 5 further confirms stronger capacitive coupling in FD-SOI (~0.05 V) than in the LPP process (~0.01 V), effectively increasing total capacitance and improving nominal retention characteristics.

Finally, Fig. 10 presents the charge-domain MAC operation results. Both processes show a nearly linear relationship at 25 °C between the accumulated charge and the expected MAC value, verifying the linearity of charge-domain accumulation. However, at 125 °C, the FD-SOI process exhibits noticeable distortion in the accumulated voltage, indicating reduced linearity and increased charge dispersion. This degradation is primarily attributed to thermally induced leakage and self-heating effects within the thin BOX layer, which elevate the local device temperature and disturb charge integration on the bitline. In contrast, the LPP process maintains more consistent linear behavior owing to its bulk substrate, which provides better thermal dissipation and stable device characteristics under high-temperature operation. These results highlight a key trade-off between the two technologies—FD-SOI offers superior retention and nominal linearity through enhanced electrostatic control, but its performance degrades more rapidly under thermal stress compared to the LPP process.

IV. CONCLUSION

This work presented a comparative analysis of 3T 2C eDRAM bitcells fabricated in 28-nm LPP and FD-SOI technologies for energy efficient PIM architectures. The FD-SOI process achieved higher effective capacitance and stronger capacitive coupling due to reduced dielectric spacing and BOX-induced electric field confinement, resulting in larger voltage margins and improved retention stability under nominal conditions. Monte Carlo and transient simulations verified reliable operation across temperature and process variations, while the charge-domain MAC behavior maintained high linearity. Although thermal degradation was observed at high temperatures due to self-heating within the BOX layer, the FD-SOI technology provides superior electrostatic control and reduced substrate coupling compared with bulk LPP. Therefore, as device scaling continues to exacerbate short-channel effects, FD-SOI emerges as an effective process technology for achieving stable, scalable, and energy efficient CIM architectures.

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