Low-Complexity Referenceless Clock and Data Recovery with a Novel Alexander Phase-Frequency Detector

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***Abstract* - This paper proposes a low-complexity referenceless clock and data recovery (CDR) circuit for high-speed serial communication systems. Its core contribution is a novel Alexander phase-frequency detector (APFD) that achieves a wide frequency acquisition range with minimal hardware overhead. The proposed APFD generates its frequency tracking signals by utilizing a single inverter on the conventional Alexander phase detector's (APD) UP signal, eliminating the need for complex pattern decoding logic. We theoretically analyze the operational principle by modeling the probabilistic behavior of the detector's outputs, and our analysis is successfully verified through simulations, which show excellent correlation with the derived mathematical model. This APFD is integrated into a comprehensive 32 Gb/s quarter-rate CDR architecture. To ensure robust performance, the system incorporates an adaptive loop gain controller based on the sign-sign LMS algorithm and a direct proportional path with a deadzone mitigation technique to enhance high-frequency jitter tracking. By drastically simplifying the frequency detection mechanism, this work presents a promising solution for next-generation wireline transceivers that offers significant advantages in terms of circuit area and power efficiency.**

***Keywords*— Stochastic Phase Frequency Detector, Referenceless CDR, Wireline LINK**

I. INTRODUCTION

The exponential growth of artificial intelligence (AI), machine learning, and large-scale data centers demands unprecedented data throughput, driving the advancement of high-speed wireline link technologies for chip-to-chip and on-chip communication. In the receivers of these high-speed serial interfaces, the clock and data recovery (CDR) circuit is the most critical block that determines the overall performance and reliability of the system. As data rates escalate from tens to hundreds of Gb/s, CDR circuits face the dual challenge of achieving high jitter performance while meeting stringent low-power and small-area requirements.

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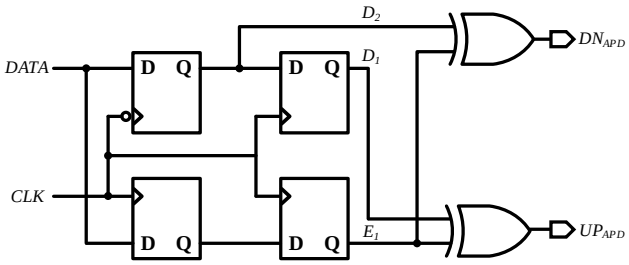

Fig. 1. Conventional APD block diagram

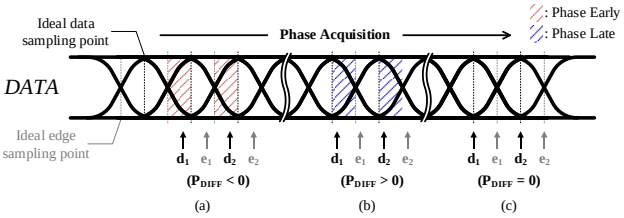

Fig. 2. Conventional APD;
(a) Phase early state (b) late state (c) locked state

Recent CDR architectures have undergone a significant paradigm shift to meet these demands. Traditionally, dual-loop architectures, which employ separate frequency-locked and phase-locked loops to secure wide frequency acquisition range, were widely used. However, this structure inherently suffers from complex interactions between the two loops, large area, and high-power consumption. Consequently, the mainstream of modern CDR design has shifted towards integrating both phase and frequency acquisition within a single loop. In particular, referenceless single-loop CDRs, which operate without an external reference clock to reduce pin count and power consumption, are gaining prominence due to their high integration density and cost-effectiveness in system-on-chip (SoC) designs [1].

Nevertheless, existing single-loop referenceless CDR architectures still face unresolved challenges. Numerous studies have attempted to compensate for wide frequency offsets quickly and accurately without a reference clock. For instance, recent advancements incorporate complex mixed-signal or digital-intensive techniques, such as SAR-based frequency acquisition, to achieve rapid locking [2]. However, these approaches inevitably introduce substantial hardware and power overhead. As a hardware-efficient alternative for phase detection, the Alexander phase detector (APD) [3] has been widely adopted due to its intuitive and simple structure,

utilizing data-edge-data (D_1-E_1-D_2) consecutive samples (Fig. 1 and Fig. 2). While the APD achieves stable phase locking with minimal area, its inherent design detects only phase differences, suffering from severe phase slips under large frequency offsets and failing to extract frequency information directly [4].

To overcome this limitation of the APD and implement a frequency detection function within a single loop, advanced techniques such as the stochastic approach have been proposed [5], [6]. These techniques extract frequency information by leveraging the fact that the occurrence probability of specific D_1-E_1-D_2 patterns changes with frequency error. Although these works have successfully demonstrated the feasibility of frequency detection without additional high-speed samplers, they still require significant digital logic overhead, such as integrator-based architectures [6] or multiple pattern decoders [7], to decode all patterns and calculate complex weights.

This work is an extended development of our previous research on Alexander-based frequency detectors [8]. Here, we enhance this idea by proposing a highly simplified APFD that requires only a single inverter to generate frequency-tracking signals, fundamentally eliminating the need for the complex pattern decoding logic seen in prior stochastic detectors. This improved detector is then implemented within a full 32 Gb/s quarter-rate CDR, and its performance is validated, confirming its suitability for high-speed applications.

II. DESIGN METHODOLOGY

A. Analysis of Stochastic Characteristics of APD

This section describes the design of the proposed low-complexity phase-frequency detector. First, we analyze the stochastic approach of a prior work that inspired our design. Based on this analysis, a new architecture and its theoretical operating principles are presented. Finally, the validity of the proposed method is verified by comparing the theoretical analysis with simulation results.

Conventional methods for implementing the frequency acquisition function in a referenceless CDR have mostly required complex additional circuits. To overcome this limitation, a stochastic method was proposed that utilizes the statistical distribution of the three consecutive bit patterns (D_1, E_1, D_2) sampled by an APD.

The prior work noted that the occurrence probability of the eight patterns (from 000 to 111) varies depending on the phase and frequency offsets [5]. The analysis confirmed that pattern groups are statistically distinguishable between a fast clock (clock frequency is higher than the data rate) and a slow clock. For instance, when the clock is fast, patterns where D_1 and E_1 have the same value (000, 001, 110, 111) tend to occur more frequently. Conversely, when the clock is slow, patterns where D_1 and E_1 have different values (010, 011, 100, 101) show a higher probability of occurrence.

Based on these statistical properties, it was demonstrated that by assigning a unique weight to each pattern and calculating their sum, both frequency and phase information

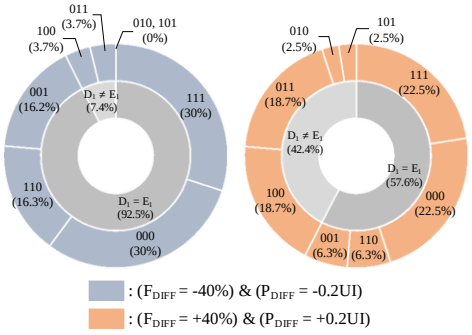

Fig. 3. Probability of D_1, E_1, D_2 pattern occurrence with frequency and phase offsets

could be extracted simultaneously within a single loop. Although this method showed that frequency detection is possible in an APD structure without additional high-speed samplers, it still has a limitation of requiring complex digital logic to decode all eight patterns and apply different weights for summation.

The stochastic approach described above clearly indicates that frequency information is embedded within the APD's sampled results. Inspired by this idea, this paper proposes a new architecture that extracts frequency information with extremely simplified hardware, eliminating the need for complex weight calculation logic.

B. Proposed Alexander Phase-Frequency Detector

The proposed architecture is derived from a stochastic analysis of $D_1-E_1-D_2$ pattern probabilities. Fig. 3, adapted from [5], illustrates these probabilities under two distinct offset conditions. The left chart (blue) corresponds to a fast-clock scenario (F_{DIFF} = -40%, P_{DIFF} = -0.2UI), where a DN signal is required. The right chart (orange) corresponds to a slow-clock scenario (F_{DIFF} = +40%, P_{DIFF} = +0.2UI), where an UP signal is needed. F_{DIFF} is defined as

$$F_{DIFF} = \frac{f_{DATA,Nyquist} - f_{CLK,Nyquist}}{f_{CLK,Nyquist}} \qquad (1)$$

By comparing the probabilities of identical patterns across these two opposing conditions, a maximum likelihood approach was adopted. Each pattern was decisively assigned to the condition under which it was more likely to occur. For instance, the '111' pattern shows a 30% probability in the fast-clock case versus 22.5% in the slow-clock case. Since its likelihood is higher in the fast-clock condition, the '111' pattern is exclusively assigned to generate a DN signal. After applying this principle to all eight patterns, a clear rule emerged: patterns with $D_1 = E_1$ consistently correlated with the fast-clock condition (DN), while patterns with $D_1 \neq E_1$ correlated with the slow-clock condition (UP). Remarkably, this resulting logic is identical to using the conventional APD's UP signal ($D_1 \oplus E_1$) and its inverse for the DN signal.

The proposed architecture implements the frequency tracking function by modifying the UP and DN generation logic of a conventional APD, as shown in the block diagram

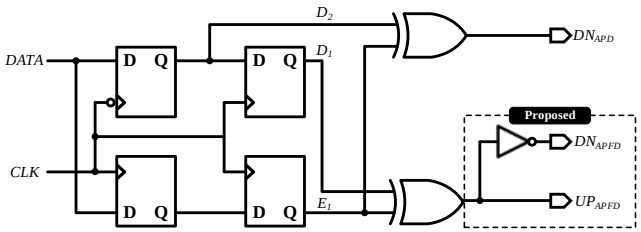

Fig. 4. Proposed APFD

$$UP\ Signal: UP_{APFD} = D_1 \oplus E_1 \quad (2)$$

$$DN\ Signal: DN_{APFD} = \overline{UP_{APFD}} = \overline{D_1 \oplus E_1} \quad (3)$$

of the proposed APFD in Fig. 4. The UP signal from the conventional APD is used directly for both phase and frequency control. However, the DN signal for frequency control is generated not by the conventional APD's DN logic, but simply by adding an inverter to the UP signal.

The core of this architecture is that it reuses a single UP signal to create two control signals, thereby eliminating the need for a separate complex decoder or pattern analysis circuit for frequency detection. This leads to a significant reduction in hardware complexity and power consumption.

To prove the principle by which the proposed structure detects and compensates for frequency error, the occurrence probabilities of the UP and DN signals were theoretically analyzed based on the relationship between the clock period (T_c) and the data unit interval (T_d).

The occurrence probabilities of the UP and DN signals are determined by the relative positional relationship of the D_1, E_1, and D_2 sampling instances, which varies due to the frequency difference between the clock and data. The positional relationship of these three sampling points within a single unit interval (UI) of the data stream can be analyzed by dividing it into several cases. Fig. 5 illustrates representative cases according to the frequency offset.

The probability of each case occurring is determined by the ratio of its time duration to the total data period, T_d. Within each case, the relative positions of D_1, E_1, and D_2 are fixed, thus limiting the possible 3-bit patterns that can occur. Assuming the data bits are random, the conditional probability of a specific pattern occurring can be calculated.

For example, let's consider the case where $0.5f_d < f_c < f_d$. In this condition, the time axis can be divided into three main regions. The first region (colored red in Fig. 5(b)) has a duration of $T_d - 0.5T_c$. In this region, D_1 and E_1 are located in the same UI, while D_2 is in the next UI. The four possible patterns (000, 001, 110, 111) all have the same value for D_1 and E_1, thus generating a DN signal. Therefore, the probability of the DN signal in the red region can be obtained through conditional probability as shown in Equation (4).

$$\Pr(DN, red) = \frac{T_d - 0.5T_c}{T_d} \times 1 \quad (4)$$

$$\Pr(UP, red) = \frac{T_d - 0.5T_c}{T_d} \times 0 \quad (5)$$

Similarly, the second region (colored blue in Fig. 5(b)) also has a duration of $T_d - 0.5T_c$. Here, D_1 and E_1 are located

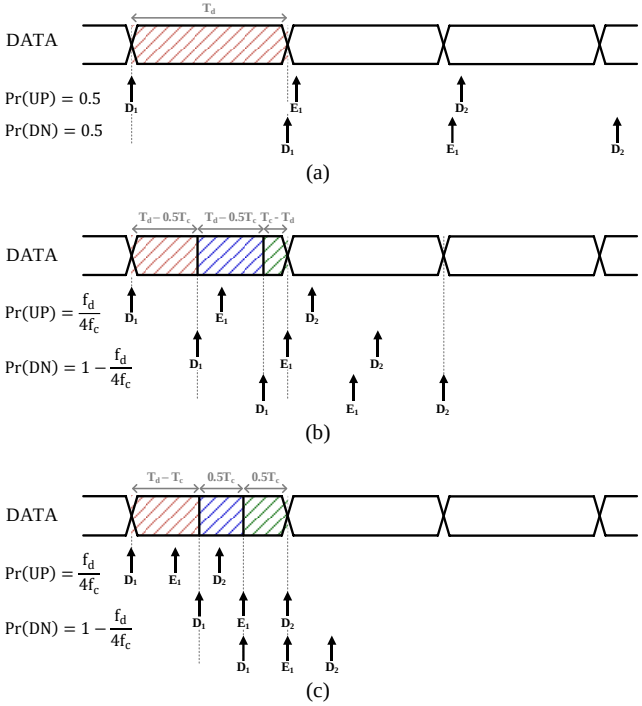

Fig. 5. Timing diagram for calculating output probability in APFD;
(a) Frequency range of $f_c < 0.5f_d$
(b) Frequency range of $0.5f_d < f_c < f_d$
(c) Frequency range of $f_d < f_c$

in different UIs, meaning their values are independent. Thus, they have a 50% chance of being identical, yielding Equation (6).

$$\Pr(DN, blue) = \Pr(UP, blue) = \frac{T_d - 0.5T_c}{T_d} \times 0.5 \quad (6)$$

The third region (colored green) spans the remaining duration of $T_c - T_d$. In this region, all three samples (D_1, E_1, D_2) fall into separate consecutive UIs. As they are completely independent, the probability for both UP and DN is again 50%, resulting in Equation (7).

$$\Pr(DN, green) = \Pr(UP, green) = \frac{T_c - T_d}{T_d} \times 0.5 \quad (7)$$

By summing these regional probabilities (e.g., Pr(UP) = Pr(UP, red) + Pr(UP, blue) + Pr(UP, green)), the final occurrence probabilities for a given frequency offset condition ($0.5f_d < f_c < 1.5f_d$) can be derived as shown in Equations (8) and (9):

$$\Pr(UP) = \frac{f_d}{4f_c} \ (0.5f_d < f_c < 1.5f_d) \quad (8)$$

$$\Pr(DN) = 1 - \frac{f_d}{4f_c} \ (0.5f_d < f_c < 1.5f_d) \quad (9)$$

These equations show that the probabilities of UP and DN vary asymmetrically with the frequency error. For a stable

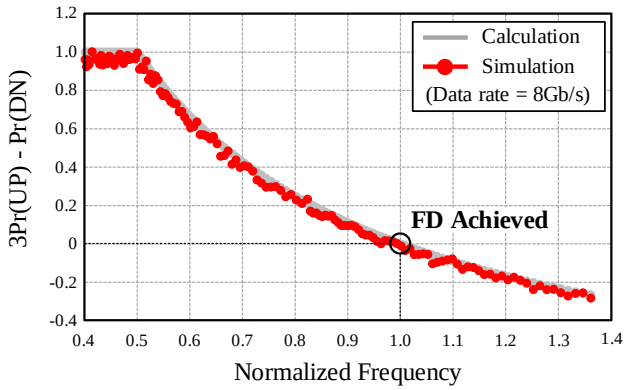

Fig. 6. Calculated and simulated frequency detection curves

frequency lock, the net control signal into the loop filter must be zero when the frequency error is zero ($f_c = f_d$). However, substituting $f_c = f_d$ into the equations yields Pr(UP)=0.25 and Pr(DN)=0.75. Since the probabilities are not equal, the loop will be biased to one side.

To solve this problem, a weighting technique is applied to the UP signal to equalize the control effectiveness of both signals. The analysis confirmed that by applying a weight of 3 to the UP signal, the loop's balance is achieved at the zero-frequency-error point. The weighted frequency detection characteristic is expressed by Equation (10).

$$3 \times \Pr(UP) - \Pr(DN) = 3 \times \left(\frac{f_d}{4f_c}\right) - \left(1 - \frac{f_d}{4f_c}\right) = \frac{f_d}{f_c} - 1 \quad (10)$$

Equation (10) shows that the average value of the weighted control signal has a linear relationship with the frequency offset near the target frequency, and it becomes exactly zero when the frequency error is zero. This theoretically proves that effective frequency tracking is possible with only the proposed simple structure and weight setting.

To validate the derived theoretical equations, simulations were performed, and the results were compared with the theoretical values. The simulation used an 8Gb/s random data pattern as input, and the occurrence probabilities of the UP and DN signals were measured while applying various frequency offsets.

Fig 6. shows the calculated and simulated results for 3×Pr(UP)−Pr(DN) through both calculation and simulation. The horizontal axis of the graph represents the normalized frequency, which is the ratio of the clock frequency to the data frequency (f_c/f_d). The two curves match almost perfectly, and notably, they pass exactly through zero where the Normalized Frequency is 1, which signifies the frequency lock point.

These results clearly substantiate the main claim of this paper: with the proposed ultra-simple structure merely applying an inverter to the conventional APD's UP signal and assigning it a 3x weight it is possible to linearly detect a wide range of frequency errors and achieve a stable lock.

C. Referenceless CDR with Proposed APFD

In the previous section, the proposed APFD was verified to have effective frequency tracking capability. This section provides a detailed description of the overall referenceless CDR system architecture, which is designed utilizing this APFD as a core block. The proposed CDR is designed to operate reliably at a data rate of 32 Gb/s, and additional design techniques have been applied to achieve low power consumption and high performance.

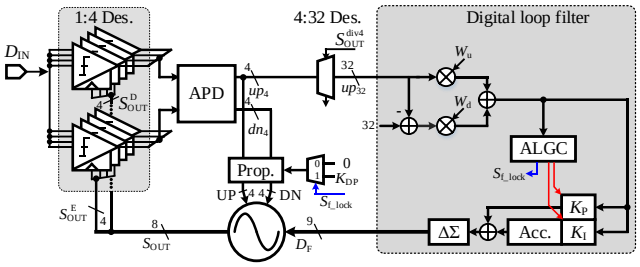

Fig. 7. Block diagram of the referenceless CDR with the proposed APFD

The overall block diagram of the proposed CDR is shown in Fig. 7. The system is based on a quarter-rate architecture to reduce the burden of high-speed operation and facilitate low-power design. The input data (D_{IN}) is converted into four parallel data streams by a 1:4 deserializer (Des.). In this process, four data samples and four edge samples are generated. These signals are then fed into an APD to generate UP and DN signals. The outputs from the APD are then directed into two main paths. One is the 'digital loop filter path', which is responsible for integrated frequency and phase tracking. The other is the 'Direct Proportional Path', which performs fast phase correction by directly feeding the output of the APD to the digitally controlled oscillator (DCO), as shown in Fig. 7.

The digital loop filter receives signals processed by the APD and a 4:32 deserializer to implement the proposed APFD logic. Although the block diagram conceptually depicts the use of an inverter to generate the DN signal, the actual implementation within the digital logic employs a highly hardware-efficient method based on the mutual exclusivity of the control signals. In the proposed APFD logic, the generation of UP and DN signals for frequency tracking is perfectly mutually exclusive; a specific 3-bit pattern yields either an UP or a DN signal, but never both. Consequently, any sample that does not assert an UP signal inherently represents a DN condition. Specifically, as the 32 parallel UP signals (up_{32}) enter the filter, the effective value of the DN signal is calculated by subtracting the number of active '1's in the UP signals from the total bit count of 32. By leveraging this mutually exclusive property, the equivalent logic of 32 physical inverters is seamlessly replaced by a single arithmetic subtraction (i.e., $DN = 32 - \Sigma UP$) within the digital domain, significantly reducing the hardware complexity. Inside the filter, weights (W_u, W_d) are applied to the UP and DN signals, respectively, to calculate the frequency and phase error. This error is then processed by an accumulator (Acc.) and a delta-sigma modulator (ΔΣ) to generate a 9-bit digital code (D_F) that controls the frequency of the DCO. To optimize the overall loop performance and stability, an adaptive loop gain controller (ALGC) is included to dynamically adjust the loop gain.

Maintaining an optimal loop bandwidth is crucial for a high-performance CDR. An overly wide bandwidth can

degrade jitter transfer characteristics, while a bandwidth that is too narrow can impair jitter tolerance. The proposed CDR employs an ALGC based on the sign-sign least mean square (SS-LMS) algorithm to optimize the loop gains, K_p and K_i, in real-time.

The ALGC adjusts the loop gain by calculating the correlation between the current and previous outputs of the phase detector. When the loop is in an optimal state, this correlation approaches zero. If the correlation is positive, it implies that the loop gain is too high, and thus the gain is decreased. Conversely, if it is negative, the gain is too low and is therefore increased. This ensures that the CDR consistently maintains optimal performance even when input jitter characteristics or operating conditions change.

While the proposed APFD has a strong capability for frequency tracking, it introduces significant latency due to the digital logic within the loop filter. This latency can limit its ability to track high-frequency jitter. To mitigate this issue and maximize phase tracking performance, a Direct Proportional Path that directly feeds the output of the APD to the DCO has been added. This path bypasses the digital loop, delivering the phase correction signals (UP, DN) to the DCO instantaneously, which minimizes loop latency and effectively extends the CDR's bandwidth.

However, a conventional proportional path can suffer from performance degradation due to the deadzone phenomenon, where the APD does not respond to very small phase errors. To address this problem, the proposed CDR applies a technique that adjusts the gain of the proportional path (K_{DP}) by detecting the frequency lock state (S^{F}_{lock}). During the initial frequency acquisition phase, the proportional path is disabled, or its gain is lowered to facilitate a stable lock. Once frequency lock is achieved, the gain of the proportional path is increased to enable precise phase tracking. This control scheme mitigates the deadzone issue and improves the overall jitter performance [9], [10].

III. SIMULATION RESULTS

To verify that the proposed APFD operates as intended within a complete closed-loop CDR system, a full system simulation was performed in a 28-nm CMOS process technology based on the architecture described in Section II. The simulation used a 32 Gb/s PRBS (Pseudo-Random Binary Sequence) data as input.

As shown in Fig. 8, the simulation of the CDR's frequency acquisition process under various initial DCO frequency conditions demonstrates that the output frequency successfully converges to the 8 GHz target, regardless of the initial frequency. Although the time to reach the target frequency varies with the initial frequency offset, the simulation results indicate that a stable frequency lock is achieved after approximately 3.6 μs for all initial conditions. This clearly demonstrates that the proposed APFD has a wide capture range and reliably detects and compensates for the frequency error within the closed-loop system.

This robust frequency acquisition performance proves that the proposed low-complexity APFD is successfully integrated into the overall CDR system, achieving stable operation at the target data rate of 32 Gb/s. Achieving a stable frequency lock lays the foundation for successful fine phase tracking and data recovery, which will be subsequently handled by the ALGC and the Direct Proportional Path.

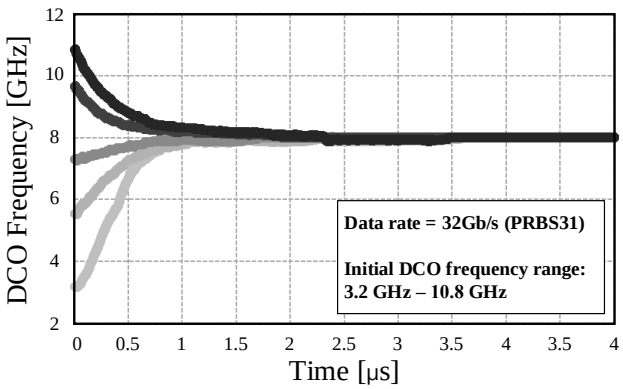

Fig. 8. Measured frequency acquisition behavior for various initial clock Frequencies

IV. CONCLUSION

This paper has proposed a low-complexity referenceless CDR for high-speed serial communications. The core contribution is a novel Alexander Phase-Frequency Detector (APFD) that implements frequency detection capability by adding only a single inverter to the conventional Alexander Phase Detector (APD) architecture. Theoretical analysis and simulation successfully verified that the proposed APFD can effectively track a wide range of frequency errors by utilizing the stochastic properties of the UP signal and a weighting scheme, without the need for complex pattern decoding logic. Based on the validated APFD, a complete CDR system targeting 32 Gb/s operation was designed. A quarter-rate architecture was adopted to minimize power consumption in high-speed operation. An adaptive loop gain control (ALGC) based on the sign-sign LMS algorithm was included to maintain optimal jitter performance under various operating conditions. Furthermore, to minimize loop latency and enhance phase tracking capability, a Direct Proportional Path was introduced, and the deadzone issue was mitigated by adjusting its gain based on the frequency lock state.

In conclusion, this work presents a new CDR design methodology that achieves both frequency and phase synchronization with extremely simplified hardware. The proposed architecture is expected to have significant advantages in terms of area and power consumption, which will be a crucial contribution to the implementation of next-generation wireline communication systems that demand higher integration and energy efficiency.

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