# A Temperature-Compensated LDO without External Reference for Compact SoC Design in 65nm CMOS

Beomsoo Kim[1], Yuli Han[4], Chanjung Park[1],
Byungjae Kwag[2], Minwoo Kim[3], Sangbin Tae[2], and Kunhee Cho[1,a]
[1]Department of Semiconductor Convergence Engineering, Sungkyunkwan University
[2]Department of Electrical and Computer Engineering, Sungkyunkwan University
[3]School of Electronic and Electrical Engineering, Kyungpook National University
[4]DB Global Chip, South Korea
E-mail : tmnman@g.skku.edu

***Abstract* - This paper presents a low-dropout (LDO) regulator with an embedded voltage reference (EVR), designed for system-on-chip (SoC) architectures requiring high-performance operation. The proposed design integrates the voltage reference directly into the error amplifier (EA), enabling the generation of a 0.95 V output from a 1.05 V input while maintaining a low temperature coefficient and robust loop stability. The circuit comprises a proportional-to-absolute-temperature (PTAT) current generator, an EVR-based EA, and a power MOSFET. The LDO has been implemented in 65nm CMOS process. The simulation results demonstrate a stable output voltage of 0.95 V with a TC of 218 ppm/°C over a wide temperature range from -60°C to 120°C. A peak current efficiency of 99.99 % is obtained, maintaining stable operation and current driving capability up to 220 mA.**

***Keywords* — CMOS, low-dropout regulator, embedded-voltage-reference.**

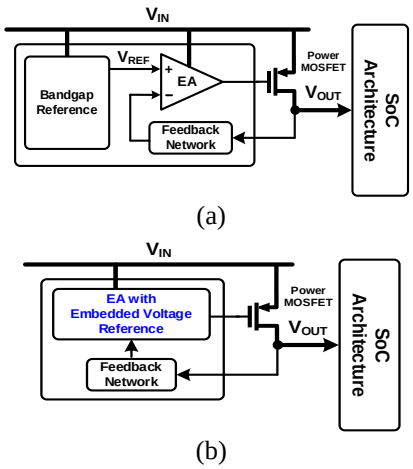


Fig. 1. LDO architecture. (a) With external voltage reference. (b) Embedded voltage reference.

## I. INTRODUCTION

A bandgap reference (BGR) voltage circuit is commonly employed in conventional low-dropout (LDO) voltage regulator designs to generate a stable reference voltage $V_{REF}$ with a low temperature coefficient (TC), as illustrated in Fig. 1. [1]-[4] However, BGR circuits suffer from limited voltage headroom under low-voltage operation. Moreover, traditional LDO regulators face challenges in achieving low power consumption and compact chip area due to the need for separate error amplifiers, resistive networks for both the regulator and the BGR, and the extensive use of bipolar junction transistors (BJTs) in the BGR.

To eliminate the additional voltage reference circuitry, LDO architectures integrating an error amplifier (EA) with an embedded voltage reference (EVR) have been demonstrated [5], [6]. These designs achieve reduced power consumption and compact chip area by removing the need for a discrete voltage reference. However, the output voltage of such LDOs is constrained by the condition for achieving zero TC, which typically fixes the output at a low voltage (e.g., 0.6 V). This low voltage level is unsuitable for system-on-chip (SoC) applications that demand higher nominal supply voltages, such as 0.9 V or above, for high-performance operation.

This paper proposes an LDO regulator architecture featuring an EA integrated with an EVR, capable of providing a nominal output voltage suitable for SoC applications requiring supply voltages above 0.9 V. The proposed design incorporates an EA with EVR, a feedback network employing a boosting technique, a power MOSFET, and a beta-multiplier for start-up operation. Circuit behavior analysis, small-signal modeling, and simulation results confirm that the proposed LDO, delivering a 0.95 V output from a 1.05 V input, achieves a compact controller area without the need for a bandgap reference circuit.

## II. PROPOSED ARCHITECTURE

Fig. 2 shows the proposed LDO architecture consisting of a beta-multiplier, an EA with EVR, feedback network including output boosting MOSFET $M_{BOOST}$, and power MOSFET $M_{PWR}$. To generate a proportional to absolute temperature (PTAT) current, the beta-multiplier is used. This current, combined with the negative temperature dependence of the $V_{GS}$ of the MOSFET $M_A$, forms a voltage with a near-zero temperature coefficient through the current

a. Corresponding author; kunhee@skku.edu

Manuscript Received Jul. 22, 2025, Revised Aug. 17, 2025, Accepted Aug. 18, 2025

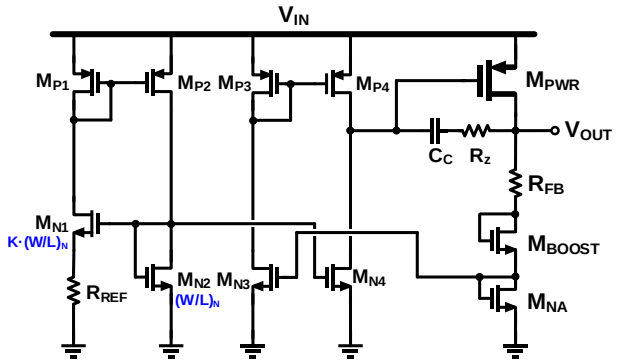


Fig. 2. Schematic of proposed output-boosting LDO with EVR EA.

feedback loop generated by the EA. In conventional architectures, the limited low output voltage was created to nsure both temperature coefficient (TC) close to zero and loop stability. In this work, an additional diode-connected MOSFET is incorporated into the feedback network to boost the output voltage level. This enables a stable output voltage level boosting without affecting the TC or the loop stability.

### *A. PTAT Current Generator*

The gate-source voltages of the MOSFETs exhibit complementary-to-absolute-temperature (CTAT) behavior. To compensate for these CTAT voltages, a PTAT current must be generated and delivered to the feedback network. In this paper, we adopt a beta-multiplier-based generator to produce a proportional-to-absolute-temperature (PTAT) current, as illustrated in Fig. 3. The PTAT current produced by the beta-multiplier is given by Equation (1):

$$I_{PTAT} = \frac{2}{\mu_n C_{ox}(W/L)_N}\frac{1}{R_{REF}^2}\left[1-\frac{1}{\sqrt{K}}\right]^2 \quad (1)$$

Here, $C_{ox}$ is the oxide capacitance, $(W/L)_N$ is the unit aspect ratio of $M_{N1}$ and $M_{N2}$, and K represents the current mirror ratio from $M_{N2}$ to $M_{N1}$. These parameters have no impact on the temperature coefficient (TC). Consequently, the TC of $I_{PTAT}$ is primarily governed by the temperature dependence of the NMOS mobility $\mu_n$ and the resistor $R_{REF}$. According to Equation (2), the resistance of $R_{REF}$ varies linearly with temperature due to its temperature coefficient α.

$$R_{REF} = R_{REF0}[1+\alpha(T-T_0)] \quad (2)$$

In this equation, temperature $T$ is expressed in units of Kelvin (K). By considering the temperature dependence, the TC of the PTAT current is approximated by Equation (3):

$$TC_{I_{PTAT}} \approx -2\alpha + \frac{1.5}{T} \quad (3)$$

In the case where a TC of polysilicon resistor α behaves as CTAT (α is -314.4 ppm/°C in this paper), the generated current $I_{PTAT}$ demonstrates a PTAT characteristic. This proposed design incorporates a CTAT-like resistor into the beta-multiplier structure to generate the PTAT current. The current mirror replicates the PTAT current to generate $I_{N4}$ which serves as the bias current for the error amplifier (EA). The bias current, $I_{N4}$, as shown in Fig. 3, is defined by Equation (4):

$$I_{N4} = \frac{(W/L)_{N4}}{(W/L)_{N2}} I_{PTAT} = I_{PTAT} \quad (4)$$

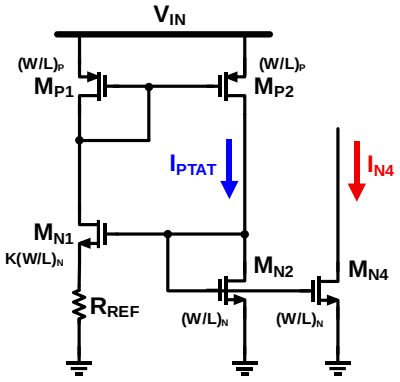


Fig. 3. PTAT current generator circuit.

Therefore, the temperature characteristic of $I_{N4}$ follows that of the $I_{PTAT}$. This current is used to bias the error amplifier.

### *B. Proposed Embedded-voltage-reference EA*

The proposed embedded-voltage-reference error amplifier is depicted in Fig. 4. To raise the output voltage level with temperature coefficient compensation and output voltage stability, the proposed structure adds an additional boosting transistor, $M_{BOOST}$. The PTAT current $I_{N4}$ is delivered to $I_{NA}$ through the current feedback loop and current mirror in the proposed EA. By exploiting the CTAT characteristic of the MOSFET's $V_{GS}$, a temperature-compensated output voltage is finally achieved. The N-type current mirror $M_{NA}$, $M_{N3}$ and P-type current mirror $M_{P3}$, $M_{P4}$ define $I_{NA}$ as follows:

$$I_{NA} \approx \frac{I_{PTAT}}{K_N K_P} \qquad K_N = \frac{(W/L)_{N3}}{(W/L)_{NA}}, K_P = \frac{(W/L)_{P4}}{(W/L)_{P3}} \quad (5)$$

where $K_N$ is an N-type current mirror ratio ($M_{NA}$, $M_{N4}$), and $K_P$ is a P-type current mirror ratio ($M_{P3}$, $M_{P4}$). On the other hand, the negative feedback with the compensation capacitance and resistance, $C_C$ and $R_Z$, regulates $V_{OUT}$ by forcing $i_{N4}$ and $i_{P4}$ to be equal, thereby determining overall stability. Therefore, $i_{N4}$ can be expressed as shown in Equation (6).

$$i_{N4} = \frac{A_C}{1+A_C} i_{P4} \approx i_{P4} \quad (6)$$

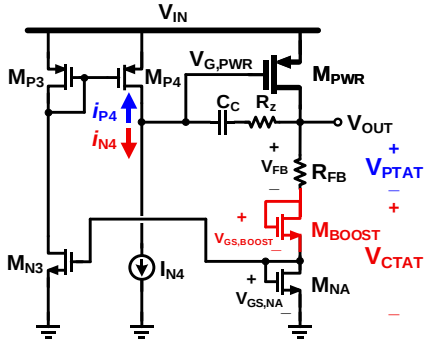


Fig. 4. Proposed embedded-voltage-reference error amplifier.

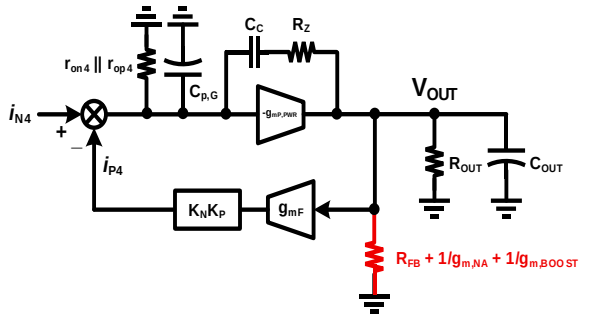


Fig. 5. Small signal model for stability analysis

$A_C$ is the current loop gain from $i_{N4}$ and $i_{P4}$ and is given by Equation (7):

$$A_C = \frac{-g_{mp,PWR} \cdot R_{OUT} \cdot K_N K_P}{(r_{on4} || r_{op4}) \left[ R_{OUT} + (R_{FB} + \frac{1}{g_{m.NA}} + \frac{1}{g_{m.BOOST}}) \right]} \quad (7)$$

where $g_{mp,PWR}$ and $g_{mn,NA}$ are the transconductance of the power MOSFET $M_{PWR}$ and the MOSFET in feedback network $M_{NA}$, $R_{FB}$ is a feedback resistor, and $R_{OUT}$ is an output load. As demonstrated in Equation (7), the effect of $M_{BOOST}$ can be negligible due to the fact that the sum of $R_{OUT}$ and $R_{FB}$ is much higher than $1/g_{m,BOOST}$. Therefore, the output voltage $V_{OUT}$ is determined by the sum of the $V_{GS,NA}$, the $V_{GS,BOOST}$, and the $V_{FB}$, as expressed as Equation (8):

$$V_{OUT} = V_{GS,NA} + V_{GS,BOOST} + \theta_{PTAT} \frac{1}{\mu_n} \quad (8)$$

$$\theta_{PTAT} = \frac{1}{K_N K_P} \frac{2}{C_{ox}(W/L)_N} \frac{R_{FB}}{R_{REF}^2} \left[ 1 - \frac{1}{\sqrt{K}} \right]^2 \quad (9)$$

The $V_{GS,NA}$ and $V_{GS,BOOST}$ have CTAT characteristics because the temperature effect of the threshold voltage is more dominant than that of the MOSFET's mobility, while the feedback resistor voltage $V_{FB}$ has a PTAT characteristic combined with the PTAT current. When generating $V_{FB}$, which serves as $V_{PTAT}$, the resistive ratio between $R_{FB}$ and $R_{REF}$ alleviates the effects of the non-linear characteristic in $I_{PTAT}$. To obtain a zero temperature coefficient of the output voltage, we adjust the values of the ratio of resistors, the aspect ratio $(W/L)_N$ and the N-type current mirror ratio $K$ of the PTAT generator, the current mirror ratio $K_N K_P$ in the proposed EA.

Moreover, the addition of the $M_{BOOST}$ has a negligible effect on the stability of the output voltage as well. Fig. 5 illustrates the small signal model of the proposed LDO architecture. The $g_{mF}$ represents the feedback factor and can be expressed as Equation (10):

$$g_{mF} = \frac{1}{R_{FB} + 1/g_{m,NA} + 1/g_{m,BOOST}} \quad (10)$$

The only stability impact of introducing $M_{BOOST}$ is the small reduction of transconductance from the output node toward the feedback network due to the large $R_{FB}$. As a result, the first non-dominant pole $P_{OUT}$ moves to the lower frequency negligibly. Additionally, the left-half-plane (LHP) zero $Z_C$, created by the compensation capacitance $C_C$ and resistance $R_Z$, is adopted to improve stability and extend bandwidth.

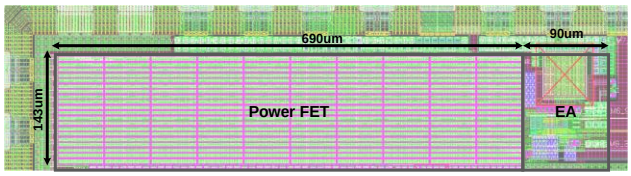


Fig. 6. Proposed IC layout.

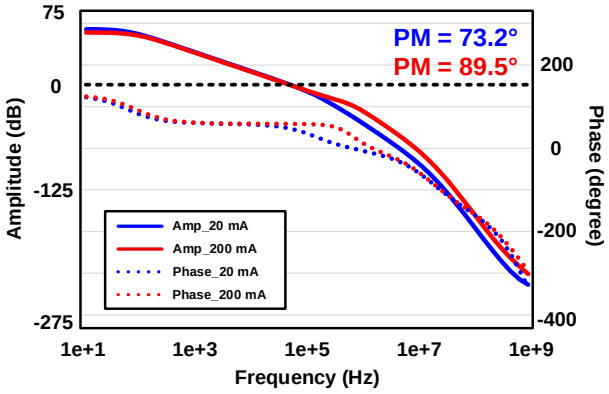


Fig. 7. Stability of the proposed LDO according to the load current.

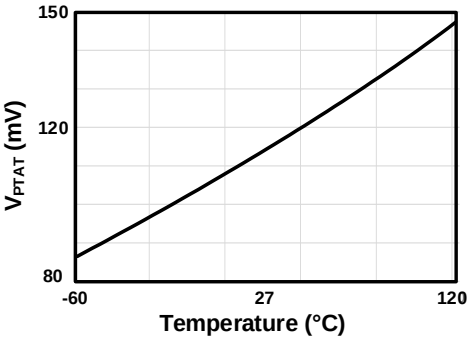


Fig. 8. Temperature plot of the PTAT voltage.

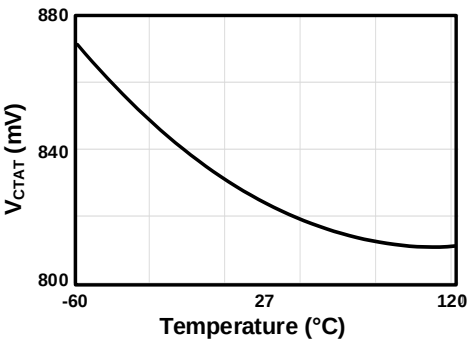


Fig. 9. Temperature plot of the CTAT voltage.

## III. RESULTS AND DISCUSSIONS

The proposed embedded-voltage-reference LDO was implemented by the 65nm process (Fig. 6). The total chip area of the proposed LDO, including power MOSFET, is 0.0987 $mm^2$ for high current capability. The main controller

TABLE I. Performance Comparison.

| | **This work** | **[5]** | **[6]** | **[1]** | **[2]** |
|---|---|---|---|---|---|
| **Process [nm]** | **65** | 21 | 180 | 65 | 500 |
| **Voltage reference** | **Embedded** | Embedded | Embedded | BGR | BGR |
| **$V_{IN}$ [V]** | **1.05** | 0.65 – 0.9 | 0.7 – 1.1 | 1.15 – 1.3 | 2.2 – 5 |
| **$V_{OUT}$ [V]** | **0.95** | 0.6 | 0.6 | 1 | 2 – 4.85 |
| **Max. $I_{LOAD}$ [mA]** | **220** | 10 | 30 | 25 | 300 |
| **$I_Q$ [uA]** | **9** | 5 | 0.22 – 660 | 150 | 50 |
| **Output capacitance [uF]** | **1** | 0.1 | 0 – 0.3 | 4 – 4.7 | 1 |
| **Peak current efficiency [%]** | **99.99** | 99.95 | 97.7 | 99.4 | 99.98 |
| **Temperature Coefficient [ppm/°C]** | **218** | 30 | 33.1 | - | - |
| **Max current density [A/mm$^2$]** | **1.97** | 0.67 | 0.4 | 0.69 | 0.77 |
| **Total area[mm$^2$]** | **0.1115** | 0.015 | 0.075 | 0.036 | 0.39 |

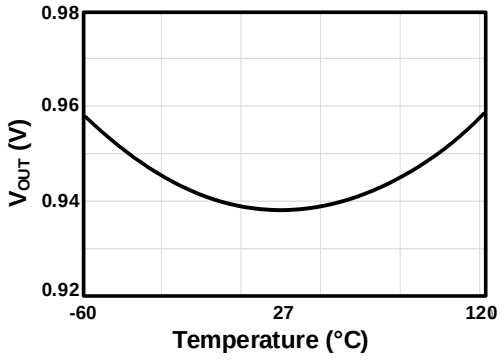


Fig. 10. Temperature plot of the output voltage.

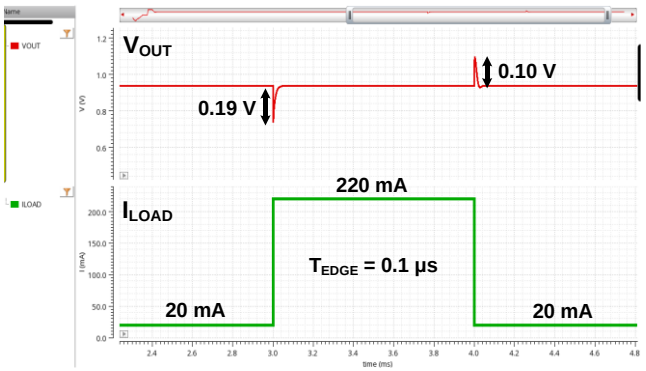


Fig. 11. Simulated load transient response.

cell size is 0.013 mm$^2$. A 1µF output capacitor is employed to mitigate a large voltage droop caused by heavy load currents.

Since the proposed architecture is designed to drive a large load current, the dominant pole is located at the gate of $M_{PWR}$, ensuring stable operation at high load currents. Meanwhile, a phase margin (PM) above 45 degrees is achieved for load currents greater than 4.7 mA.

Fig. 8 and Fig. 9 show the simulated temperature variations of the PTAT voltage $V_{PTAT}$ and the CTAT voltage $V_{CTAT}$ respectively, over a range from −60 °C to +120 °C. The generated PTAT voltage, generated by $I_{PTAT}$ and $R_{FB}$, exhibits the temperature coefficient of 327 ppm/°C. On the other hand, the generated CTAT voltage, combined with $V_{GS,NA}$ and $V_{GS,BOOST}$, exhibits the temperature coefficient of -350 ppm/°C. Adequate TC compensation can be achieved by tuning the values of $I_{PTAT}$ and $R_{FB}$, while still maintaining nominal output voltage level. As shown in Fig. 10, the temperature coefficient of the total output voltage of the proposed architecture shows 218 ppm/°C.

Fig. 11 shows the simulated load transient response. The load current changes 20 mA to 220 mA and vice versa with a slew rate of 0.1us rise/fall time. The overshoot and undershoot voltages are 0.19 V and 0.10 V, respectively. The proposed design is capable of maintaining a stable output

voltage while driving load currents up to 220 mA. The current density is 1.97 A/mm², which indicates a compact design compared to previous works. The peak current efficiency of the proposed work is 99.99 % due to the quiescent current of 9 μA. The total chip area is 0.1115 mm$^2$. Table I summarizes the performance metrics of the proposed embedded-voltage reference LDO with a comparison to prior papers.

## IV. CONCLUSION

This proposed EVR LDO comprises the PTAT generator, EVR EA, and power MOSFET. In proposed EVR EA, the boost MOSFET supports shifting output voltage level from low voltage to nominal voltage level without TC performance and output stability degradations. The proposed LDO can obtain the maximum current density of 1.97 A/mm$^2$ and the peak current efficiency of 99.99% including the voltage reference with a TC of 218 ppm/°C. The proposed EVR LDO is expected to supply high power due to nominal voltage level and high current driving capability. These advantages of the proposed EVR LDO are suitable for SoC architectures which demand high performance.

## ACKNOWLEDGMENT

The chip fabrication and EDA tools were supported by the IC Design Education Center (IDEC), Korea. This work was supported by Korea Planning & Evaluation Institute (KEIT) grand funded by the Korea Government (MOTIE) (RS-2024-00404313).

## REFERENCES

[1] Y.-S. Yuk, S. Jung, C. Kim, H.-D. Gwon, S. Choi, and G.-H. Cho, “PSR Enhancement Through Super Gain Boosting and Differential Feed-Forward Noise Cancellation in a 65-nm CMOS LDO Regulator,” IEEE Trans. VLSI Syst., vol. 22, no. 10, pp. 2181–2191, Oct. 2014.

[2] D.-K. Kim, S.-U. Shin, and H.-S. Kim, “A BGR-Recursive Low-Dropout Regulator Achieving High PSR in the Low- to Mid-Frequency Range,” IEEE Trans. Power Electron., vol. 35, no. 12, pp. 13441–13454, Dec. 2020.

[3] A. A. Khan and R. K. Palani, "Analysis and Design of Low Noise Voltage Regulator with Integrated Single BJT Bandgap Reference Up to 10 mA Loads," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 6, pp. 2966-2970, June 2024.

[4] Z. Zhang, C. Zhan, L. Wang, and M.-K. Law, “A − 40°C–125 °C 0.4-μA Low-Noise Bandgap Voltage Reference With 0.8-mA Load Driving Capability Using Shared Feedback Resistors,” IEEE Trans. Circuits Syst. II, vol. 69, no. 10, pp. 4033–4037, Oct. 2022.

[5] W.-C. Chen, Y.-P. Su, Y.-H. Lee, C.-L. Wey, and K.-H. Chen, “0.65V-Input-Voltage 0.6V-Output-Voltage 30ppm/°C Low-Dropout Regulator with Embedded Voltage Reference for Low-Power Biomedical Systems,” in 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, USA: IEEE, pp. 304–305, Feb. 2014.

[6] I. Bhattacharjee and G. Chowdary, “A 0.45 mV/V Line Regulation, 0.6 V Output Voltage, Reference-Integrated, Error Amplifier-Less LDO With a 5-Transistor Regulation Core,” IEEE J. Solid-State Circuits, vol. 58, no. 11, pp. 3231–3241, Nov. 2023.

**Beomsoo Kim** received the B.S. in electronics engineering from Pusan National University, Pusan, South Korea, in 2023. He is currently pursuing the M.S. degree at Sungkyunkwan University, Suwon, Republic of Korea. His research interests include power management ICs, DC–DC converters and Linear Dropout Output regulator.

**Yuli Han** received the B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, South Korea, in 2022 and 2025, respectively. She is currently an IC Design Engineer with DB Global Chip, South Korea. Her research interests include Linear Dropout Output regulator and power management ICs.

**Chanjung Park** received the B.S. and M.S. degrees in electronics engineering from Kyungpook National University, Daegu, South Korea, in 2022 and 2025, respectively. He is currently pursuing a Ph.D. degree at Sungkyunkwan University, Suwon, Republic of Korea. His research interests include power management ICs, DC–DC converters and AC-DC converters.

**Byungjae Kwag** received the B.S. degree in electrical engineering from Hanyang University, Ansan, South Korea, in 2025. He is currently pursuing the M.S.-Ph.D. program degree at Sungkyunkwan University, Suwon, Republic of Korea. His research interests include power management ICs, and Linear Dropout Output regulator.

**Minwoo Kim** is currently pursuing a B.S. degree in electronics engineering from Kyungpook National University, Daegu, Republic of Korea. He is scheduled to begin an integrated M.S.-Ph.D. program at Sungkyunkwan University in Suwon, South Korea, in the latter half of 2025. His research interests include analog integrated circuit design for power management ICs.

**Sangbin Tae** is currently pursuing a B.S. degree in electronics engineering from Sungkyunkwan University, Suwon, Republic of Korea. He is scheduled to begin an integrated M.S.-Ph.D. program at Sungkyunkwan University in Suwon, South Korea, in the latter half of 2025. His research interests include analog integrated circuit design for power management ICs.

**Kunhee Cho** received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2007 and 2009, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Texas at Austin, Austin, TX, USA, in 2016.
From 2009 to 2012, he was with Fairchild Semiconductor, Bucheon, South Korea, where he designed power management integrated circuits (ICs). In 2015 and 2016, he was a Graduate Research Intern with Texas Instruments Incorporated, Dallas, TX, USA, in the low-power RF team. From 2017 to 2020, he was with Qualcomm Technologies Incorporated, Santa Clara, CA, USA, where he designed power management ICs for battery charger systems. From 2020 to 2025, he was an Associate Professor with Kyungpook National University, Daegu, South Korea. In 2025, he joined Sungkyunkwan University, Suwon, South Korea. His research interests include power management ICs, high-voltage gate drivers, class-D amplifiers, and RF power amplifiers. Dr. Cho was a recipient of the Texas Instruments Outstanding Student Design Award in 2013.