Design of a High-Gain Low-Power K-Band Mixer in 65-nm Bulk CMOS Technology

Joon-Hyuk Yoon[1], Hyeon-Wook Kang[2], Ji-Ho Yoo[3], Ui-Gyu Choi[*,a], and Jong-Ryul Yang[b]
Department of Electrical and Electronics Engineering, Konkuk University, Seoul, South Korea.
*Microwave Technology Development Division, LIGNex1, Yongin, South Korea.
E-mail : [1]yoonkevin@konkuk.ac.kr, [2]hyeonwook0817@konkuk.ac.kr, [3]jhy0502@konkuk.ac.kr

***Abstract* – This paper presents a single-balanced down-conversion mixer for K-band applications requiring high conversion gain and compact integration. The proposed design incorporates gate inductive peaking at the RF transconductance stage to enhance the effective transconductance while simultaneously achieving input impedance matching. To address the limitations of conventional designs that require high LO drive levels, a transformer-based structure is introduced at the LO port, enabling differential LO injection and improved LO power efficiency. This configuration provides sufficient LO swing at the switching core without increasing power consumption or circuit complexity. The mixer is implemented in a 65-nm bulk CMOS process and occupies an area of 0.36 mm², including probing pads. Measurement results show impedance matching around 24 GHz for both LO and RF ports, along with an RF-to-LO isolation greater than 22 dB. The simulated conversion gain is 5.1 dB with a 5 dBm LO drive, an input 1-dB compression point of –18 dBm, and a noise figure of 15 dB at 24 GHz.**

***Keywords*—CMOS, down-conversion mixer, high conversion gain, K-band, single-balanced**

I. INTRODUCTION

K-band, covering frequencies roughly from 18 to 27 GHz, plays a crucial role in emerging wireless technologies due to its capability to support high data rates and wide bandwidths [1], [2]. Key applications include automotive radar, 5G millimeter-wave communications, satellite links, and high-resolution imaging systems [3], [4], [5], [6]. The short wavelength at these frequencies enables compact and highly integrated circuit designs, making K-band well-suited for system-on-chip (SoC) solutions using silicon-based processes.

Down-conversion mixers are essential components in K-band receivers, converting high-frequency RF signals to lower intermediate frequency (IF) or baseband signals suitable for digital processing [7], [8], [9], [10]. Mixer performance critically affects overall receiver gain, noise figure (NF), and linearity. Conversion gain determines the level of signal amplification before subsequent stages. Elevated conversion gain suppresses thermal and flicker noise impacts, improving signal-to-noise ratio (SNR) and receiver sensitivity.

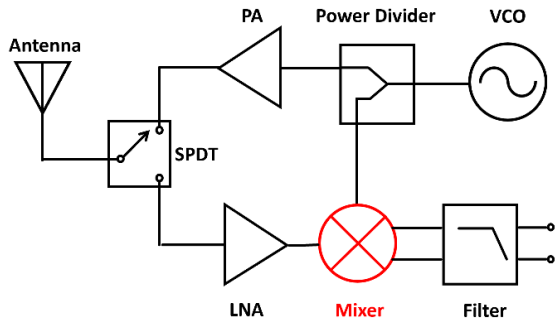

Fig. 1. Down-conversion mixer used in K-band radar system.

Designing mixers with high gain in the K-band presents challenges, especially in bulk CMOS technology. Despite advantages in integration and cost-effective mass production, CMOS suffers from reduced gain at high frequencies due to low-quality passive components and higher substrate losses. Conventional mixers often require high local oscillator (LO) drive levels or multi-stage amplification to offset these issues, increasing power consumption and complexity [11], [12], [13], [14].

In this paper, a single-balanced K-band down-conversion mixer utilizing gate inductive peaking technique is proposed to improve conversion gain while maintaining input impedance matching [15], [16]. Gate inductive peaking enhances the RF-stage transconductance (Gm) by placing a series inductor at the input of the transistor gate node, resonating out the parasitic gate-source capacitance (C_{gs}) and increasing effective Gm across the operating bandwidth. A transformer is employed at the LO port, which enables differential LO injections, enhancing LO drive efficiency. The proposed mixer is fabricated in 65-nm bulk CMOS technology with a chip area of 0.36 mm². The measurement results demonstrate a return loss of under –10 dB from 24 GHz to 26.5 GHz.

Section II describes the detailed design methodology of the proposed K-band mixer. Section III presents the chip layout and implementation. Section IV shows the measurement

a. Co-corresponding author; uigyu.choi@lignex1.com
b. Corresponding author; jryang@konkuk.ac.kr

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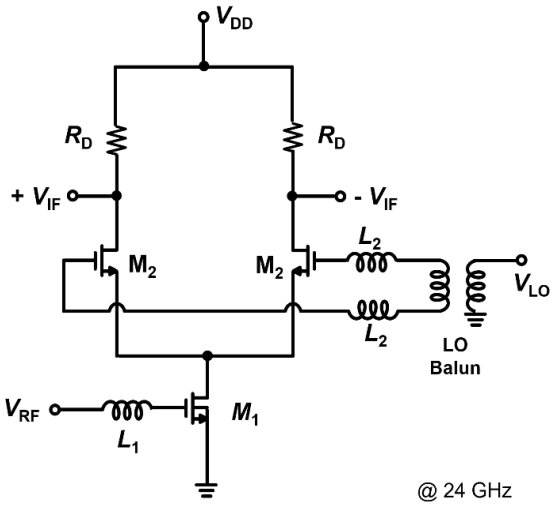

V_{DD}	M_1	M_2	L_1	L_2	R_D
1.2 V	28 μm	117 μm	1.1 nH	0.3 nH	100 Ω

Fig. 2. Schematic diagram of the proposed K-band mixer.

results, including S-parameter, conversion gain, and linearity performance, including a performance comparison with previous works in the literature. Section V concludes the paper.

II. DESIGN METHODOLOGY OF THE K-BAND MIXER

A conceptual block diagram of a K-band radar transceiver system is illustrated in Fig. 1. In the receiver architecture, the down-conversion mixer plays a critical role in translating the incoming RF signal to a lower IF signal, where subsequent amplification and baseband processing are performed. The performance of the mixer has a direct impact on the overall system's performance and reliability. Therefore, a high conversion gain with low power operation is essential for ensuring adequate sensitivity, especially in K-band applications where thermal noise and substrate losses are more pronounced due to the high operating frequency.

A single-balanced topology-based down-conversion mixer with inductive peaking at the RF input is proposed, as shown in Fig. 2. The proposed mixer consists of an RF transconductance stage, followed by a switching core driven by the LO signal, and differential load resistors at the IF output. The input RF signal is applied to a common-source (CS) NMOS transistor that converts the voltage input into a current signal. The current is then steered by the LO-driven differential pair, effectively performing the frequency translation. The single-balanced configuration provides a good compromise between gain, design complexity, and area efficiency, while also facilitating easier LO drive compared to fully differential double-balanced mixers. As illustrated in Fig. 2, the transistor dimensions are carefully chosen to achieve sufficient transconductance while maintaining low parasitic capacitance, thereby ensuring wideband RF performance and stable LO switching operation.

A gate inductive peaking technique is employed at the input transistor to enhance the performance of the Gm stage. Fig. 3 depicts the circuit and small signal equivalent model

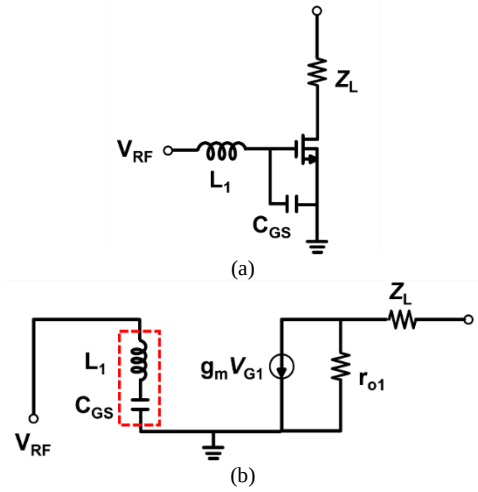

Fig. 3. RF input stage using gate inductive peaking technique: (a) circuit model, (b) equivalent small signal circuit model.

of the CS stage transistor when the inductive peaking technique is applied. The method involves designing a high-Q inductor in series with the gate of the RF transistor. The inductor, in conjunction with the parasitic C_{gs}, forms a resonant LC network which is tuned to the operating frequency. The resonance effectively cancels the capacitive loading of C_{gs}, leading to a sharper impedance peak at the input node. The gain enhancement directly improves the overall conversion gain of the mixer without increasing the power consumption of the circuit. The inductive peaking technique can be verified through the input impedance and voltage equations. The input impedance at the gate node can be derived as:

$$Z_{in} = jw_0 L_1 + \frac{1}{jw_0 C_{GS}} \tag{1}$$

where a resonant response is shown at w_0. Then the input voltage at the gate node can be characterized as follows, depending on the use of the inductor L_1.

$$V_{in} = V_{RF} \cdot \frac{1}{1 + jw_0 C_{GS} Z_{source}} \tag{2}$$

$$V_{in} = V_{RF} \cdot \frac{1}{1 + w_0^2 L_1 C_{GS}} . \tag{3}$$

Eq. (3) induces a resonance response, which effectively eliminates the denominator and maximizes the input voltage. The maximized input swing leads to Gm boosting, which increases the overall conversion gain.

Transistor sizing and biasing are also critical in optimizing the performance of both the transconductance stage and the LO switching core. For the RF transistor, a large width can maximize the Gm characteristics but lead to a larger C_{GS} value. With the use of the gate inductor, the C_{GS} must remain within the range that can be effectively tuned out. A total width of 28 μm was chosen for an optimal balance between the trade-offs.

The LO switching pair is designed to balance between switching speed and LO drive requirements. Excessively

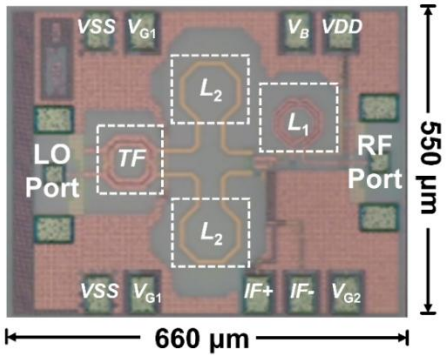

Fig. 4. Die photograph of the proposed K-band mixer.

large devices tend to increase parasitic capacitance and degrade RF-to-LO isolation, while smaller devices may not switch effectively at K-band frequencies. A total width of 117 µm is adopted in the design to ensure the switching operation. The LO core is biased to 0.5 V, which is near the threshold region to minimize DC power consumption while maintaining adequate switching behavior under a modest LO swing. The use of a transformer at the LO port enables differential injection with enhanced swing at the gates of the switching pair, further assisting in full-switching operation without requiring large LO power.

III. CHIP LAYOUT AND IMPLEMENTATION

The proposed mixer is implemented with a 65-nm bulk CMOS process. The total layout area, including all RF and bias pads, is 0.55 mm × 0.66 mm, with an active core circuit area of 0.19 mm². Fig. 4 shows the chip micrograph, highlighting the core mixer blocks and external pad arrangement. A ground-signal-ground (GSG) configuration is used for the RF and LO ports to facilitate high-frequency on-wafer probing.

Symmetrical layout practices are applied to maintain balanced signal paths and minimize phase mismatch. The transformer designed at the LO switching core is placed to ensure minimal parasitic coupling and consistent routing lengths between the differential paths. Bias lines and decoupling capacitors are placed close to each transistor to minimize noise injection.

Passive components such as the gate inductor and LO transformer are thoroughly designed using 3D full-wave electromagnetic (EM) simulation. The inductor is optimized for resonance near 24 GHz with the C_{gs} element of the Gm stage transistor. The LO transformer is configured to provide differential LO injections with minimal imbalance and insertion loss. Layout-extracted parasitics are included in the final circuit co-simulation to ensure accurate prediction of the performance metrics.

IV. RESULTS AND DISCUSSIONS

On-wafer measurements are conducted using GSG probes for both the RF and LO ports. A Model 40A probe from GGB Industries Inc. is used throughout the setup. Small-signal characterization is performed using a Keysight N5222B network analyzer configured for S-parameter measurements. Short-open-load-thru (SOLT) calibration is applied on an impedance standard substrate (ISS) up to the probe tips to ensure accurate de-embedding of all transmission and reflection losses.

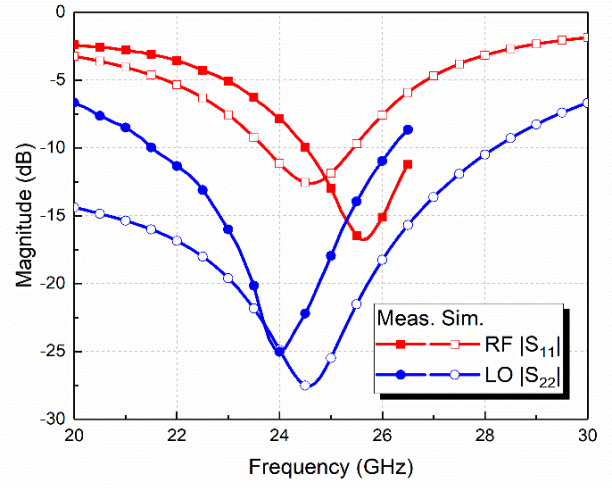

Fig. 5. Reflection coefficients of the RF and LO ports.

Due to the frequency limitations of the available spectrum analyzer, direct measurement of conversion gain and output power could not be performed. Instead, co-simulation results combining circuit-level and 3D electromagnetic (EM) models are utilized. The passive structures, including the gate inductor and LO transformer, were rigorously modeled using full-wave EM simulation, and the extracted models were integrated into the circuit simulation. As shown in the measured S-parameter results, key RF characteristics such as input matching and return loss closely align with the simulation, validating the accuracy of the EM co-simulation approach. Therefore, the simulated conversion gain and power response are considered reliable substitutes in evaluating the performance of the proposed mixer.

Fig. 5 shows the measured input reflection coefficients of the RF and LO ports when the RF port is considered port 1 and the LO port is considered port 2. Both ports exhibit return loss better than −10 dB near the operating frequency of 24 GHz, indicating effective impedance matching. These results are consistent with the EM circuit co-simulation and confirm the functionality of the gate inductive peaking and transformer-based input network. In particular, the LO port exhibits a matching bandwidth wider than 2 GHz around 24 GHz, which ensures robust performance even under process and packaging, validating that the proposed transformer network provides sufficient performance. Although the measured RF frequency response is shifted upward compared with the simulation, the downward shift expected from loading effects indicates that the results remain well aligned with practical K-band radar system requirements.

Fig. 6 presents the measured RF-to-LO isolation. The isolation level remains better than 22 dB across the intended operating range, which indicates that the physical layout effectively suppresses undesired coupling between LO and RF paths. The measured isolation is sufficient to prevent LO leakage from degrading the linearity or the noise performance of the overall K-band receiver. Compared with

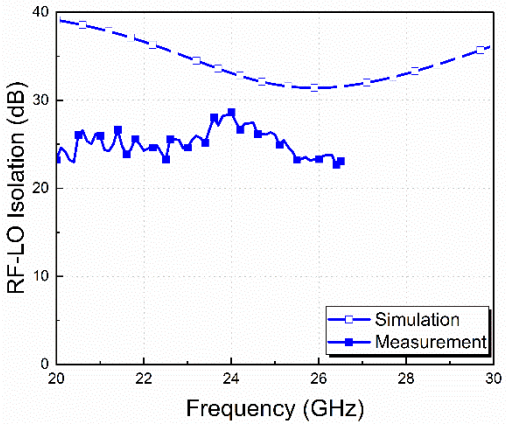

Fig. 6. Simulated and measured results of isolation between RF and LO ports.

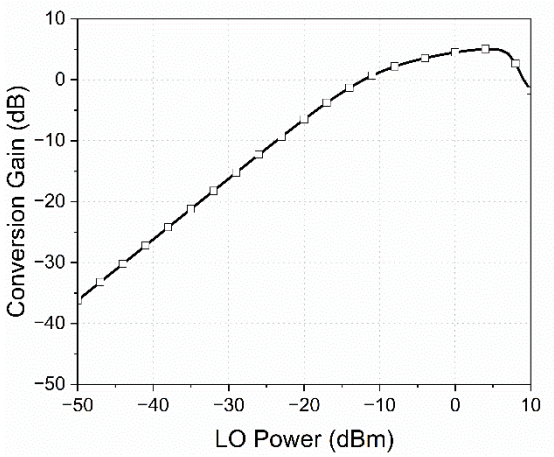

Fig. 7. Simulated conversion gain as a function of the LO power.

conventional single-balanced mixers, where isolation often falls below 15 dB, the achieved isolation demonstrates the effectiveness of the port separation and on-chip shielding strategy. This performance confirms that the proposed design is well-suited for integration into multi-stage receiver chains where LO leakage can otherwise accumulate and deteriorate overall system sensitivity.

The simulated conversion gain under varying LO input powers is shown in Fig. 7. A peak conversion gain of 5.1 dB is observed at 10 MHz IF with an LO power of 5 dBm. The observed gain behavior is consistent with the expected Gm enhancement from the inductive peaking at the RF input and with proper input impedance matching. At lower LO drive levels below 0 dBm, insufficient switching activity reduces the effective transconductance, whereas excessive LO drive above 7 dBm leads to overdriving of the switching pair, resulting in degraded gain and potential linearity penalties. These results highlight that an LO drive of approximately 5 dBm provides the optimal trade-off between conversion efficiency and linearity for the proposed topology.

Fig. 8 illustrates the simulated conversion gain (CG) and the noise figure (NF) as functions of RF frequency over 20–30 GHz when the LO frequency is fixed at 24 GHz with an LO drive of 5 dBm. The CG exhibits a bandpass-like response, peaking at the LO frequency of 24 GHz with a maximum value of 5.3 dB and gradually rolling off on either

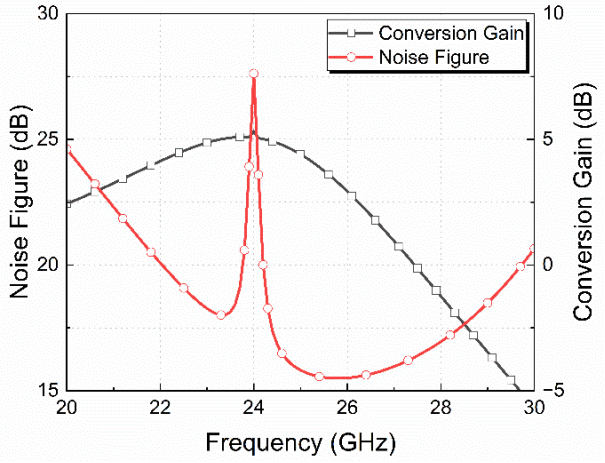

Fig. 8. Simulated conversion gain and noise figure as a function of the RF frequency.

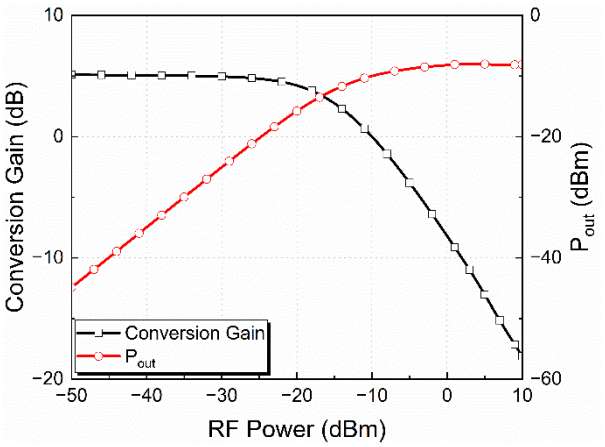

Fig. 9. Simulated conversion gain and output power as a function of the RF power.

side of the peak. This RF frequency response with a fixed LO arises from the combined effect of input impedance matching at the RF port and enhanced switching efficiency when the RF approaches the LO frequency. When the RF and LO frequencies coincide, the down-converted output collapses to DC and includes additional DC offsets, which is a characteristic of direct-conversion operation and should not be interpreted as a low-IF mixer result. The NF also shows a distinct frequency dependence. It decreases progressively, reaches a minimum near 26 GHz, and then increases again toward 30 GHz. A pronounced NF peak is observed at 24 GHz, where the RF coincides with the LO. This behavior indicates the dominance of flicker noise in the switching devices under direct-conversion conditions. Like the CG response, this phenomenon does not represent the performance of the mixer in the intended low-IF architecture. These results demonstrate that the proposed mixer achieves stable CG and low noise performance across the K-band under low-IF operation.

Fig. 9 displays the simulated input 1-dB compression point (P1dB) with a 5-dBm LO drive at 24 GHz. The proposed mixer achieves an ultra-low power consumption of 3.5 mW, while exhibiting a P1dB of −18 dBm, indicating that the circuit can tolerate moderate RF input levels without

TABLE I. Measurement Summary and Comparison of Performance

Reference	Process	Topology	Frequency (GHz)	CG (dB)	NF (dB)	LO Power (dBm)	OP1dB	P_{DC} (mW)	Area (mm^2)
[7]	65-nm	DBM	26.5 – 29.5	10.1	9.9	-7*	19.3	11/21*	0.18/0.28*
[8]	40-nm	DBM	24 – 40	1.2	15.3	N/A	6.8	28.3	0.65
[9]	65-nm	DBM	26 – 39	4.4	13.9	5	4	9.8	0.4
[10]	65-nm	DBM	26.5 – 29.5	11	8.9	-10*	13.5	13.7/23.8*	0.2/0.39*
[17]	22-nm FD-SOI	SBM	25 – 31	12	7 – 12	0	N/A	25	0.64
This work	65-nm	SBM	24 – 26.5	5.1†	15†	5†	-13†	3.5†	0.36

*including LO buffer, †simulation results

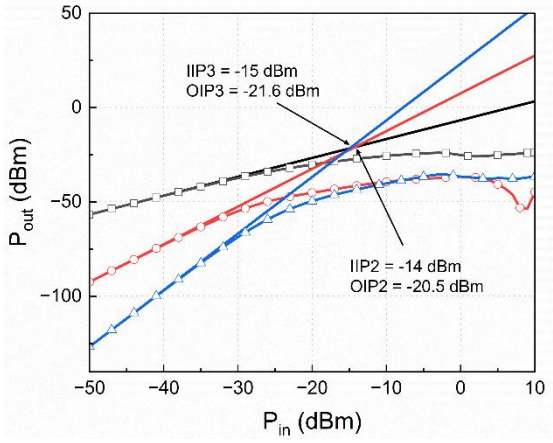

Fig. 10. Simulated IIP2 and IIP3 results demonstrating the linearity of the proposed mixer.

significant distortion. In terms of two-tone linearity, Fig. 10 presents the simulated input intercept points, where the simulated third-order input intercept point (IIP3) and the second-order input intercept point (IIP2) are –15 dBm and –14 dBm, respectively. The narrow margin between IIP2 and IIP3 reveals insufficient suppression of even-order distortion, mainly due to the single-ended RF input configuration, which inherently lacks common-mode rejection of second-order harmonics. Despite this limitation, the proposed mixer demonstrates competitive linearity relative to recently reported K-band CMOS designs, particularly when its extremely low power consumption is considered. These results confirm that the proposed mixer is well-suited for a low-power and wideband receiver front-end, where energy efficiency is as critical as linearity.

Table I summarizes the key performance metrics of the proposed mixer and compares them with recently published CMOS-based K-band down-conversion mixers. This represents the lowest power consumption among comparable CMOS implementations. Power efficiency is achieved without the use of additional LO buffering circuits. The proposed design achieves a peak conversion gain of 5.1 dB while consuming only 3.5 mW from a 1.2 V supply, which relies instead on a transformer-based LO injection that enables effective switching with minimal LO drive power. Despite employing a single-balanced topology, which generally provides lower gain compared to double-balanced structures, the proposed mixer achieves competitive gain performance by utilizing gate inductive peaking that enhances the effective transconductance of the RF input stage. In addition to high gain and power efficiency, the compactness of the circuit is also a key advantage. The single-balanced structure simplifies the design and routing, contributing to a total active chip area of only 0.19 mm^2. The proposed design is significantly smaller than the typical double-balanced mixers, making the proposed design more suitable for area-constrained SoC implementations. Taken together, the proposed design achieves a favorable balance between performance and integration efficiency, validating its potential for use in low-power, high-frequency K-band receiver applications such as wireless communication and radar systems.

V. CONCLUSIONS

A K-band single-balanced down-conversion mixer has been proposed, aiming for high conversion gain, low power consumption, and compact chip integration suitable for advanced millimeter-wave systems. The design incorporates a gate inductive peaking technique at the RF input stage, which enhances the effective transconductance by alleviating parasitic capacitances without additional bias overhead, thereby improving gain efficiency under low-power operation. Furthermore, a transformer-based differential LO injection is employed to drive the switching stage effectively, reducing LO power requirements while enhancing RF-to-LO isolation. Fabricated in a 65-nm CMOS process, the mixer demonstrates adequate impedance matching, robust RF-to-LO isolation, and competitive linearity performance verified through both electromagnetic and circuit-level simulations. These results validate the effectiveness of the proposed design methodologies and confirm the suitability of the mixer for incorporation into a low-power K-band receiver front-end, where energy efficiency and integration are as critical as linearity.

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Joon-Hyuk Yoon received the B.S. degree in Electronic Engineering from Yeungnam University, Gyeongsan, Korea, in 2023 and is pursuing his M.S. in Electronics, Information and Communication Engineering in Konkuk University, Seoul, Korea.

His research interest includes millimeter-wave CMOS circuits, especially Dicke and SPnT switches.

Hyeon-Wook Kang received the B.S. degree in Mechanical & Electronic Engineering from Konkuk University, Chungju, Korea, in 2025. He is pursuing the integrated M.S. and Ph.D. degrees in Electrical and Electronics Engineering in Konkuk University, Seoul, Korea.

His research interest includes millimeter-wave CMOS IC design, especially frequency conversion circuits.

Ji-Ho Yoo received the B.S. degree in Electronic Engineering from Dong-A University, Busan, Korea, in 2024. He is pursuing the integrated M.S. and Ph. D. degrees in Electrical and Electronics Engineering in Konkuk University, Seoul, Korea.

His research interest includes millimeter-wave CMOS IC design, especially signal generators.

Ui-Gyu Choi received the B.S. and M.S. degrees in Electronic Engineering from Yeungnam University, Gyeongsan, Korea, in 2018 and 2020, respectively, and a Ph.D. in Electronic Information and Communication Engineering from Konkuk University, Seoul, Korea, in 2024. He was a Postdoctoral Fellow at the Department of Electrical and Electronics Engineering, Konkuk University, from Sep. 2024 to Dec. 2024. Since January 2025, he has been working as a Senior Engineer in the Microwave Technology Development Division, LIGNex1, Yongin, South Korea.

His research interests include millimeter-wave/terahertz circuits and systems, particularly front-end integrated circuits.

Jong-Ryul Yang received dual B.S. degrees in Electrical Engineering and Materials Science from Ajou University, Suwon, South Korea, in 2003 and a Ph.D. degree in Electrical Engineering and Computer Science from Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2009. From Feb. 2009 to Oct. 2011, he worked as a Senior Engineer in the System LSI Division, Samsung Electronics, Yongin, South Korea. From Nov. 2011 to Aug. 2016, he was a Senior Researcher in the Advanced Medical Device Research Division, Korea Electrotechnology Research Institute, Ansan, South Korea. From Sep. 2016 to Feb. 2023, he was an Associate Professor in the Department of Electronic Engineering, Yeungnam University, Gyeongsan, South Korea. Since Mar. 2023, he has been an Associate Professor in the Department of Electrical and Electronics Engineering, Konkuk University, Seoul, South Korea. He is a Senior Member of IEEE, a Lifetime Member of KIEES, KICS, KIEE, and IEIE.

His research interests include RF/millimeter-wave /terahertz-wave circuits and systems, specifically CMOS front-end ICs, sub-terahertz imaging systems, and miniaturized radar sensors for vital signal detection and smart space monitoring for spatial intelligence.