Implementation and Characterization of a Digital Phase-Locked Loop (DPLL) in 65-nm CMOS Technology

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***Abstract* - This paper presents an experimental study on the influence of digital loop filter (DLF) gains $K_{P,PLL}$ and $K_{I,PLL}$ on the dynamic and noise performance of a 65 nm CMOS digital phase-locked loop (DPLL). By varying $K_{P,PLL}$ and $K_{I,PLL}$ across a range of values, the resulting changes in loop bandwidth, lock time, phase noise, and output jitter were measured. Silicon prototype measurements demonstrate that increasing $K_{P,PLL}$ reduces lock time but may introduce peaking in the closed-loop response, whereas increasing $K_{I,PLL}$ enhances low-frequency phase error suppression at the expense of slower settling. Under optimal gain settings, silicon measurements show an output spur level as low as −68.80 dBc and an RMS jitter of 0.638 ps, confirming excellent noise and spur performance.**

***Keywords*—Phase-Locked Loop, Digital Loop Filter, Proportional gain, Integral gain**

I. INTRODUCTION

Phase-locked loops (PLLs) are indispensable circuit blocks for precise frequency synthesis and low-jitter clock generation in applications such as wireless transceivers, high-speed data converters, and SoC clock networks [1]. Traditional analog PLLs offer low phase noise and fast lock times, but are sensitive to process–voltage–temperature (PVT) variations and present integration challenges for analog filters and phase detectors [2]. In modern CMOS technologies, where digital logic density and speed have dramatically advanced, analog circuitry can become a bottleneck in terms of design complexity, area, and power consumption.

Digital PLLs (DPLLs) overcome these limitations by implementing phase detection, loop filtering, and frequency control entirely in the digital domain [3], [4]. A fully digital implementation ensures robust process portability across various CMOS nodes, supports automated digital design flows (e.g., RTL-to-GDSII), and simplifies system-level integration with other digital blocks. Moreover, programmable digital loop filters (DLFs) allow designers to adjust proportional and integral gain parameters in real time, facilitating on-chip optimization of lock time, phase-noise floor, and spur behavior without custom analog design iterations. Nonetheless, DLF-based architectures introduce quantization noise, switching artifacts, and clock-to-output timing constraints, complicating the trade-off between noise-shaping performance and critical-path delay. Selecting the appropriate DLF coefficient resolution is critical: longer word lengths improve noise shaping but increase logic depth, while higher target frequencies require aggressive timing closure and stricter noise-shaping to meet modern communication standards.

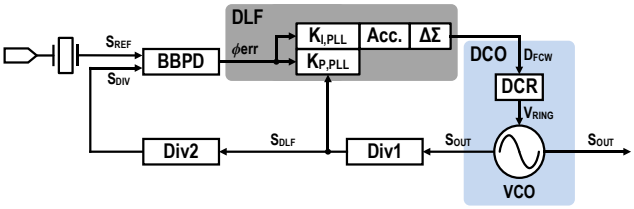

Fig. 1. Block Diagram of a Conventional Digital PLL

This paper focuses on the internal DLF gain parameters of a digital PLL implemented in a 65 nm CMOS process, analyzing how the proportional gain $K_{P,PLL}$ and integral gain $K_{I,PLL}$ affect its dynamic and spectral characteristics. The specific contribution of this work is not in proposing a new circuit architecture, but in providing a detailed characterization that quantitatively links the simulated autocorrelation of the internal phase error signal (Fig. 6) to the externally measured phase noise and spur performance (Fig. 9). This analytical approach offers a practical and intuitive methodology for optimizing DLF gains in deep-submicron DPLLs, bridging the gap between theoretical loop dynamics and practical silicon performance [5]. Section II presents simulations targeting the DLF gains and analyzes their results. Section III presents the silicon measurement setup and actual measurement results to validate performance. Finally, Section IV concludes the paper.

II. DIGITAL PLL DESIGN AND ANALYSIS

A. *Operating Principle of the Digital PLL*

Fig. 1 shows the block diagram of the implemented digital PLL [1], [3], [4]. The reference clock (S_{REF}) serves as the external input to the PLL, is supplied at a lower frequency

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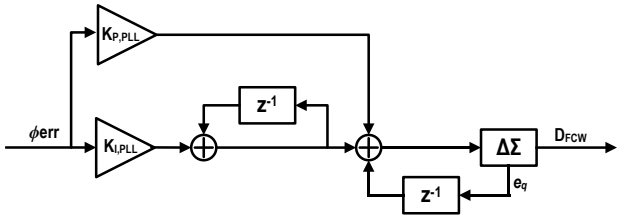


Fig. 2. DLF Architecture Proportional–Integral Paths and ΔΣ Quantizer

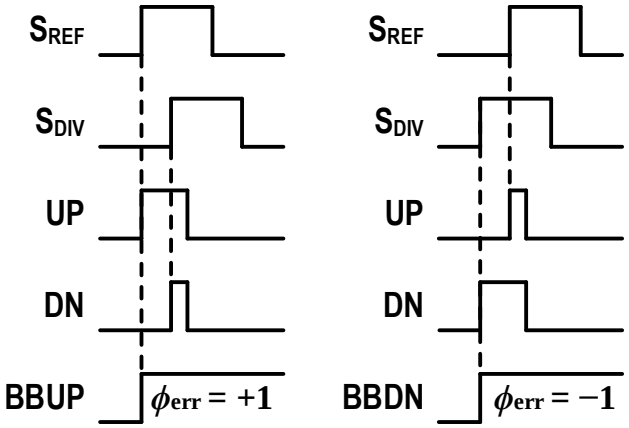


Fig. 3. Timing diagram illustrating the BBPD operation

than the digitally controlled oscillator (DCO) output (S_{OUT}), and originates from a clean, low-noise source. Both S_{REF} and the feedback clock (S_{DIV}) are fed into a bang-bang phase detector (BBPD). The BBPD compares their phases and produces two single-bit outputs, BBUP and BBDN, indicating whether S_{DIV} leads or lags S_{REF}.

The BBPD outputs are subsequently passed to the DLF. Synchronized to the rising edge of the Div1-derived clock (S_{DLF}), the DLF samples BBUP and BBDN on every rising edge and converts them into a digital phase error signal (ϕ_{err}).

Fig. 2 shows the detailed block diagram of the proposed DLF, which implements a proportional-and-integral loop filter. The DLF has two paths: the proportional path applies the current phase error (ϕ_{err}) scaled by the proportional gain ($K_{P,PLL}$) to provide fast phase correction, and the integral path accumulates the phase error scaled by the integral gain ($K_{I,PLL}$) to remove steady-state frequency offset. The two paths are summed and the resulting control value is mapped to the DCO through a delta–sigma (DSM) block. Because this mapping converts a high-resolution control value into a finite-resolution digital frequency control word (D_{FCW}), quantization error would otherwise appear in-band and degrade phase-noise performance. The DSM mitigates this by noise-shaping the error so that most of its power is pushed out of band. The resulting D_{FCW} drives the DCO to precisely control its output frequency, keeping the loop phase- and frequency-locked to the reference clock.

B. Analysis of Digital Loop Filter Gains

As illustrated in Fig. 3, the BBPD operates as follows: the rising edge of the reference clock (S_{REF}) sets the UP signal high, and the rising edge of the divided clock (S_{DIV}) sets the DN signal high [6]. Once both UP and DN signals are high, an internal reset is triggered after a fixed delay,

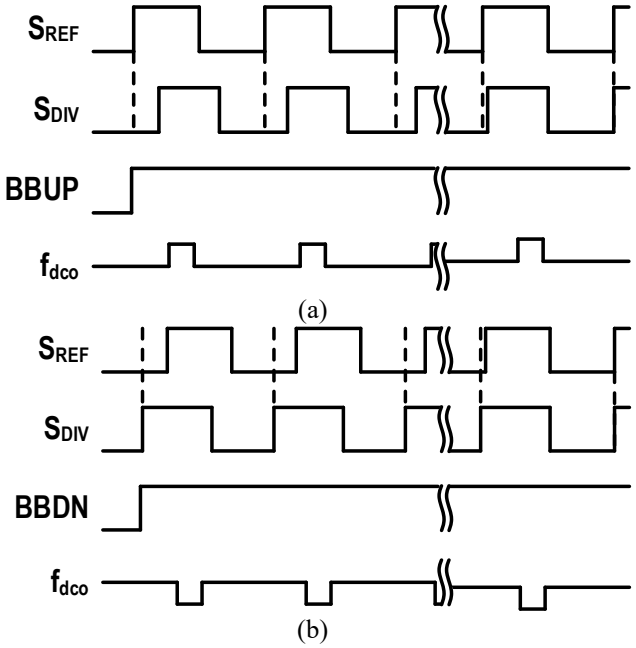


Fig. 4. Timing diagrams illustrating BBPD-based phase locking: (a) BBUP dominant (S_{REF} leads S_{DIV}), (b) BBDN dominant (S_{REF} lags S_{DIV})

simultaneously pulling both signals low. The operational principles and modeling of such bang-bang phase detectors are analyzed in detail in [6], [7]. The BBPD outputs either the BBUP or BBDN signal depending on the relative timing of the UP and DN signals. Specifically, if only the UP signal is high, indicating that S_{DIV} lags behind S_{REF}, the BBUP signal is asserted high, resulting in a positive phase error ($\phi_{err} = +1$) in the DLF. Conversely, if only the DN signal is high, indicating that S_{DIV} leads S_{REF}, the BBDN signal is asserted high, representing a negative phase error ($\phi_{err} = -1$) in the DLF. In all other cases, the BBUP and BBDN signals retain their previous states.

Fig. 4(a) illustrates the phase alignment process when the reference clock (S_{REF}) leads the divided clock (S_{DIV}), corresponding to the BBUP-dominant case. The BBPD continuously outputs a positive phase error signal (BBUP), indicating that S_{DIV} is lagging behind S_{REF}. The DLF processes this error ($\phi_{err} = +1$) by using the proportional gain ($K_{P,PLL}$) to momentarily increase the DCO frequency (f_{DCO}), thereby advancing the rising edge of S_{DIV}. At the same time, the integral gain ($K_{I,PLL}$) accumulates the error over time and gradually raises the baseline frequency of the DCO. This process, through the delta-sigma modulator, generates an updated D_{FCW}, driving the DCO to achieve both rapid phase correction and long-term frequency accuracy.

Fig. 4(b) shows the case where the divided clock (S_{DIV}) leads the reference clock (S_{REF}), corresponding to the BBDN-dominant scenario. The BBPD outputs a negative phase error signal (BBDN, $\phi_{err} = -1$), and the DLF uses $K_{P,PLL}$ to immediately decrease the DCO frequency, delaying the rising edge of S_{DIV}. The $K_{I,PLL}$ term reflects the accumulated negative error, systematically lowering the DCO's baseline frequency. This mechanism corrects phase and frequency mismatches without excessive correction, ensuring loop stability.

The optimal selection of these DLF gains is critical to the stability and performance of the DPLL. Fig. 5 conceptually

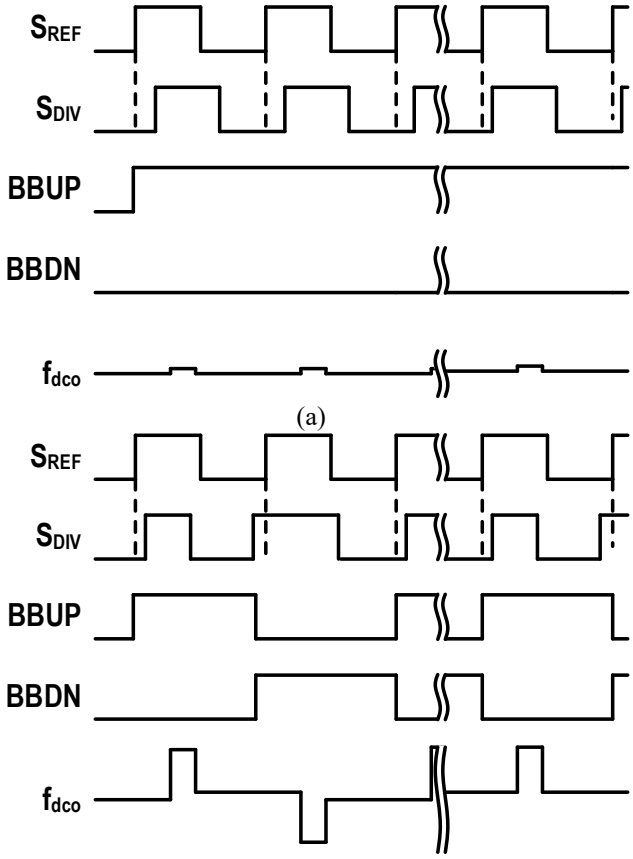


Fig. 5. Timing diagrams illustrating DPLL signals under (a) low gain and (b) high gain conditions.

illustrates the DPLL's behavior at the two extremes of the gain settings. In Fig. 5(a), when the loop gain is too low, the correction applied by the DLF is insufficient to overcome the phase error in a timely manner, leading to a very slow settling process or even a failure to achieve phase lock. Conversely, Fig. 5(b) depicts the case where the loop gain is excessively high. The DLF applies an overly aggressive correction to the phase error, causing the loop to overshoot the lock point and resulting in the BBUP and BBDN signals rapidly alternating as the DCO frequency oscillates around the target. These contrasting scenarios highlight that a carefully optimized gain value is essential for achieving a fast and stable lock, which will be further analyzed in the following section.

The dual-gain structure—where $K_{P,PLL}$ governs transient response (rapid phase alignment) and $K_{I,PLL}$ ensures steady-state accuracy (frequency offset elimination)—enables the PLL to maintain stable lock under dynamic conditions. However, loop gain magnitude critically determines PLL stability: excessively high gains induce quantization noise leakage, elevating spurs and degrading phase noise, while insufficient gains prolong locking time and fail to suppress low-frequency noise. Since $K_{P,PLL}$ and $K_{I,PLL}$ directly control loop bandwidth and phase margin, their optimization is essential for simultaneous precise frequency tracking and rapid locking.

The statistical behavior of the phase error, represented by the BBUP (+1) and BBDN (−1) pulses seen in Fig. 5, can be used to quantify the loop's stability. Fig. 6 visualizes this

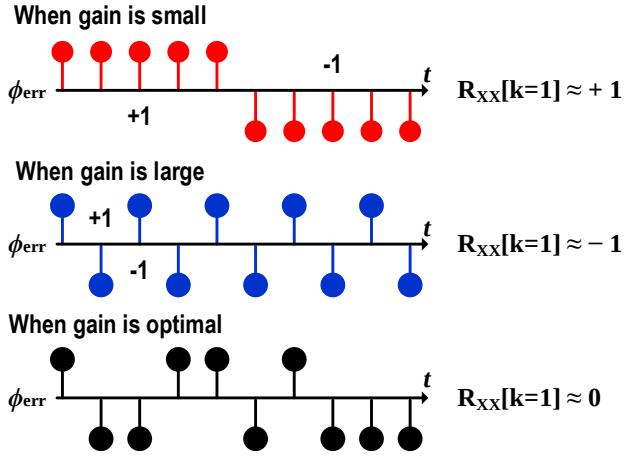


Fig. 6. Effect of DLF gain on the behavior of the phase error.

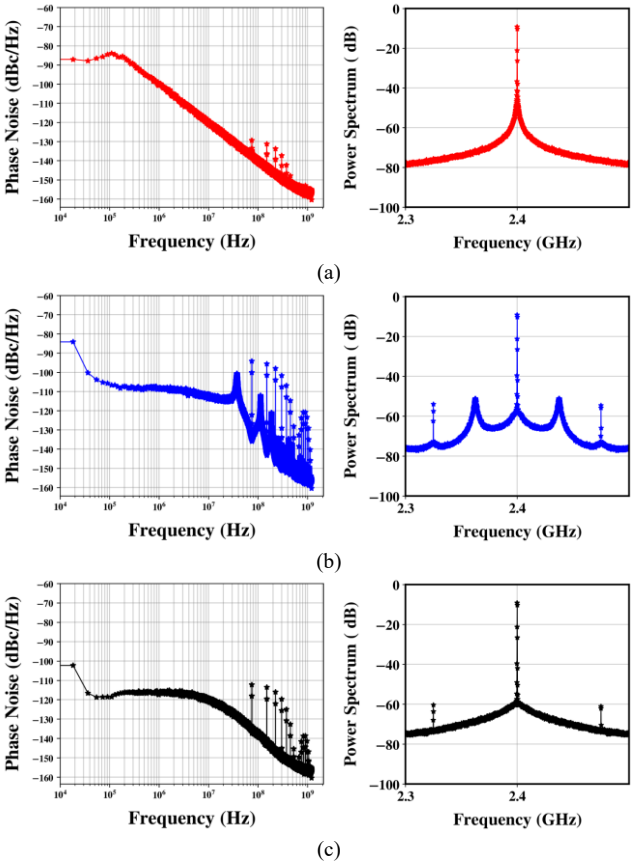


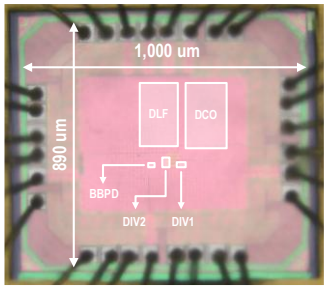
Fig. 7. Simulated phase noise and power spectrum comparison for various digital loop filter gains: (a) low gain, (b) high gain, (c) optimal gain.

dependency by plotting the simulated autocorrelation function of the phase error under three different gain settings. The autocorrelation function, $R_{XX}[k]$, measures the correlation of the phase error signal with a time-shifted version of itself by a lag of k, and is defined as:

$$R_{XX}[k] = \frac{1}{N}\sum_{n=0}^{N-1}(\phi_{err}[n] \times \phi_{err}[n+k]) \quad (1)$$

where k = 1 evaluates the correlation between adjacent samples. Applying this function to ϕ_{err} enables quantitative assessment of DLF gain suitability.

Fig. 6 visualizes the dynamic behavior of phase error (ϕ_{err}) and its autocorrelation characteristics under different DLF gain settings. This analysis, based on the autocorrelation method proposed in [8], provides a powerful tool for



Area & Power Breakdown			
Block		Area (mm²)	Power (mW)
DLF		0.0135	2.33
Analog	BBPD	0.001	3.18
	DIV1	0.001	
	DIV2	0.002	
DCO		0.0151	2.06
All		**0.0326**	**7.57**

Fig. 8. Chip microphotograph with area and power table.

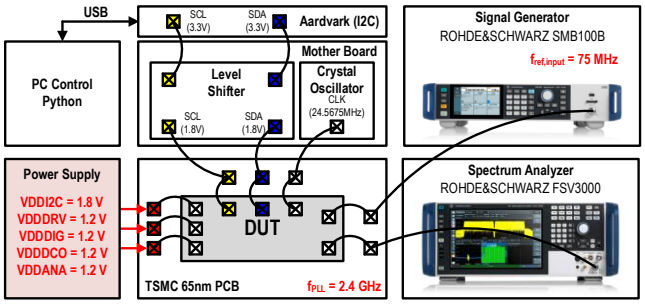


Fig. 9. Measurement setup.

diagnosing loop stability. Under low gain (red), the DLF's corrective steps are too small to promptly counteract the phase error. This allows the error to accumulate in one direction, maintaining a persistent polarity over many cycles. Such a persistent error is highly correlated with that of the preceding cycle, resulting in an autocorrelation value where RXX[k=1] is close to +1. This is a classic sign of insufficient correction due to a narrow loop bandwidth, as noted in [7].

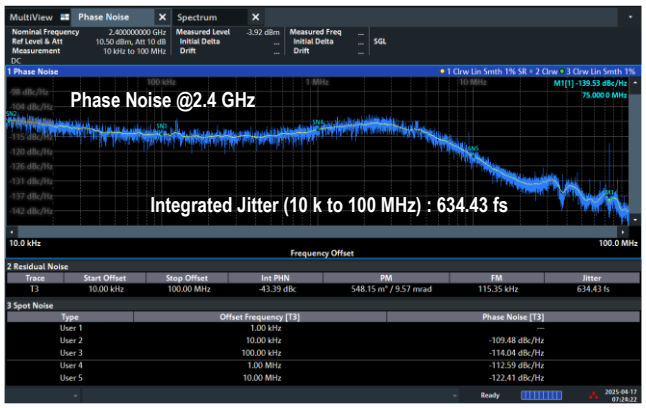
Conversely, with excessive gain (blue), the DLF applies an overly strong correction that causes the DCO to overshoot its target. This overshoot triggers an equally aggressive counter-correction on the next cycle, leading the loop to oscillate around the lock point. This periodic inversion of the error's polarity results in a strong negative correlation, causing the $R_{XX}[k=1]$ value to be near −1 and clearly indicating instability from overcorrection.

Finally, under optimal gain (black), the loop strikes a balance, effectively correcting the error without significant overshoot. The residual error thus becomes small and random, showing little correlation with its past values. Consequently, the $R_{XX}[k=1]$ value approaches 0, which confirms a stable lock condition and minimal residual noise.

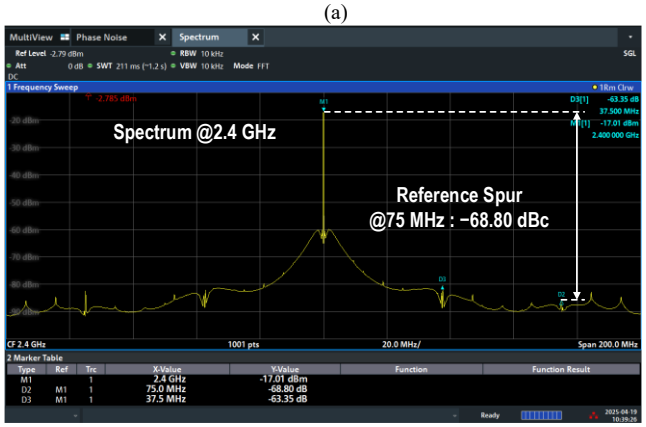
The loop stability analyzed in Fig. 6 directly impacts the phase noise and spur performance of the DPLL. Fig. 7 illustrates the simulated phase noise and output power spectra under three different DLF gain settings.

Under the low-gain condition (Fig. 7(a)), the phase error retains the same polarity for extended periods ($R_{XX}[k=1] \approx +1$). This indicates inadequate phase offset correction due to a narrow loop bandwidth, which in turn degrades the in-band phase noise suppression. In the output spectrum, this effect manifests as an elevated noise floor around the 2.4 GHz carrier frequency.

In contrast, under the high-gain condition (Fig. 7(b)), the phase error polarity alternates every cycle due to overcompensation ($R_{XX}[k=1] \approx -1$). These residual



(a)



(b)

Fig. 10. Measured (a) Phase Noise and (b) Spectrum of the PLL Output

oscillations leak quantization noise from the delta-sigma modulator into high-frequency bands, elevating spurs in the output spectrum and degrading the overall phase noise profile [9], [10].

The optimal-gain condition (Fig. 7(c)) exhibits randomized ±1 transitions in the phase error, with its autocorrelation approaching zero ($R_{XX}[k=1] \approx 0$). This indicates a stable lock condition where the loop corrects phase errors only when necessary. Such behavior minimizes residual noise while ensuring rapid convergence, significantly improving the measured phase noise and spur performance.

III. MEASUREMENT RESULTS

Fig. 8 presents the chip microphotograph and area and power breakdown analysis of the digital PLL fabricated in 65-nm CMOS technology. The overall die size is 1000 μm × 890 μm (0.89 mm²), while the active core occupies 0.0326 mm². To separate the contributions of the digital loop filter (DLF) and the digitally controlled oscillator (DCO), the bang-bang phase detector (BBPD) and both frequency dividers (DIV1, DIV2) are biased from the analog supply (AVDD) and thus grouped together as "analog blocks." All core power domains operate at 1.2 V, while the I²C interface runs at 1.8 V as shown in Fig. 9. The measured total power consumption is 7.57 mW with current consumption of 6.31 mA, distributed as follows: DLF = 2.33 mW (1.94 mA, 31%), analog blocks = 3.18 mW (2.65 mA, 42%), and DCO = 2.06 mW (1.72 mA, 27%). The active area breakdown

TABLE I. Performance Comparison Table.

	This work	[11] Wei '16	[12] Tierno '08	[13] Hamza '15	[14] Park '11
Technology (nm)	65 CMOS	40 CMOS	65 SOI	65 CMOS	65 CMOS
Architecture	BBPD-based	ΣΔ TDC-based	BBPD-based	TDC-based	TDC-based
Supply Voltage (V)	1.2	1.1	0.9	1.2	1.1
Core Area (mm²)	0.0326	0.0805	0.0300	0.0260	0.0352
f_{REF} (MHz)	75	31.25	250	100	N/A
f_{OUT} (GHz)	2.4	4.0	4.0	5.0	2.5
Power (mW)	7.57	3.51	17.2	5.4	13.7
RMS Jitter (ps)	0.634	0.861	0.700	1.59	3.2
Spur (dBc)	−68.80 (Ref.)	−70	N/A	N/A	N/A
FoM* (dB)	−235	−236	−230.8	−228.6	−222

FoM* (dB) = $20\log(\sigma_{rms})+10\log(P_{DC}/1mW)$

shows DLF occupying 0.0135 mm², analog blocks 0.004 mm², and DCO 0.0151 mm².

Fig. 9 shows the measurement setup used for the evaluation of the DUT. The DUT measurements were conducted using a Python-based control program on a PC through I^2C communication. The I^2C interface enables programmable configuration of the DLF gain parameters, allowing real-time optimization during testing. The final measurement results presented in this work are based on the optimal DLF gain settings that achieve the best performance in terms of phase noise and spurious suppression.

Fig. 10 presents the final measured performance of the DPLL under the optimally tuned DLF gain settings, validating the analysis presented in Section II.

The phase noise profile in Fig. 10(a) further highlights the success of the gain optimization. Within the loop bandwidth, where the loop is active, the phase noise is strongly suppressed, reaching an excellent value of −114.04 dBc/Hz at a 10 kHz offset. This demonstrates the loop's capability to clean up the DCO's intrinsic noise. Outside the loop bandwidth (e.g., above 1 MHz), the phase noise flattens out to −122.41 dBc/Hz at a 10 MHz offset, reflecting the inherent noise floor of the DCO itself.

The output spectrum in Fig. 10(b) is exceptionally clean, centered at the target frequency of 2.4 GHz. A key performance indicator, the reference spur at a 75 MHz offset, is suppressed to −68.80 dBc. This low spur level is a direct result of the optimized loop filter effectively attenuating reference feedthrough, which is a critical achievement for spectrally pure signal generation.

Ultimately, integrating this well-controlled phase noise profile from 10 kHz to 100 MHz yields a final RMS jitter of just 634.43 fs. This excellent time-domain stability is a testament to the fact that the DLF gains were not just arbitrarily set, but carefully characterized and optimized to balance the trade-offs between noise suppression and loop stability, confirming the effectiveness of our characterization methodology.

These results confirm that the DLF gains were appropriately tuned. Reference clock noise is effectively suppressed at low frequencies, while quantization noise from the delta-sigma modulator is shaped toward higher frequencies. Consequently, the proposed DPLL achieves low jitter and spur-free operation under stable lock conditions.

Table I summarizes the performance of this work and provides a comparison with other DPLLs employing conventional architectures. The proposed DPLL demonstrates a competitive Figure-of-Merit (FoM) and occupies a smaller active area, highlighting its efficiency in both performance and implementation.

IV. CONCLUSION

This work presents the design, implementation, and characterization of a DPLL fabricated in 65-nm CMOS technology, with a focus on the impact of DLF gain parameters. Through both simulation and silicon measurements, we analyzed how proportional ($K_{P,PLL}$) and integral ($K_{I,PLL}$) gain values affect the phase-locking behavior, phase noise, and output spur characteristics of the PLL.

Analysis shows that setting $K_{P,PLL}$ too low leads to insufficient correction of phase errors, resulting in repeated phase error polarity and degraded low-frequency phase noise. Conversely, excessively high $K_{P,PLL}$ introduces overcompensation and instability in the loop, manifesting as strong spurious tones in both the phase noise and spectrum due to quantization noise leakage from the ΔΣ modulator. In contrast, optimal gain tuning effectively balances loop stability and noise suppression. The phase error becomes randomized, allowing the system to achieve fast locking with minimal residual noise and spurs.

Measurement results confirm that with optimal gain settings, the PLL achieves a center frequency of 2.4 GHz, an output spur level as low as −68.80 dBc, and an integrated RMS jitter of 0.638 ps. These results demonstrate that careful tuning of DLF gain parameters is essential for achieving low-jitter, spur-free, and spectrally clean DPLL operation suitable for modern communication and mixed-signal SoC applications.

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