dV_{DS}/dt Sensing Based Multi-Level Active Gate Driver IC for SiC MOSFETs

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***Abstract* - Silicon carbide (SiC) MOSFETs are widely used in power electronics to achieve higher power density and efficiency. However, as switching speeds increase to enable high-density systems, issues such as voltage overshoot, false turn-on, electromagnetic interference (EMI) arise, degrading system performance and reliability. This paper proposes a multi-level active gate driver (AGD) IC based on Miller plateau detection to improve the switching characteristics of SiC MOSFETs. The switching performance of SiC MOSFETs using the proposed gate driver IC is validated through simulations in Cadence Virtuoso. During turn-on and turn-off events, the proposed AGD shows a 5% and 4% increase in ringing magnitude compared to a conventional gate driver IC, respectively, but improves the switching speed by 18% and 21%, demonstrating a better trade-off.**

***Keywords*— Active gate driver (AGD), false turn-on, Miller plateau, silicon carbide (SiC) MOSFET, voltage spike**

I. INTRODUCTION

High power density and efficiency are critical factors in the technological advancement of the power electronics field. To achieve these goals, there is a growing demand for power semiconductor devices based on wide bandgap materials, which offer superior physical characteristics. Among them, silicon carbide (SiC) MOSFETs have gained significant attention due to their advantages over silicon insulated gate bipolar transistors (Si-IGBTs), which have been widely used in power applications. SiC MOSFETs exhibit lower intrinsic parasitic components, higher breakdown voltage, and superior thermal conductivity, enabling power conversion systems to achieve higher power density, efficiency, operating voltage and temperature, and switching frequency [1], [2]. Owing to these benefits, SiC MOSFETs are now extensively used in electric vehicles, renewable energy systems, and various industrial power sectors.

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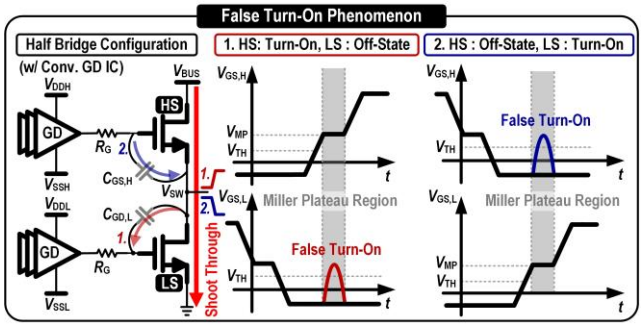


Fig. 1. Mechanism of false turn-on phenomenon.

However, several challenges arise during the high-speed operation of SiC MOSFETs, which hinder the full utilization of WBG semiconductor technology and compromise system reliability. The inherent parasitics in circuits, along with the rapid switching transients, result in high dv/dt and di/dt, inevitably generating electromagnetic interference (EMI) noise. Additionally, gate or drain voltage overshoot in SiC MOSFETs can occur, leading to degraded system performance, reduced device lifetime, or even permanent damage, thereby introducing serious design concerns [3], [4].

Fig. 1 illustrates the mechanism of false turn-on caused by gate voltage overshoot in a half-bridge circuit consisting of a high-side (HS) switch and a low-side (LS) switch. During high-speed switching operation, a steep voltage transition (dv_{SW}/dt) occurs at the switching node within the Miller plateau region. In both scenarios depicted in Fig. 1, charge is coupled into the gate terminal through the parasitic capacitance, following the relation $i = C \cdot dv_{SW}/dt$. As a result, the gate voltage of the HS or LS switch—whichever should remain off—exceeds its threshold voltage, unintentionally turning the device on. This false turn-on can lead to a significant shoot-through current, effectively creating a short-circuit condition. Such an event causes excessive power loss and may result in permanent device failure, thus it must be strictly avoided. However, the issue of false turn-on and the EMI noise induced by high dv/dt is fundamentally in trade-off with switching speed and switching loss. Therefore, conventional gate driving techniques that rely on fixed gate resistance or constant driving voltage are insufficient to simultaneously ensure high system stability and performance [5], [6].

To address these issues, various active gate driver (AGD) circuits have been proposed. AGDs can generally be

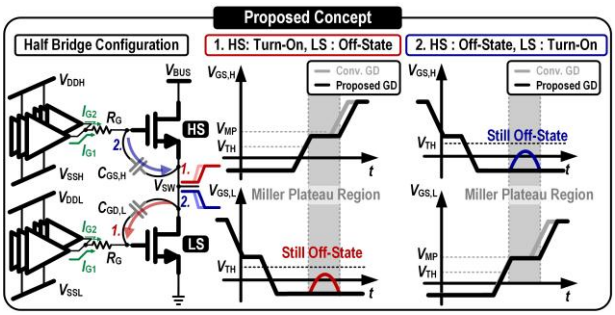


Fig. 2. Concept of the multi-level gate current driving.

categorized into open-loop and closed-loop control schemes [7]. Open-loop control methods offer the advantage of relatively simple design. However, to enhance the switching performance of power semiconductor devices, users must manually tune the optimal parameters based on the operating environment. This makes open-loop approaches highly impractical for real-world applications [8]–[10].

In contrast, closed-loop control schemes are more practical and better suited for optimization, as they can autonomously detect specific switching intervals under arbitrary operating conditions and accordingly adjust the driving current or voltage. Nevertheless, in most studies, the control topology has been implemented using off-chip components, which not only increases susceptibility to parasitic effects but also results in lower power density [11], [12]. Furthermore, some research efforts [13], [14] have introduced programmable logic devices (PLDs) such as field-programmable gate arrays (FPGAs) or complex programmable logic devices (CPLDs) to calculate the optimal driving current and voltage based on sensed information. While effective, these approaches involve high cost and system complexity.

In this paper, a multi-level AGD IC is proposed to address the false turn-on and the EMI noise induced by high dv/dt, while also mitigating the trade-off between switching speed and switching loss. By minimizing the use of external components and incorporating a closed-loop control scheme, the proposed design overcomes the limitations of previous works and enhances overall performance. The feasibility and effectiveness of the proposed gate driver (GD) circuit have been validated through simulations using Cadence™ Virtuoso.

II. DESIGN METHODOLOGY

A. Multi-level Gate Current Driving

Fig. 2 illustrates the concept of the multi-level gate current driving scheme proposed in this work. As shown in the figure, by controlling the output buffer of the GD IC to reduce the gate drive current specifically during the Miller plateau region, the resulting dv/dt can be significantly reduced. In both cases presented in Fig. 2, this leads to a decrease in the amount of charge injected into the gate of the high-side or low-side switch through the parasitic capacitance, thereby mitigating false turn-on events and other dv/dt-related issues. In conventional gate driving methods that use a fixed gate resistance or constant driving

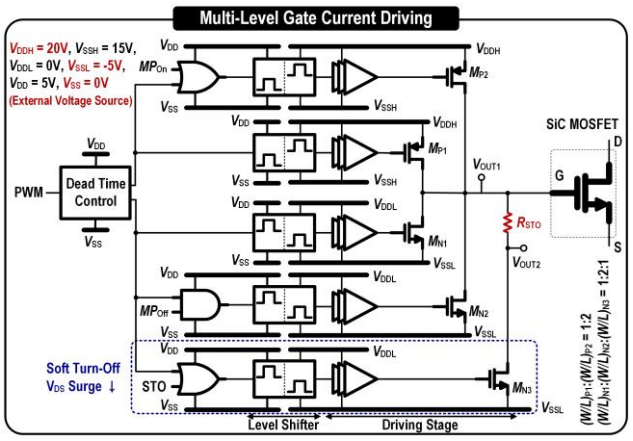
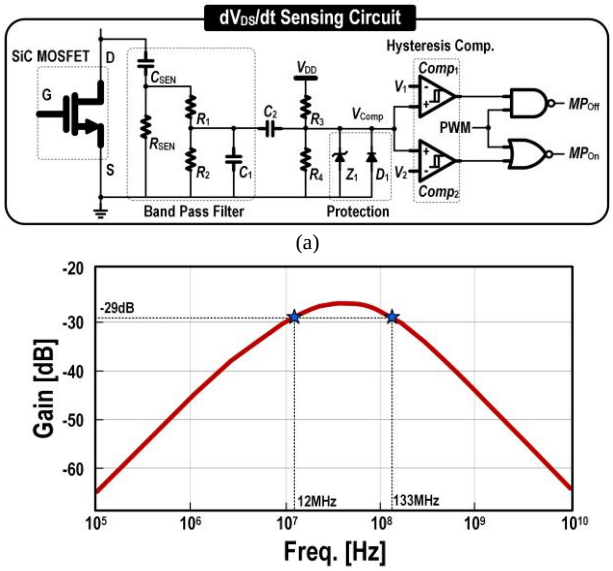


Fig. 3. Schematic of the multi-level GD IC.



(a)

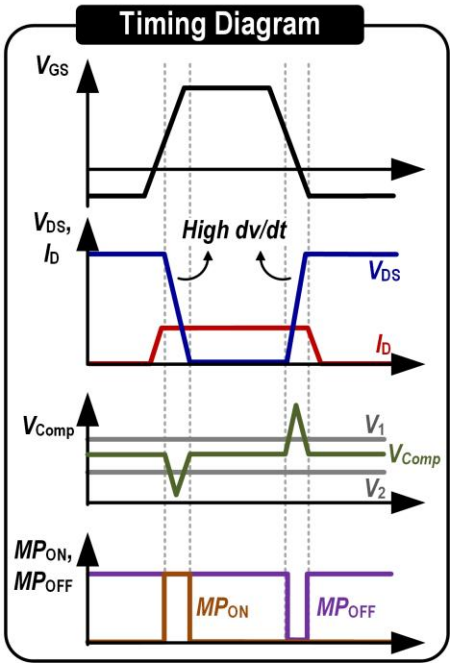
(b)

(**R 2.1**) Fig. 4. (a) Schematic of the Miller plateau sensing circuit and (b) Frequency response of the band pass filter.

voltage, lowering dv/dt typically comes at the cost of reduced switching speed across the entire transition. In contrast, the proposed method selectively slows down the switching only during the Miller plateau, thus minimizing the impact on overall switching speed while effectively suppressing high dv/dt-induced problems. Therefore, it achieves an improved trade-off between switching performance and reliability.

Fig. 3 shows the circuit diagram of the proposed GD IC. To regulate the gate current, the circuit incorporates output buffers ($M_{P1–2}$, $M_{N1–3}$) with different drive sizes. The size ratios of the output buffers are configured as $(W/L)_{P1} : (W/L)_{P2} = 1 : 2$ and $(W/L)_{N1} : (W/L)_{N2} : (W/L)_{N3} = 1 : 2 : 1$.

MP_{On} and MP_{Off} are control signals indicating the detection of the Miller plateau region during turn-on and turn-off transitions, respectively. Under normal conditions, MP_{On} and MP_{Off} remain Low and High, respectively. When the PWM signal is High, the SiC MOSFET turns off. Outside of the Miller plateau region, all $M_{N1–3}$ transistors are turned on to achieve a fast turn-off. However, during the Miller plateau,



(**R1.1**) Fig. 5. Timing diagram of the proposed dV_{DS}/dt sensing block.

the sensing circuit described in section II-B asserts MP_{Off} to Low, which turns off M_{N2}, thereby reducing the gate drive current. Conversely, when the PWM signal is Low, the SiC MOSFET turns on. Outside of the Miller plateau, both M_{P1} and M_{P2} are activated for fast turn-on. During the Miller plateau, however, the sensing circuit triggers MP_{On} to High, which disables M_{P2} and reduces the gate drive current.

B. Sensing Circuit for Miller Plateau Detection

Fig. 4 (a) illustrates the sensing circuit used to detect the Miller plateau region. During both turn-on and turn-off transitions, the drain-to-source voltage (V_{DS}) of the SiC MOSFET experiences a sharp change within the Miller plateau region. To capture this behavior, a high-pass filter is implemented using C_{SEN} and R_{SEN} to sense the slope of V_{DS} (i.e., dv_{DS}/dt). However, due to rapid switching transients and the parasitic elements within the power loop, high-frequency ringing is often induced. This ringing can propagate through the high-pass filter and cause erroneous outputs in the following comparator or logic stages. To mitigate this issue and avoid false triggering of the Miller plateau detection, additional components R_1, R_2, and C_1 are added to form a band-pass filter.

Assuming the condition $C_1 = C_2$ and $R_3 = R_4$, the transfer function of the band-pass filter can be approximated as shown in Equation (1).

$$H(s) = \frac{sR_{SEN}C_{SEN}}{1 + sR_{SEN}C_{SEN}} \cdot \frac{sR_2R_3^2C_1}{2R_3 + sR_3^2 + 2R_3(R_1 + R_2)C_1 + s^2R_2R_3^2C_1^2} \quad (1)$$

Meanwhile, the approximate cutoff frequency (f_C) of the filter can be estimated by the rise/fall time of V_{DS}, as expressed in equation (2).

TABLE I. Simulation Parameter of the Proposed GD IC

Parameter	Value
V_{DC}	400 [V]
f_{SW}	200 [kHz]
I_D	33 [A]
L_{LOAD}	300 [μH]
V_{DDH} / V_{SSL}	20 / -5 [V]
C_{SEN} / C_1 / C_2	30 / 1.2 / 1.2 [pF]
R_{SEN} / R_1 / R_2 / R_3 / R_4	50 / 20k / 30k / 50k / 50k [Ω]

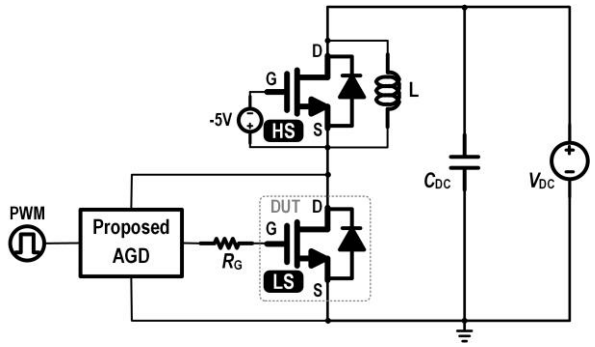
$$f_C \approx \frac{0.35}{f_C} \quad (2)$$

As a result, the passive components used in the band-pass filter can be optimally configured based on equations (1) and (2), depending on the operating environment. In the simulation environment used to validate the proposed design in this study, the parameter values were set as shown in Table I. (**R2.1**) The simulation results of the frequency response of the BPF, presented in Fig. 4(b), confirm that the cutoff frequencies of 12 MHz and 133 MHz are obtained, visually demonstrating the expected performance of the BPF.

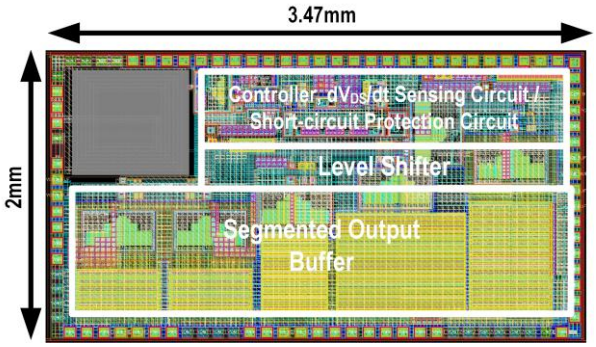
The signal processed through the band-pass filter is coupled via capacitor C_2 and applied to the inputs of two comparators ($Comp_1$ and $Comp_2$). Two comparators are used to detect the Miller plateau regions during both turn-on and turn-off transitions. In the steady state, the inputs of the comparators are biased to 2.5 V through resistors R_3 and R_4, and the reference voltages V_1 and V_2 are set to 3 V and 2 V, respectively. The signal containing the slope information of V_{DS} is coupled through C_2 and compared with the respective reference voltages to detect the Miller plateau region.

All comparators are designed with a 600 mV hysteresis to prevent false triggering caused by switching noise. (**R2.3**) This value was empirically chosen, and simulations using approximate models of parasitic components from an actual PCB confirmed that it provides an optimal trade-off between switching speed and noise immunity. Additionally, a Zener diode (Z_1) and a Schottky diode (D_1) are added to protect the comparator input transistors.

(**R1.1**) Fig. 5 is a timing diagram illustrating the generation of MP_{on} and MP_{off} signals of the proposed dV_{DS}/dt sensing circuit, which explains the detection process of the Miller plateau region. The detection process of the Miller plateau region is as follows. First, when the PWM signal is High, a turn-off operation is performed, and during the Miller plateau region, the slope of V_{DS} of the SiC MOSFET is positive. Therefore, the positive dv_{DS}/dt passes through the band-pass filter, causing the output of $Comp_1$ to go High, which results in the MP_{Off} signal going Low. This turns off the output buffer M_{N2}, thereby reducing the gate drive current. Conversely, when the PWM signal is Low, a turn-on operation is performed, and during the Miller plateau



(**R2.2**) Fig. 6. Double pulse test simulation setup.



(**R2.5**) Fig. 7. Layout design of the proposed GD IC.

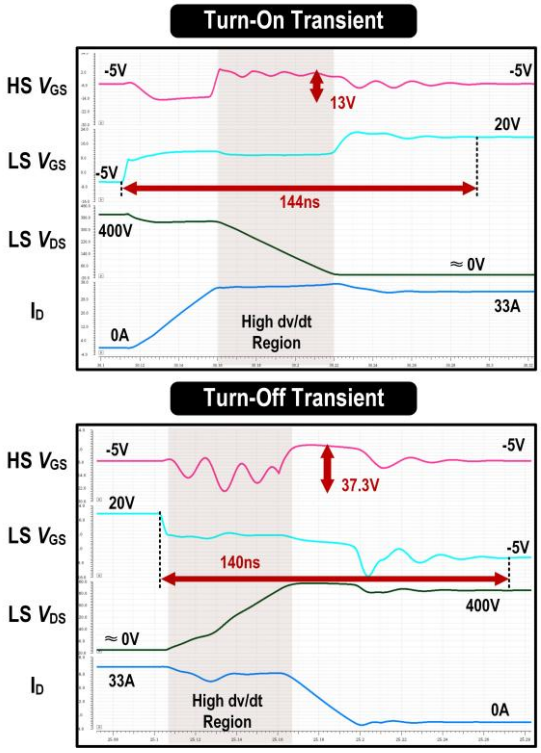
region, the slope of V_{DS} is negative. Thus, the negative dv_{DS}/dt passes through the band-pass filter, causing the output of $Comp_2$ to go Low, which results in the MP_{On} signal going High. This turns off the output buffer M_{P2}, again reducing the gate drive current.

Once the Miller plateau region ends in each case, M_{N2} or M_{P2} is turned back on to enable high-speed switching operation. As a result, since all components except the band-pass filter used to detect dv_{DS}/dt are implemented on-chip, the proposed circuit successfully realizes closed-loop control while significantly mitigating the drawbacks of previous studies.

(**R2.4**) In a half-bridge consisting of both HS and LS switches, the dV_{DS}/dt sensing circuit is shared. This is because the circuit senses the slope of the switching node voltage, which inherently contains information from both the V_{DS} of the LS and the V_{DS} of the HS. If multi-level driving is also to be applied to the HS switch, it is expected that this could be realized simply by extending the control logic.

III. RESULTS AND DISCUSSIONS

To verify the effectiveness of the proposed multi-level gate current driving scheme, simulations were conducted. In order to analyze the switching characteristics of the SiC MOSFET, a double pulse test (DPT) setup was configured as shown in Fig. 6, and simulations were performed under the conditions specified in Table I. The lower SiC MOSFET was used as the device under test (DUT), while the upper SiC MOSFET remained in the off state and operated as a freewheeling diode. Both SiC MOSFETs were modeled using MSC040SMA120B from Microchip.



(**R1.4**) Fig. 8. Simulation results with CGD.

Fig. 7 shows the layout of the IC designed using Cadence Virtuoso and the TSMC 180nm BCD process design kit (PDK). Based on this layout, post-simulation was performed considering parasitic components within the chip. Additionally, to enhance the reliability of the simulation environment, parasitic components present in the actual PCB layout, such as those in the gate loop and power loop, were modeled and included in the simulation.

(**R1.3**) During these simulations, it should be noted that in a half-bridge configuration, the HS and LS switches are never turned on simultaneously; one must always remain off. For the simulation cases, the HS switch was kept off, and the LS switch was analyzed both in the on and off states. This allows examination of the HS V_{GS} ringing under different conditions. If the HS V_{GS} ringing grows large enough to exceed the threshold voltage (V_{TH}), both LS and HS switches may unintentionally turn on, leading to a short-circuit condition. Therefore, minimizing the ringing amplitude is crucial. To quantitatively demonstrate the suppression effectiveness, HS V_{GS} ringing is presented in terms of peak-to-peak voltage. Note that auxiliary circuits such as the active Miller clamp were intentionally disabled to highlight the suppression capability, but in practical applications, these features should be activated for enhanced robustness.

Fig. 8 shows the simulation results of the conventional gate driver (CGD) circuit before applying the proposed technique, while Fig. 9 and Fig. 10 present the results after applying the proposed multi-level gate current driving scheme. To objectively verify the effectiveness of the proposed method, the simulations were performed under identical conditions, enabling or disabling only the multi-level gate current control function. In the CGD, the gate-source voltage (V_{GS}) ringing of the high-side switch during turn-on and turn-off

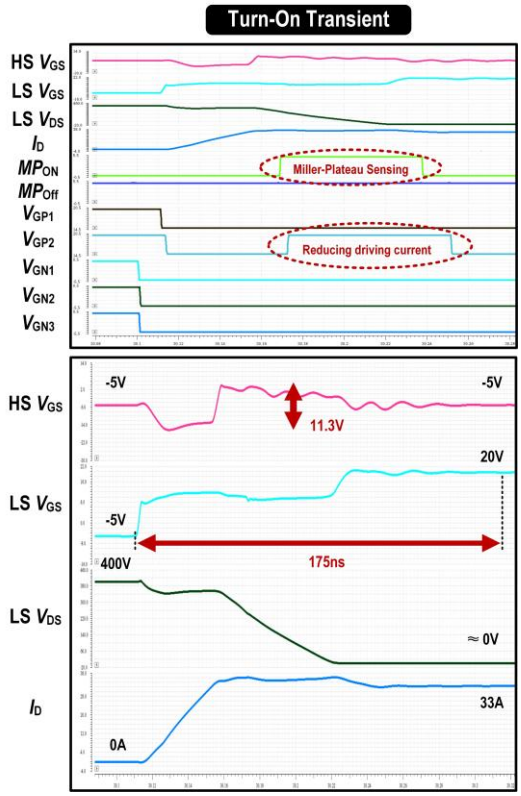


Fig. 9. Simulation results of turn-on transient with the proposed AGD.

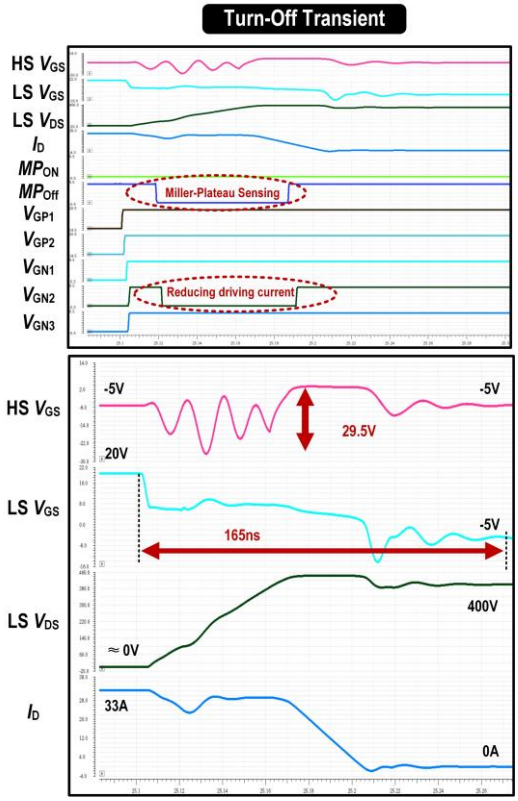


Fig. 10. Simulation results of turn-off transient with the proposed AGD.

was measured to be 13 V and 37.3 V, respectively. The corresponding V_{GS} rise and fall times of the SiC MOSFET were 144 ns and 140 ns. On the other hand, with the proposed AGD, the V_{GS} ringing of the high-side switch during turn-on and turn-off was reduced to 11.3 V and 29.5 V, respectively, while the V_{GS} rise and fall times were slightly increased to 175 ns and 165 ns. A summary of the switching characteristics with different gate resistance values (R_G) is provided in Table II. First, when comparing the proposed AGD with the CGD at the same $R_G = 10\ \Omega$, the turn-on and turn-off switching speeds were reduced by 18% and 15%, respectively, but the V_{GS} ringing was improved by 15% and 26%, respectively. Next, when comparing the proposed AGD at $R_G = 10\ \Omega$ with the CGD at $R_G = 20\ \Omega$, the V_{GS} ringing increased slightly by 5% and 4% during turn-on and turn-off, respectively. However, the switching speeds improved by 18% and 21%, respectively. As a result, since the switching speed was selectively reduced only during the Miller plateau region, the proposed method effectively mitigates high dv/dt-induced issues while improving the trade-off between switching speed and switching losses compared to conventional approaches.

TABLE II. Comparison of Turn-on/off Switching Characteristics

		CGD		Proposed AGD
R_G [Ω]		10	20	10
Turn-on	$V_{GS,Ringing}$ [V]	13	10.7	11.3
	t_R [ns]	144	207	175
Turn-off	$V_{GS,Ringing}$ [V]	37.3	28.3	29.5
	t_F [ns]	140	200	165

IV. CONCLUSION

In this study, a GD IC was proposed to enable safe and reliable high-speed switching of SiC MOSFETs by overcoming limitations that conventional gate drivers fail to address. The proposed circuit enables multi-level gate current control by detecting the dv_{DS}/dt of the SiC MOSFET and employing a pair of output buffers with different current-driving capabilities, the proposed circuit enables multi-level gate current control. This approach selectively reduces the gate drive current only during the Miller plateau region. The effectiveness of the proposed method was verified through simulation results, which demonstrated improvements in the trade-off between switching speed and switching loss, as well as mitigation of high dv/dt-related issues such as false turn-on. In addition, when abnormal conditions such as over-current or short-circuit faults occur, the proposed design utilizes part of the internal output buffer to implement a soft turn-off operation without requiring any additional external components. This approach enhances the reliability of SiC MOSFETs in a cost-effective and straightforward manner. The proposed functionality was validated through simulations, and chip fabrication has been completed. Experimental verification will be conducted to further demonstrate the advantages of the proposed architecture.

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