# A Digitalized Chaotic Oscillator Probabilistic Bit for Static Annealing Ising Machine

Woojin Lee[1] and Chulwoo Kim[a]
Department of Electrical Engineering, Korea University
E-mail : [1]lwj@kilby.korea.ac.kr

***Abstract* – This work presents a digital tent-map chaotic oscillator (DCO)-based probabilistic bit (p-bit) architecture for compute-in-memory probabilistic computing applications. Unlike conventional p-bits, the DCO-based p-bit takes both advantage of high throughput and robustness of pseudo-random number generator (PRNG)-based p-bits and small area consumption of the analog domain p-bits. The DCO achieves high energy efficiency of 0.041 pJ/bit. We apply this noise generator to static annealing, a schedule that maintains fixed temperature during operation, and demonstrate its effectiveness on the Max-Cut problem. Compared to conventional thermal annealing approaches that rely on gradually changing temperatures, the static annealing scheme converges faster and achieves lower final Hamiltonian values in our experiments. Our findings highlight that static annealing is not only feasible but advantageous in solving complex problems with compute-in-memory hardware.**

***Keywords*—Probabilistic bit (p-bit), chaotic oscillator, static annealing, Ising machine**

## I. INTRODUCTION

Probabilistic computing has recently emerged as a promising approach to solve combinatorial optimization with high energy efficiency and inherent parallelism. The key computational primitive in such systems is the probabilistic bit (p-bit), which stochastically fluctuates between binary states with a tunable probability. Prior implementations of p-bits have used either analog domain noise sources [1]–[4], such as magnetic tunnel junctions (MTJs) [1], or digital pseudo-random number generators (PRNGs) [5]–[7]. Each having distinct trade-offs in terms of area, robustness, and statistical quality.

As shown in Fig. 1, analog p-bits benefit from compact circuit implementations but are often susceptible to process, voltage, and temperature (PVT) variations, as well as static power consumption [1], [2]. In contrast, digital p-bits using linear-feedback shift registers (LFSRs) [5], [7] or XOR-based PRNGs [6] are more robust and scalable, but require large hardware resources to mitigate correlation and ensure sufficient cycle length. Therefore, directly adopting PRNGs as a noise generator for a p-bit limits their applicability to large-scale compute-in-memory (CIM) systems.

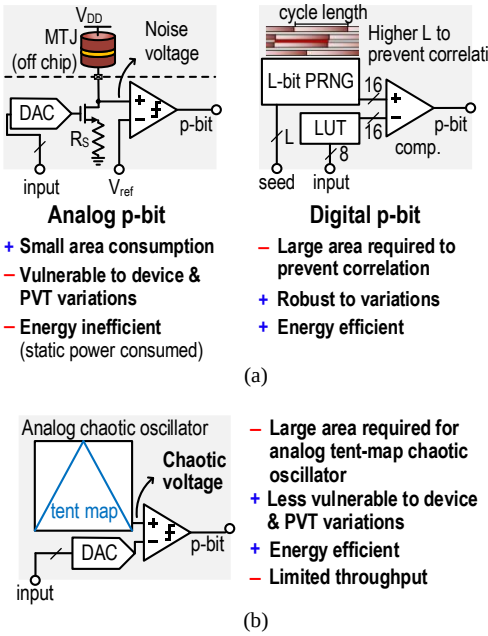



Fig. 1. Conventional p-bits which utilize (a) analog noise voltage or PRNG and (b) analog domain chaotic oscillator as a noise generator.

To overcome these limitations, we propose a digitalized chaotic oscillator (DCO)-based p-bit architecture (Fig. 2) that combines the statistical robustness of digital p-bits with the compactness of analog chaotic oscillators. Our DCO p-bit employs a tent-map-based chaotic update rule enhanced with XOR boosting, generating high-quality noise sequences with minimal correlation and reduced area overhead. The proposed p-bit achieves a high energy efficiency of 0.041 pJ/bit and supports high-throughput operation suitable for parallel large-scale implementation.

We demonstrate the effectiveness of the DCO-based p-bits by applying them to static annealing, a low-temperature, fixed-schedule optimization framework. Unlike conventional thermal annealing approaches, which gradually reduce system temperature to converge to suboptimal local

a. Corresponding author; ckim@korea.ac.kr

Manuscript Received Apr. 25, 2025, Revised May 24, 2025, Accepted May 26, 2025

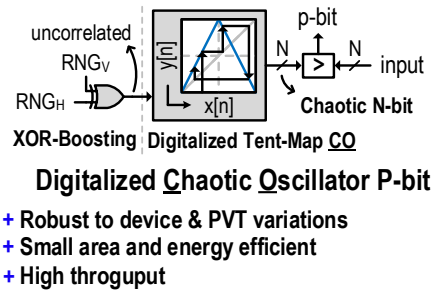



Fig. 2. Simplified block diagram of the proposed digitalized chaotic oscillator p-bit.

minima, static annealing maintains a constant low system temperature, enabling faster convergence and lower final Hamiltonian values in combinatorial problems such as Max-cut. The proposed architecture is fabricated in 28nm CMOS and integrates 1440 DCO p-bits, achieving state-of-the-art energy and area efficiency compared to previous p-bit-based systems.

## II. PROPOSED HARDWARE DESIGN FOR STATIC ANNEALING ISING MACHINE WITH DCO P-BITS

### *A. Digitalized tent-map chaotic oscillator*

Prior works [1], [2] of analog-domain p-bits suffer from their inherent sensitivity to PVT variations, necessitating careful per-device calibration before deployment. This calibration requirement significantly limits the scalability of large-scale probabilistic computing systems, where large number of p-bits is required. To mitigate this issue, recent work [3] proposed an analog tent-map chaotic oscillator (ACO) as a noise source for p-bit generation (Fig. 1b). The tent-map oscillator exhibits chaotic behavior without the need for calibration, and its broad noise range enables an 8-bit resolution for the input-to-probability transfer function, thereby improving the dynamic range and accuracy of the p-bit outputs.

Despite these advantages, ACO relies on a voltage amplifier that forms a specific chaotic map with a slope higher than 1, which inherently limits its throughput and incurs significant area overhead compared to other analog-domain noise sources. In addition, ACO suffers from escaping issue [3], [8], which is a loss of chaotic behavior due to an out-of-range state caused by circuit mismatch or inherent noise. To prevent the escaping issue, additional techniques should be applied such as flipped-hook [3].

Fig. 2 shows a simplified diagram of tent-map DCO. Compared to ACO, where an inherent device noise shifts the chaotic trajectory every cycle and the chaotic behavior is maintained by analogously implemented chaotic map, DCO takes a random bit to least significant bit (LSB) to make unpredictable chaotic trajectory and digital circuits for chaotic map implementation. Fig. 3a shows a schematic of DCO with 6-bit output resolution. To form a DCO with N-bit output resolution, only N+1 DFFs and N multiplexers (MUXs) and N inverters are required. The slope of two of the tent map is easily implemented with shift registers, and

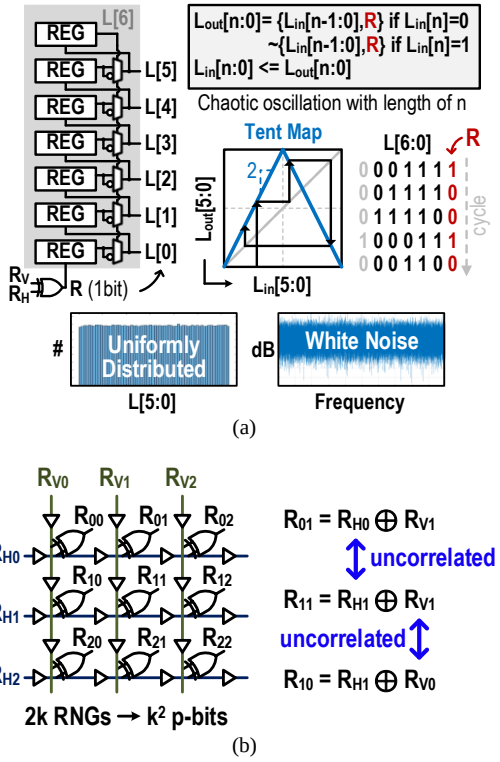



Fig. 3. A schematic and the operation of the proposed DCO (a), and a diagram of the proposed XOR boosting technique (b).

the MUXs and inverters form a tent map based on the last DFF output bit. The tent-map DCO follows the exact tent map equation:

$$x_{n+1} = \begin{cases} 2x_n + R, & 0 \le x_n < 2^{N-1} \\ -2x_n + R + 2^{N+1}, & 2^{N-1} \le x_n < 2^N \end{cases} \quad (1)$$

where $x_n$ is a N-bit DCO state expressed in integer, $R$ a random bit, which is rather 0 or 1, and $N$ the DCO output resolution. Based on the characteristics of tent-map [3], the DCO outputs form a uniform distribution and a white noise characteristic.

### *B. XOR boosting*

If a single PRNG is attached to each DCO, the architecture still suffers from the same problem as PRNG-based p-bit. To prevent from the correlation dependent area consumption issue of PRNG-based p-bits, we propose a XOR boosting technique (Fig. 3b). By using XOR boosting technique, a single DCO takes two random bits, horizontal and vertical random bits ($R_H$, $R_V$). By passing through a XOR gate, the output bit becomes uncorrelated to neighbor bits, and since the unpredictable trajectories of each DCOs make the DCO output bits uncorrelated. Thanks to the XOR boosting, only 2k RNGs are required for $k^2$ DCO-based p-bits.

### *C. Static annealing and hybrid-connected Ising machine*

Annealing-based optimization has been widely adopted in probabilistic computing systems to address various combinatorial optimization problems. In most

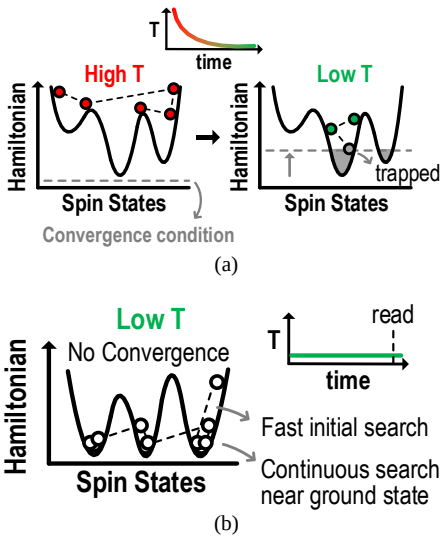



Fig. 4. Diagram of Hamiltonian in Ising machine based on dynamic annealing (a), and static annealing with low system temperature (b).

implementations, a dynamic annealing schedule is used, where the system temperature is gradually decreased over time to escape local minima and promote convergence toward the global minimum (Fig. 4a). This approach, often referred to as simulated annealing, is effective but computationally costly on large-scale hardware implementation since a broad range of system temperature needs to be multiplied in each p-bit.

Recent work [1] has introduced static annealing as a compelling alternative, where the system operates at a fixed temperature throughout the entire computation. Rather than relying on temperature decay, the solution space is explored by maintaining continuous stochastic fluctuations, allowing for repeated trials around near-optimal states. In their study, static annealing was successfully applied to perform prime factorization by constructing histograms of low-energy states. The correct factors were identified as the most frequently visited configurations, demonstrating the method's effectiveness in applications where convergence to exact solutions is not mandatory, but high-probability outcomes are sufficient. Despite this advantage, the application of static annealing to general-purpose Ising machine has been limited. Most existing Ising machines rely on dynamic schedules due to their closer resemblance to physical annealing processes.

As shown in Fig. 4b, this work adopts static annealing to enable fast and power efficient exploration of solution candidates, which is particularly well-suited for compute-in-memory systems. To further enhance both convergence speed and mapping flexibility, we adopt a hybrid-connected Ising machine architecture (Fig. 5a). This structure combines the low-latency benefits of sparsely-connected p-bits to intra-unit interactions with the high programmability of fully-connected p-bits to inter-unit interactions, enabling efficient implementation of optimization problems without sacrificing either parallelism or scalability.

Fig. 5b shows the layout of a single Ising unit. An Ising unit consist of 6 p-bits with multiply-and-accumulate (MAC)

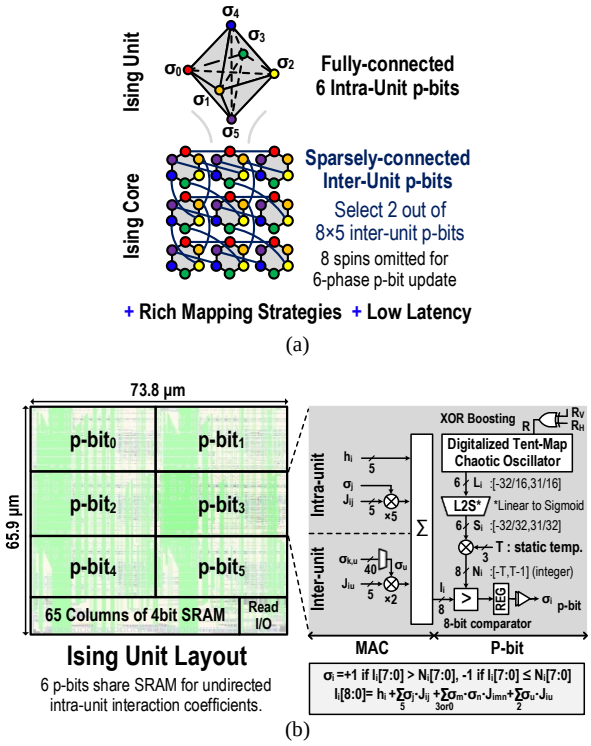



Fig. 5. The proposed hybrid-connected Ising machine (a) and a diagram of DCO p-bit with inter-unit and intra-unit interactions (b).

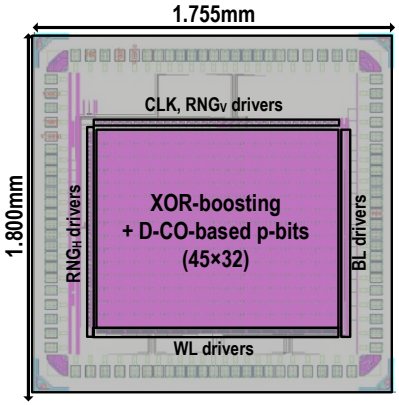
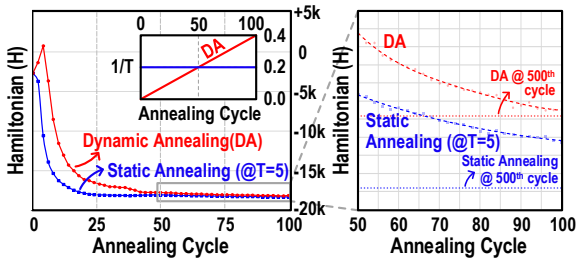



Fig. 6. Chip layout containing 45x32 DCO-based p-bits.

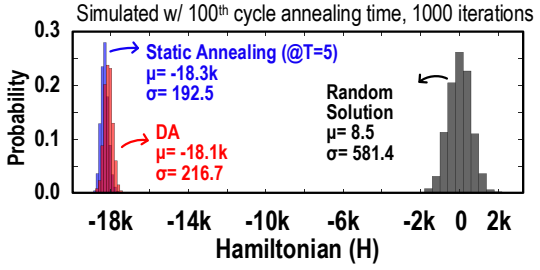
block, SRAM array for interaction coefficient, and read I/O. As shown in Fig. 6, 45x32 DCO-based p-bits, total number of 1440 number of p-bits, are integrated in a single chip. A single DCO occupies 30.2 µm$^2$, while the ACO [3] that was used for p-bit occupies 28800 µm$^2$. Even after normalizing the area with each technology, the normalized area of DCO is approximately 23 times smaller than that of ACO [3].

## III. RESULTS AND DISCUSSIONS

Fig. 7 shows the Hamiltonian of the proposed static-annealing-based Ising machine during the Max-Cut optimization. Compared to the dynamic annealing, the Hamiltonian of the static annealing drastically drops to lower value due to the low system temperature value. As illustrated




(a)




(b)

Fig. 7. The transient Hamiltonian using dynamic annealing and static annealing (a), and the histogram of Hamiltonian at the 100th cycle point (b).

in Fig. 7a, even after 500 annealing cycles, static annealing consistently maintains a significantly lower Hamiltonian compared to dynamic annealing. This is attributed to the fixed low-temperature operation, which facilitates continuous exploration near the ground state while the dynamic annealing tends to trap to local ground state with higher Hamiltonian. Notably, the Hamiltonian achieved by static annealing at the 500th cycle is approximately 4.3x lower than the final value achieved by dynamic annealing under identical runtime conditions.

To evaluate statistical robustness, 1,000 annealing iterations were performed and the Hamiltonian values at the 100th cycle were collected and plotted as a histogram (Fig. 7b). The results indicate that static annealing yields a lower average Hamiltonian compared to that of dynamic annealing. This confirms that not only does static annealing achieve lower energy states more rapidly, but it also shows reduced variance, demonstrating more stable convergence behavior.

Table I presents a performance comparison of the state-of-the-art p-bit designs. The proposed DCO-based p-bit, implemented in 28-nm CMOS, operates in the digital domain which ensures calibration-free operation and achieves a high operating frequency of 1000 MHz at 0.9 V supply voltage, which is 20 times faster than that of ACO [3]. The energy efficiency is also reduced to 0.041 pJ/bit, which includes the energy consumption of horizontal and vertical RNG drivers.

## IV. CONCLUSION

This work presents a DCO-based p-bit architecture optimized for probabilistic computing with CIM architecture. By replacing the analog chaotic oscillator with a fully digital circuit, the proposed DCO achieves compact area, and high energy efficiency of 0.041 pJ/bit, which is over 100 times lower than prior analog implementations. To support a large-scale in-memory probabilistic computing, a two-dimensional XOR boosting technique is introduced to minimize RNG overhead.

Integrated with a static annealing engine, the DCO-based p-bits demonstrated superior performance in solving Max-Cut problems. Simulated results show that static annealing achieves faster and more stable convergence compared to dynamic annealing, attaining significantly lower average Hamiltonian values. The fabricated chip integrates 1,440 DCO-based p-bits in 28-nm CMOS.

TABLE I. Comparison with State-of-the-Art P-Bits

| | **This Work** | Sci. Rep.'25 [3] | ISSCC'23 [4] | Nature Elec.'22 [5] | Nature'19 [1] |
|---|---|---|---|---|---|
| Device | **28-nm CMOS** | 180-nm CMOS | 65-nm CMOS | FPGA | MTJ + 14nm FinFET |
| Noise Generation Domain | **Digital Chaotic Bit** | Analog Chaotic Voltage | Analog Voltage | Digital bit | Analog Voltage |
| Application | **Max-Cut** | Factorization | 3SAT | Factorization, 3SAT | Factorization |
| Annealing Policy | **Static** | Dynamic | Dynamic | Dynamic | Static |
| Connectivity | **Hybrid** | Full | N/A | Sparse | Full |
| Noise Generator | **Digitalized Chaotic Oscillator** | Tent-map Chaotic Oscillator | Current Driven by Ring Oscillator | 32-bit LFSR | Stochastic MTJ |
| Calibration Required | **No** | No | Yes | No | Yes |
| Operating Frequency [MHz] | **1000 @ 0.9 V** | 50 @ 1.8V | 400 @ 1.2 V | 15, 30 | 0.001 [c] |
| Noise Generator Output Resolution | **6-bit** | 8-bit [d] | 2-bit [d] | 32-bit | <5-bit [d e] |
| Nosie Generator Energy efficiency [pJ/bit] | **0.041 @ 0.9 V** | 4.26 @ 1.8 V | 0.094 [f] @ 1.2 V | Not Reported | 20,000 [c] |

[a] Number of IMT-based p-bit that generates probability near 50% is under 75 for total 100 p-bits.
[b] Fluctuation speed ($\tau_{fluctuation}$): ~ns or <ns.
[c] Considered the smallest zero-bias dwell time as the minimum retention time, 1 ms.
[d] Input resolution that extracts stochastic output bit of analog p-bit.
[e] Displays stochastic behavior within input voltage range of ±75mV, and 12-bit DAC with 6.1 mV resolution.
[g] Power consumption of 64 noise generators at 400Mb/s: 2.41 mW.

## ACKNOWLEDGMENT

The chip fabrication and Electronic Design Automation (EDA) tools were supported by the IC Design Education Center (IDEC), Daejeon, South Korea.

## REFERENCES

[1] W. A. Borders, A. Z. Pervaiz, S. Fukami, K. Y. Camsari, H. Ohno, and S. Datta, "Integer factorization using stochastic magnetic tunnel junctions," *Nature*, vol. 572, no. 7774, pp. 390–393, 2019.

[2] S. Heo, D. Kim, W. Choi, S. Ban, O. Kwon, and H. Hwang, "Experimental Demonstration of Probabilistic-Bit (p-bit) Utilizing Stochastic Oscillation of Threshold Switch Device," *in 2023 IEEE Symposium on VLSI Technology and Circuits*, June 2023, pp. 1–2.

[3] W. Lee, H. Kim, H Jung, Y. Choi, J. Jeon, and C. Kim, "Correlation free large-scale probabilistic computing using a true-random chaotic oscillator p-bit," *Sci. Rep.*, vol. 15, no. 8018, 2025.

[4] D. Kim, N. M. Rahman, S. Mukhopadhyay, "A 32.5mW Mixed-Signal Processing-in-Memory-Based k-SAT Solver in 65nm CMOS with 74.0% Solvability for 30-Variable 126-Clause 3-SAT Problems," *in 2023 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech.*

*Papers*, Feb. 2023, pp. 418–420.
[5] N. A. Aadit *et al.*, "Massively parallel probabilistic computing with sparse Ising machines," *Nature Electronics*, vol. 5, no. 7, pp. 460–468, 2022.
[6] K. Yamamoto *et al.*, "STATICA: A 512-Spin 0.25M-Weight Annealing Processor With an All-Spin-Updates-at-Once Architecture for Combinatorial Optimization With Complete Spin–Spin Interactions," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 165–178, Jan. 2021.
[7] H. Jung, H. Kim, W. Lee, J. Jeon, Y. Choi, T. Park, and C. Kim, "A quantum-inspired probabilistic prime factorization based on virtually connected Boltzmann machine and probabilistic annealing," *Sci. Rep.*, vol. 13, no. 16186, 2023.
[8] M. Kennedy, R. Robatti, and G. Setti, *Chaotic Electronics in Telecommunications*, CRC Press, 2000.

**Woojin Lee** (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2022, where he is currently pursuing the integrated M.S. and Ph.D. degree.

His current research interests include probabilistic computing, CMOS true random number generators, and high speed analog-to-digital converter (ADC) designs.

**Chulwoo Kim** (Senior Member, IEEE) received the B.S. and M.S. degrees in electronics engineering from Korea University in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 2001.

In May 2001, he joined IBM Microelectronics Division, Austin, TX, where he was involved in Cell processor design. Since September 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor at the University of California at Los Angeles in 2008 and at the University of California at Santa Cruz in 2012. He is a coauthor of two books, namely, CMOS Digital Integrated Circuits: Analysis and Design (McGraw Hill, 4th edition 2014) and High-Bandwidth Memory Interface (Springer, 2013). His current research interests are in the areas of wireline transceiver, power management, data converters, and quantum-inspired computing.

Dr. Kim received the Samsung HumanTech Thesis Contest Bronze Award (1996), the ISLPED Low-Power Design Contest Award (2001, 2014), the DAC Student Design Contest Award (2002), SRC Inventor Recognition Awards (2002), the Young Scientist Award from the Ministry of Science and Technology of Korea (2003), the Seoktop Award for excellence in teaching (2006, 2011, 2018, 2023) and ASP-DAC Best Design Award (2008) and Special Feature Award (2014), Korea Semiconductor Design Contest: Prime Minister's Award (2016). He served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference and as a Guest Editor for the IEEE Journal of Solid-State Circuits. He also served as the Chair of the SSCS Seoul Chapter and as the Distinguished Lecturer of the IEEE Solid-State Circuits Society for 2015 2016. He is currently on the editorial boards of the IEEE Journal of Solid-State Circuits and Transactions on VLSI Systems and an elected AdCom member of the IEEE Solid State Circuits Society.