A Single-Ended NRZ Transceiver in 28-nm CMOS Process with Power-Isolated LVSTL Driver and 3-Stage Sampler for Low-Power Memory Interfaces

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***Abstract* – This paper presents a low-power, high-speed non-return-to-zero (NRZ) transceiver for low-power memory interfaces. The proposed transceiver (TRX) consists of a single-ended transmitter (TX) and receiver (RX), achieving data rates of 15 Gb/s and 12 Gb/s, respectively, each incorporating a 2-tap feed-forward equalizer (FFE) and a 1-tap direct decision feedback equalizer (DFE). The quarter-rate clocking architecture, enhancing timing margin and power efficiency, is adopted in both the transmitter and the receiver. The TX utilizes a low voltage swing terminated logic (LVSTL) driver operating at a 0.5-V VDDQ and employs a 2-tap de-emphasis FFE to compensate for channel loss. The RX incorporates a 3-stage sampler structure. The 1-tap direct DFE effectively compensates for inter-symbol interference (ISI) caused by channel loss, improving signal integrity. Fabricated in a 28-nm CMOS process, the TRX achieves an energy efficiency of 0.64 pJ/bit at 15 Gb/s in the TX and 0.043 pJ/bit at 12 Gb/s in the RX, providing a solution for high-speed and low-power memory interfaces.**

***Keywords*—Equalizer, low power, memory interface, non-return-to-zero, quarter-rate clocking, transceiver**

I. INTRODUCTION

In the face of rapidly advancing technologies, various interface standards are increasingly demanding higher bandwidths [1]. Within this context, mobile dynamic random-access memory (DRAM) interface, particularly low power double data rate (LPDDR), requires both increased speed and reduced power consumption with each successive generation [1]-[2]. To achieve low power operation, LPDDR4X mandated a reduction of the output driver's supply voltage, VDDQ, to 0.6 V, while LPDDR5 and LPDDR5X further lowered VDDQ to 0.5 V [3]-[4].

In LPDDR interfaces, to achieve low power consumption, a voltage-mode driver is employed instead of a current-mode driver, which suffers from static current consumption. As the VDDQ of LPDDR4X is reduced, a voltage-mode driver capable of operating at a lower voltage is required. Fig. 1 shows the two voltage-mode driver structures. Fig. 1(a) is a pseudo open drain logic (PODL) structure adopted up to LPDDR3, and Fig. 1(b) is the low voltage swing terminated logic (LVSTL) structure employed from LPDDR4. In the PODL structure, a reduced supply voltage can lead to nonlinear output impedance behavior due to limited voltage headroom and degraded MOSFET performance. In contrast, the LVSTL structure utilizes an NMOS pull-up transistor, which enhances linearity at low supply voltages and reduces power consumption owing to its low output swing [5]-[7]. Moreover, the increased current-driving capacity of NMOS transistors allows for reduced transistor dimensions without compromising drive strength, consequently enhancing speed performance by minimizing parasitic capacitance [5].

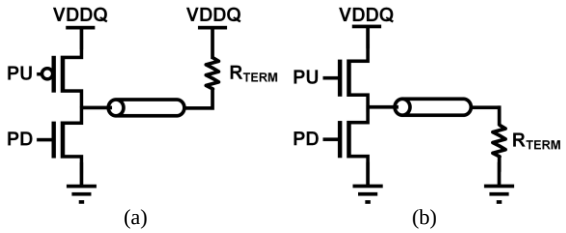

Fig. 1. Output driver structures of (a) PODL and (b) LVSTL.

In high-speed data transmission, an equalizer circuit is essential to compensate for channel loss. To mitigate inter-symbol interference (ISI) in the channel, pre-emphasis or de-emphasis feed-forward equalization (FFE) is commonly employed at the transmitter (TX) [6]. In the receiver (RX), a continuous-time linear equalizer (CTLE) or a decision feedback equalizer (DFE) is commonly adopted. While the CTLE improves signal quality by boosting high-frequency components, it also amplifies high-frequency noise and increases power consumption, making them unsuitable for LPDDR memory interfaces [8]. As a result, DFE-only equalization is widely used, typically with a 1-tap direct DFE architecture at memory interfaces [3]. Fig. 2(a) and (b) show the 1-tap direct DFE and loop-unrolled DFE architectures. The direct DFE has better area efficiency and uses less power than the loop-unrolled architecture, and its sequential feedback also removes the need for parallel loop-unrolled paths, reducing design complexity [2], [9].

The following key trends are evident in recent studies on low-power memory interfaces [1], [6], [10]-[12]. In the TX, the output drivers adopt LVSTL structures for memory interfaces [1], [6], [11], where [1] and [6] propose a pre-emphasis technique based on FFE. Pre-emphasis has the

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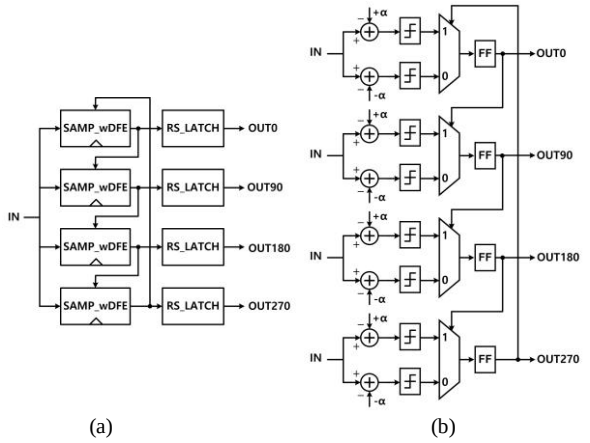


Fig. 2. RX implementation using (a) direct and (b) loop-unrolled 1-tap DFE.

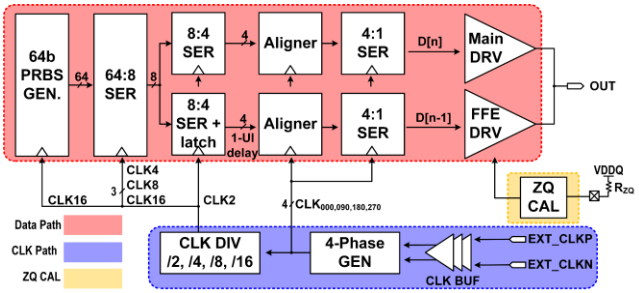


Fig. 3. TX top block diagram.

advantage of maintaining a peak-to-peak swing. However, as the number of DQ pins per channel in LPDDR increases, the spacing between DQ pins continues to narrow, further increasing crosstalk noise when pre-emphasis is applied [13]. [11] introduces a stacked driver by adding a MOSFET stack to the conventional LVSTL structure. Although this technique can address power supply-induced jitter issues in conventional LVSTL structures, it may suffer from voltage headroom limitations due to the additional stacked MOSFET. In the RX, [10] employed an asymmetric 1-tap DFE that selectively compensated for ISI depending on the data pattern, and [12] introduced a 1-tap DFE sense amplifier that combines a double-tail amplifier with a cross-coupled inverter structure.

This paper presents a single-ended non-return-to-zero (NRZ) transceiver (TRX) for low-power memory interfaces. The TX employs a voltage-mode driver based on the power isolated (PI)-LVSTL architecture and utilizes a 2-tap de-emphasis FFE technique. The RX incorporates a 3-stage sampler architecture with a 1-tap direct DFE and is designed to ensure stable performance even at low supply voltages.

The remaining parts are organized as follows: Section II details the TX architecture. Section III outlines the RX architecture. Section IV presents the measurement results. Finally, Section V concludes the paper with a comparative analysis and validation of these results.

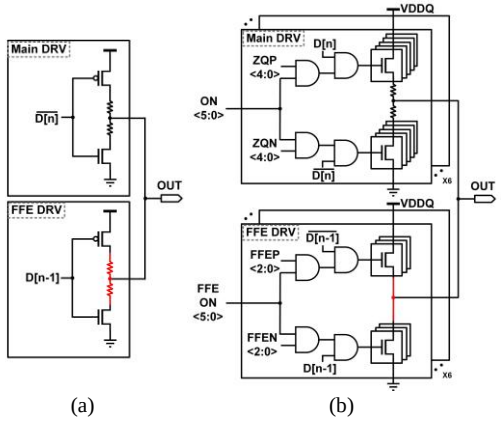


Fig. 4. Output drivers: (a) conventional FFE driver and (b) proposed FFE drivers.

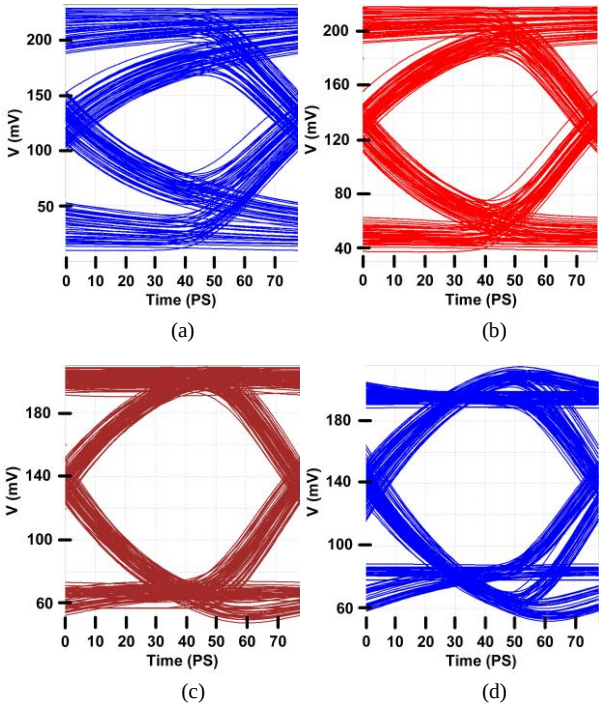


Fig. 5. Simulated eye diagrams when applying a FFE coefficient of (a) 000, (b) 001, (c) 010, and (d) 011.

II. TRANSMITTER

A. TX Architecture

The overall block diagram of the TX is depicted in Fig. 3. In this architecture, the output driver is designed to operate at a VDDQ of 0.5 V, and the other circuit blocks operate at a VDD of 1.05 V to meet the recent LPDDR specification. In order to improve timing margin and power efficiency, the transmitter utilizes quarter-rate clocking operation using a lower clock (CLK) frequency. When an external CLK signal enters the CLK path, a 4-phase generator (4-phase GEN) divides the input CLK signal frequency by two and generates 4-phase CLK signals to enable quarter-rate operation. Subsequently, CLK dividers (CLK DIV) generate lower-frequency CLK signals, which are then distributed to the data path.

The data path includes a 64-bit pseudo-random binary

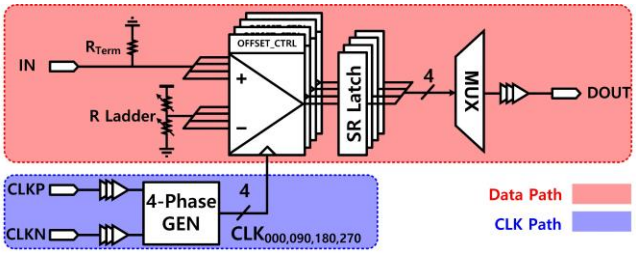


Fig. 6. RX top block diagram.

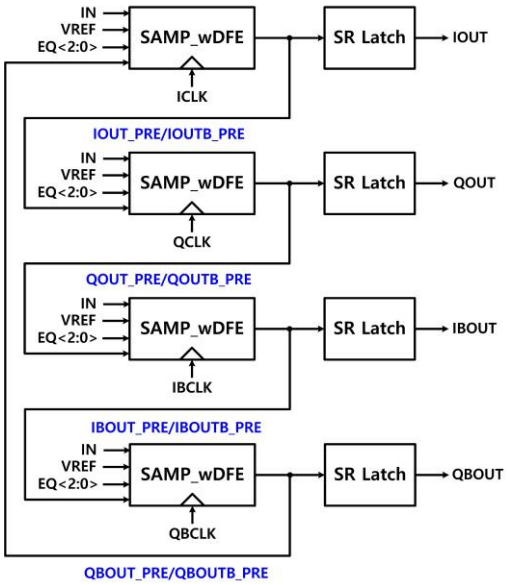


Fig. 7. Block diagram of sampler integrated with 1-tap direct DFE.

sequence generator (PRBS GEN), a 64:8 serializer (SER), an 8:4 SER, and an 8:4 SER with a latch, two aligners, two 4:1 SERs, and Main and FFE drivers (DRVs). The 64-bit parallel PRBS data is serialized into 8-bit data using the 64:8 SER. The serialized data is passed to two 8:4 serializers (SERs), one of which includes the latch to generate 1-UI delayed data for the FFE. The outputs of the two 8:4 SERs are processed through aligners and 4:1 SERs and are finally serialized into D[n] and its 1-UI delayed version D[n-1]. The main output, D[n], is sent to the Main DRV, while the 1-UI delayed signal, D[n-1], is conveyed to the FFE DRV.

B. Main and FFE Driver

Figs. 4(a) and (b) illustrate the output DRVs merged with a conventional and proposed de-emphasis FFE DRVs [14]. Both output DRVs adopt a 2-tap de-emphasis-based FFE. However, our proposed DRV employs a PI-LVSTL structure, utilizing NMOS transistors in both the pull-up and pull-down paths. Starting with LPDDR4X, the VDDQ for the output DRV has been lowered to reduce power consumption, and the PI-LVSTL structure with an N-over-N driver configuration is employed for the output DRV to operate under a separately supplied low VDDQ. In addition, to achieve the output impedance linearity requirement of JEDEC specification [3], passive resistors of about 100 Ω were added to the pull-up and pull-down paths at the Main DRV [15]. The de-emphasis-based FFE integrated into both

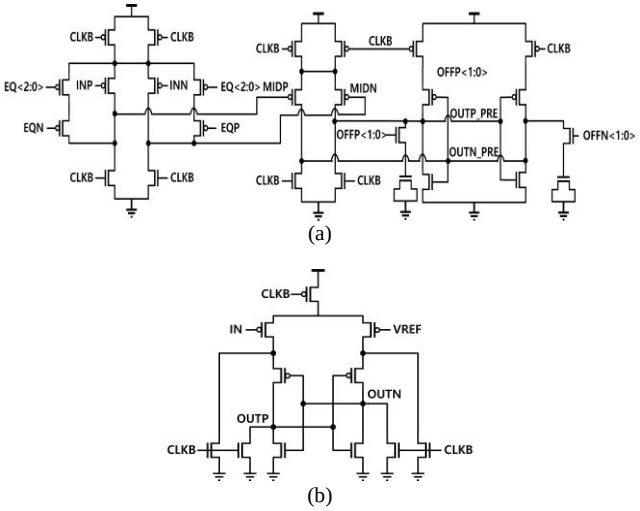


Fig. 8. Circuit diagram of (a) 3-stage sampler including 1-tap DFE and offset cancellation and (b) conventional StrongArm-latch sampler.

designs improves signal integrity. When identical bits are transmitted consecutively, low-frequency components dominate the signal. By attenuating these low-frequency components, the equalizer effectively emphasizes the relative strength of high-frequency components. This addresses the attenuation in high-frequency signals caused by the low-pass features of transmission channels.

In the conventional structure, both Main and FFE DRVs have a termination passive resistor. However, adding the passive resistor to each segment increases the MOSFET size in the DRV, which can be unsuitable for memory interfaces with parallel DQ signaling. The proposed FFE DRV does not use the termination passive resistor, making it approximately four times smaller than the Main DRV and providing better FFE resolution than conventional structures. Our FFE supports 7-step controllability with a resolution of 15 mV, resulting in a total range of 105 mV.

Fig. 5 illustrates the post-layout simulated eye diagrams through a channel with −7.6 dB loss at 12.8 Gb/s, based on the various FFE coefficients. These results show that increasing the FFE coefficient enlarges the eye-opening but eventually leads to over-equalization. These simulation results confirm the FFE operation. The proposed structure makes it harder to achieve perfect impedance matching compared to conventional designs. However, in some cases, allowing a small amount of mismatch can even help improve signal quality [16]. Simulation results show that the eye improvement due to FFE operation is greater than distortion due to reflection caused by impedance mismatch.

III. RECEIVER

A. RX Architecture

Fig. 6 shows the top-level block diagram of the RX. As the RX adopts a quarter-rate clocking architecture, 4-phase CLK must be distributed to four samplers. The external differential CLK input is converted into 4-phase CLK signals (ICLK, QCLK, IBCLK, QBCLK) with half the input frequency and then distributed to four samplers. The

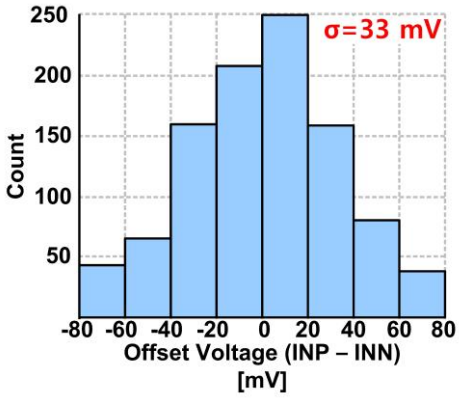
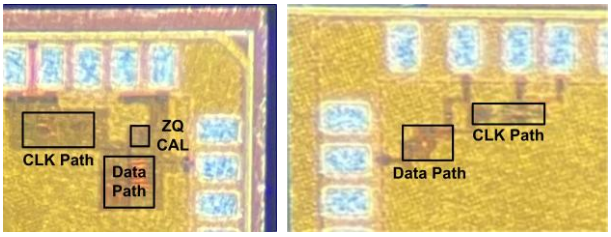
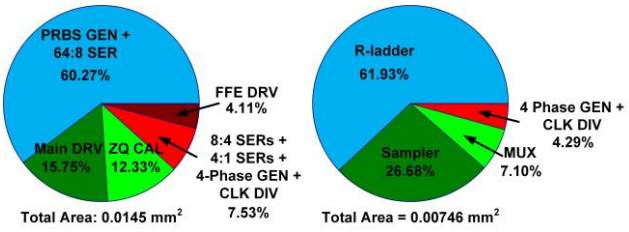


Fig. 9. Monte-Carlo simulation result of sampler's offset voltage.



(a) (b)

Fig. 10. Die photographs of (a) TX and (b) RX.



(a) (b)

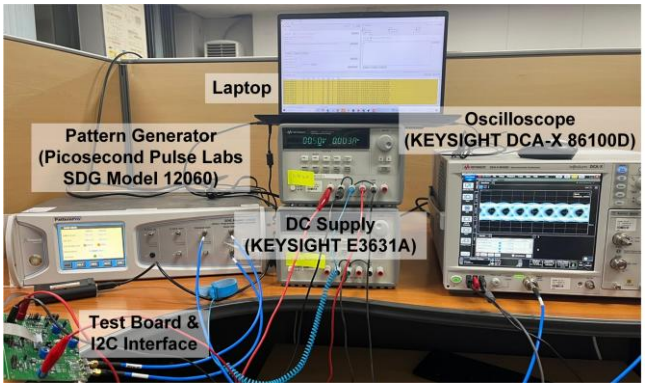
Fig. 11. Area breakdowns of (a) TX and (b) RX.

samplers sample the input data and generate corresponding outputs (IOUT_PRE, QOUT_PRE, IBOUT_PRE, QBOUT_PRE), which are then transferred to the following SR latches. To enhance sampling performance, a three-stage architecture with a reduced number of MOSFET stacks is adopted. In addition, to improve robustness against the device mismatch, offset cancellation is employed in the sampler [17].

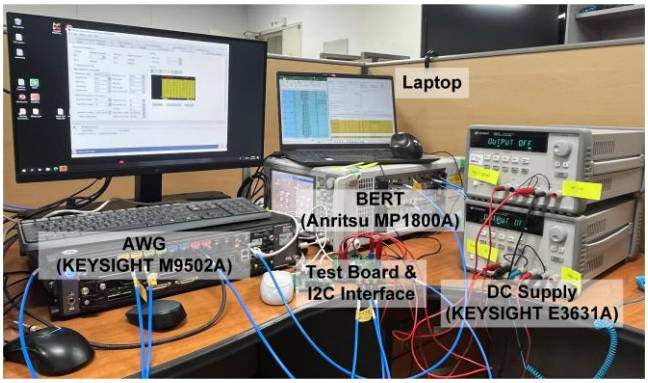
As shown in Fig. 7, the 1-tap direct DFE integrated into the sampler effectively compensates for ISI caused by channel loss by utilizing feedback data from the previous bit. This architecture reduces circuit complexity and power consumption, satisfying the requirements of low-power memory interfaces.

B. Sampler with 1-tap DFE

As shown in Fig. 8(a), the receiver employs a three-stage sampler architecture, where two amplification stages are followed by a cross-coupled regeneration latch. The conventional StrongArm-latch structure, as shown in Fig. 8(b), has been widely utilized for the sampler circuit at RX [18]. The StrongArm latch has the advantage of zero static current. However, it also has two disadvantages. Due to its



(a)



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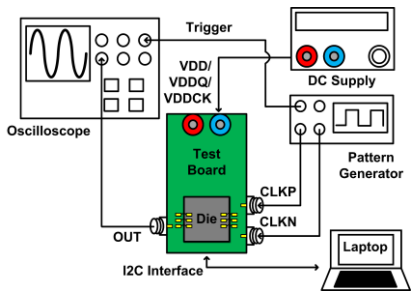
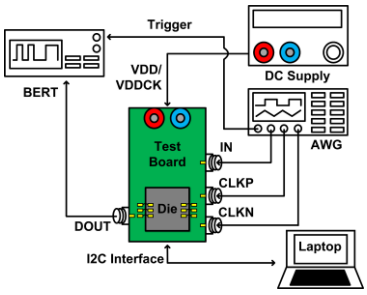


(c)

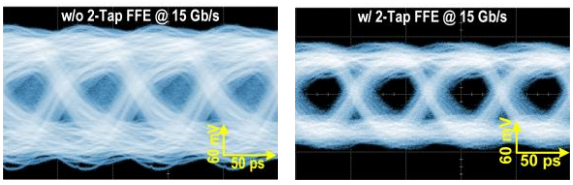


(d)

Fig. 12. Measurement environments of (a) TX and (b) RX and block diagrams for measuring the performance of (c) TX and (d) RX.

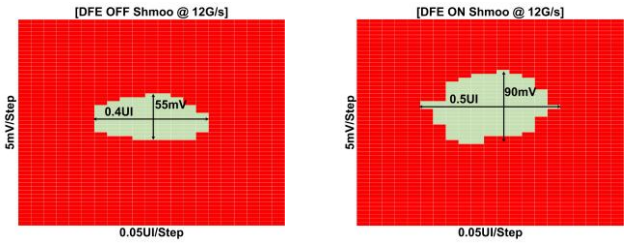
four-transistor stack structure, it suffers from voltage headroom limitation in low-power design. Another disadvantage is that performance is sensitive to the common mode voltage [19], [20].

To overcome these limitations, the design employs a double-tail latch structure, which is more robust to variations in input common-mode voltage [18]. In addition, a reduced transistor stacking structure is applied to alleviate voltage



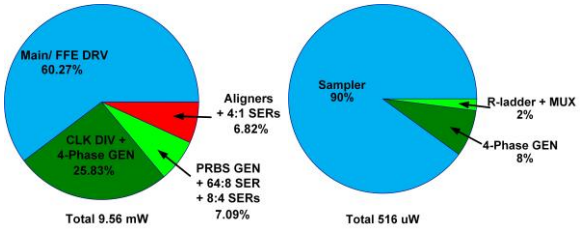
(a) (b)

Fig. 13. TX eye diagrams when 2-tap FFE is (a) turned off and (b) on.



(a) (b)

Fig. 14. RX Shmoo plots when DFE is (a) turned off and (b) on.



(a) (b)

Fig. 15. Power breakdowns of (a) TX and (b) RX.

headroom issues and ensure stable operation in low-voltage environments [9], [19]. As a result, this structure achieves high latch gain and fast decision speed, enabling robust and reliable output generation even at reduced supply voltages.

This sampler structure combines a 1-tap direct DFE to effectively compensate for post-cursor ISI caused by channel attenuation. A 1-tap direct DFE is integrated into each sampler, where it selectively activates either the EQN or EQP transistor based on the previous bit to cancel the ISI. The DFE coefficient is programmed using a 3-bit digital thermometer code (DFE<2:0>), which dynamically adjusts the drive strength of the selected transistor according to the prior decision. The resolution of the DFE weight is 13 mV per bit, resulting in a total range of 39 mV.

C. Offset Cancellation

In the RX, input-referred offset can occur due to device mismatch, degrading the sampling performance. This issue becomes more pronounced in quarter-rate clocking designs, where the number of the sampler increases, and the transistor sizes become smaller [21]. To address this problem, an offset cancellation circuit is connected to the output node of the latch.

Fig. 9 shows the offset voltage distribution at the sampler input, obtained through a 1,000-point Monte-Carlo simulation. The simulation result shows that the proposed sampler has a standard deviation (σ) of 33 mV. To cancel this offset, as shown in Fig. 8(a), the offset cancellation circuit is directly connected to the latch output nodes

Table I. Performance Summary and Comparison.

Reference	*[6]	**[10]	[22]	This Work
CMOS Technology	28 nm	55 nm	65 nm	28 nm
TX Supply [V]	1.0/0.6	N/A	1.0	1.05/0.5
RX Supply [V]	N/A	1.3V	0.9	1.1
TX Data Rate (Gb/s)	15	N/A	10	15
RX Data Rate (Gb/s)	N/A	10.4	10	12
TX FFE	2-tap Pre-emphasis	N/A	N/A	2-tap De-emphasis
RX FFE	N/A	1-tap DFE (asymmetric)	10-tap DFE	1-tap DFE
BER	N/A	10^{-12}	10^{-9}	10^{-9}
TX Energy Efficiency (pJ/bit)	1.35	N/A	1.393	0.64
RX Energy Efficiency (pJ/bit)	N/A	0.16	0.568	0.043
Total Energy Efficiency (pJ/bit)	N/A	N/A	1.961	0.683
TX Area (mm^2)	0.0191	N/A	0.0054	[b]0.0145
RX Area (mm^2)	N/A	[a]0.001	0.0024	[b]0.00746
Total Area (mm^2)	N/A	N/A	0.0078	[b]0.02196

*: with only TX. **: with only RX.
[a]: DFE core only [b]: except CLK buffer

(OUTP_PRE, OUTN_PRE) of each sampler and employs two NMOS transistors configured as MOS capacitors. These transistors are controlled by 2-bit thermometer codes (OFFP<1:0>, OFFN<1:0>) providing 25 mV resolution per bit, resulting in a total offset cancellation range of 50 mV, and are selectively activated to delay the voltage rise at the output nodes. This delay shifts the latch decision threshold, thereby correcting static offset. As a result, the sampler mismatch between samplers is reduced, improving signal integrity. To measure the input-referred offset of each sampler, the INN is fixed at 125 mV while the INP is swept from 0 V to 250 mV. The input voltage at which the sampler output transitions from logic '0' to logic '1' is recorded as the switching point. The input-referred offset is then calculated as the difference between this point and 125 mV.

IV. MEASUREMENT RESULT

Figs. 10 and 11 illustrate the die photographs and area breakdowns of the TX and RX. The TX and RX were fabricated using a 28-nm CMOS process with a core area of 0.0145 mm² and 0.00746 mm², except for the CLK buffer, respectively.

Figs. 12(a), (b), (c), and (d) show the measurement setups and block diagrams to verify the function and performance of the TX and RX. For TX measurement, the eye was measured using an oscilloscope, and for RX, bit error rate (BER) and Shmoo plot were acquired using a BER tester (BERT).

Fig. 13 shows eye diagram comparisons before and after applying 2-tap FFE with the coefficients of '100' at 15 Gb/s. In Fig. 13(a), the eye diagram remains closed without applying FFE. However, as shown in Fig. 13(b), enabling FFE improves signal integrity, resulting in an open eye with a timing margin of 29.25 ps and a voltage margin of 65.4 mV. Additionally, the peak-to-peak amplitude is reduced

due to the de-emphasis effect.

Fig. 14 illustrates Shmoo plots for the RX. To measure BER and obtain the Shmoo plot, the delay of the CLK signal and the reference voltage were adjusted. As a result, the eye size with a BER of 10^{-9} was 0.4 UI horizontally and 55 mV vertically when DFE was turned off, whereas the eye size increased to 0.5 UI horizontally and to 90 mV vertically when DFE was turned on with the coefficients of '111.'

Figs. 15(a) and (b) show the power breakdown of the TX and RX, respectively. The TX consumed 9.56 mW at 15 Gb/s, and RX consumed a 516 uW at 12 Gb/s.

Table I summarizes the performance of our TRX and compares it with other TX and RX designs for low-power memory interfaces. The proposed TX achieves an energy efficiency of 0.64 pJ/bit at a data rate of 15 Gb/s, while the RX achieves an energy efficiency of 0.043 pJ/bit at a data rate of 12 Gb/s.

V. CONCLUSION

In this work, a single-ended NRZ TX and RX for low-power memory interfaces are presented. The TX employs a 2-tap de-emphasis FFE structure and operates at 1.05 V of VDD and 0.5 V of VDDQ, achieving an energy efficiency of 0.64 pJ/bit at a data rate of 15 Gb/s. The RX integrates a 1-tap direct DFE and a three-stage low-voltage sampler with offset cancellation, operating at 1.1 V with an energy efficiency of 0.043 pJ/bit at a data rate of 12 Gb/s.

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