# On-Chip Battery EIS Analog Frontend for Embedded Battery Management System

Byeongho Hwang[1], Yunchae Lee[1], Uikyoung Lee[1], Jihan Shin[2], Kyeongha Kwon[a]
[1]School of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST)
[2]School of AI Semiconductor, Korea Advanced Institute of Science and Technology (KAIST)
E-mail: [1]crovas@kaist.ac.kr

***Abstract* - Electrochemical Impedance Spectroscopy (EIS) is an emerging diagnostic technique for battery characterization. Conventional EIS systems utilize external instrumentation assemblies, limiting their practicality for real-time monitoring applications in electric vehicles (EVs) and energy storage systems (ESS) that require timely impedance data acquisition for operational battery management decisions. This paper presents a novel integrated circuit conforming to AEC-Q100 Grade 1 specifications, operating reliably from -40°C to 125°C, with four measurement channels. The architecture incorporates an on-chip high-pass filter (HPF) for impedance measurement and a zero-temperature-coefficient (ZTC) power supply that maintains stability across the operational temperature range. This integration eliminates the need for external RC components at the HPF stage, thereby reducing system complexity and cost. Post-layout simulation results demonstrate measurement accuracy across various operating conditions. The presented solution enables real-time battery diagnostics and predictive maintenance capabilities, enhancing safety, reliability, and operational lifespan for next-generation embedded battery management systems.**

***Keywords*— Battery Management System (BMS), Electrical Vehicles (EVs), Electrochemical Impedance Spectroscopy (EIS), Zero-Temperature-Coefficient (ZTC) Circuit, Analog Frontend (AFE)**

## I. INTRODUCTION

The rapid growth of electric vehicles (EVs) and energy storage systems (ESS) has increased the deployment of high energy density batteries, elevating new safety challenges. Recent battery fire incidents, possibly attributed to mechanisms such as lithium plating that induce internal short-circuits, underscore the necessity for enhanced battery management systems (BMS) [1]. Conventional BMS solutions monitor fundamental parameters including voltage, current, and temperature to diagnose battery conditions and perform essential state estimations (State of Charge; SOC, State of Health; SOH, State of Power; SOP). However, these external measurements provide insufficient insight into internal degradation processes, limiting their effectiveness for early detection of critical failure mechanisms.

Electrochemical impedance spectroscopy (EIS) enables detailed characterization of battery internal states through frequency-dependent impedance analysis. This method applies sinusoidal current signals to series-connected cells and measures the corresponding voltage responses, particularly within the critical sub-1kHz frequency range [2]. EIS reveals essential electrochemical parameters including charge transfer resistance, double layer capacitance, and solid electrolyte interphase properties that remain undetectable through conventional measurement techniques [3].

However, implementation of EIS in practical EV battery modules presents significant technical challenges for accurate impedance data acquisition under automotive operating conditions. The high-voltage environment of series-connected battery modules necessitates robust power management and precise current control [4]. Measurement precision requirements remain difficult to achieve within AEC-Q100 Grade 1 (-40°C to 125°C).

This paper presents a novel integrated circuit architecture that addresses these challenges through specific design innovations. The system incorporates a precise current excitation stage, a low-noise voltage sensing circuit, and a zero-temperature-coefficient (ZTC) power supply stage to achieve accurate impedance measurements. The current excitation stage utilizes a digital-to-analog converter (DAC) and current driver to generate single-frequency sinusoidal signals with high accuracy, operating in the 7–70 mA range, significantly lower than typical excitation currents exceeding 1A. The voltage sensing circuit features a high-pass filter (HPF) with a low cutoff frequency of 0.615 Hz and an analog multiplexer (AMUX) optimized for on/off resistance (Ron/Roff). Additionally, the ZTC circuit employs piecewise linear compensation to ensure stable operation across the -40°C to 125°C temperature range [5], [6]. The proposed solution demonstrates the feasibility of miniaturizing EIS functionality for potential integration into embedded BMS.

a. Corresponding author: Kyeongha Kwon(kyeongha@kaist.ac.kr)

Manuscript Received Apr. 08, 2025, Revised Jul. 28, 2025, Accepted Aug. 22, 2025

## II. CIRCUIT IMPLEMENTATION

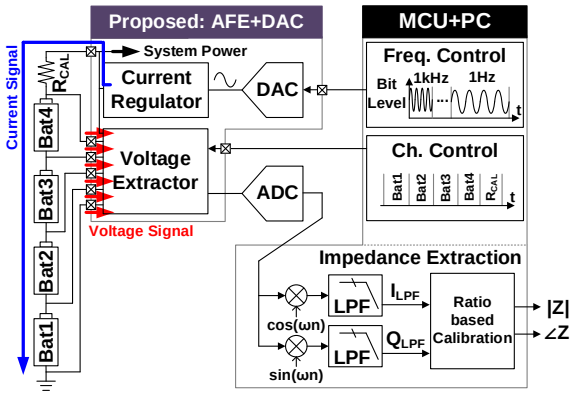



Fig. 1 Overall functional diagram of the proposed system

Figure 1 illustrates the architecture of the proposed EIS system, which comprises an analog frontend (AFE) with a current regulator and voltage extractor, as well as a microcontroller unit (MCU) and a PC for system control and management. The system incorporates a precision calibration resistor ($R_{CAL}$) which eliminates the need for an external current sensor. $R_{CAL}$ is implemented using a low temperature coefficients resistor, ensuring minimal variation across the -40°C to 125°C. During measurement, the perturbation current from the current regulator flows through both the battery and $R_{CAL}$, generating the corresponding terminal voltages. The frequency sweep control, managed by the MCU and PC components, operates across a range from 1kHz to 1Hz to control the DAC and current regulator. The extracted voltage signals undergo digital processing where they are multiplied by orthogonal reference signals at perturbation frequency, then passed through low-pass filters. A ratio-based calibration technique subsequently determines the magnitude and phase, enabling accurate extraction of battery impedance $Z_{BAT}$ by comparing against the known $R_{CAL}$ characteristics. This approach enables accurate impedance determination across the frequency spectrum while maintaining measurement precision throughout the operating range.

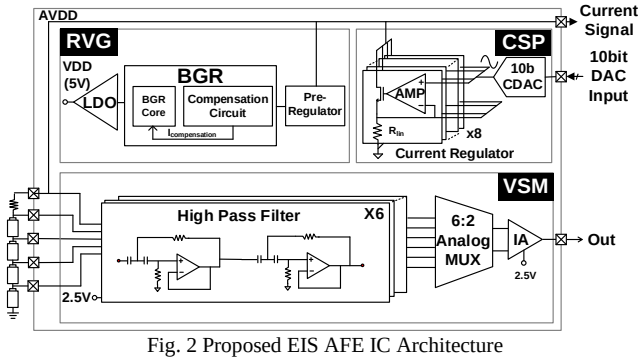



Fig. 2 Proposed EIS AFE IC Architecture

The AFE incorporates three primary components including the reference voltage generator (RVG), the current signal perturbator (CSP), and the voltage signal measurement (VSM) unit, as shown in figure 2. The RVG steps down a cell top voltage to a stable 5V level, facilitating IC-level operation in a high voltage environment typical of EV and ESS applications. The circuit incorporates advanced temperature compensation technology that maintains voltage stability across the entire operating range. This design ensures precise reference voltage performance within the AEC-Q100 Grade 1 automotive temperature requirements.

The CSP integrates a DAC and a linear amplifier-based current regulator. This unit receives frequency control signals from the MCU and generates a precision sinusoidal current perturbation with controlled amplitude and frequency characteristics. Additionally, the system applies a well-defined DC bias current combined with the AC perturbation signal to generate the appropriate test current for the battery.

Meanwhile, the VSM unit incorporates six high-pass filters (HPFs), a 6:2 analog multiplexer (AMUX), and an instrumentation amplifier (IA) with adjustable gain through external resistors. The HPF block consists of a 4th order Sallen-Key HPF network that effectively blocks DC offset voltages from the measurement path. After filtering, a 6:2 AMUX selects the isolated AC voltage signals and routes them into a shared IA block. This arrangement allows for selective measurement of multiple battery cells or modules with high common-mode rejection and minimal noise interference.

### *A. Zero-temperature Coefficient (ZTC) Power Supply*

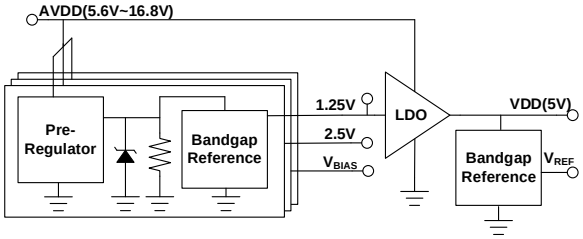



Fig. 3 Proposed RVG Block Diagram

Figure 3 depicts a proposed RVG that consists of a pre-regulator, bandgap reference (BGR), and low dropout (LDO). The pre-regulator converts high input voltages to an intermediate 5V level suitable for subsequent regulation stages. A temperature-compensated BGR circuit implements advanced second-order piecewise linear compensation to ensure voltage stability across temperature fluctuations. The LDO uses this precision reference voltage from BGR to generate stable supply voltages with minimal temperature coefficients, ensuring consistent power delivery to all system components under varying environmental conditions. For a 2.5 V supply, it serves as the bias for the high-pass filter.

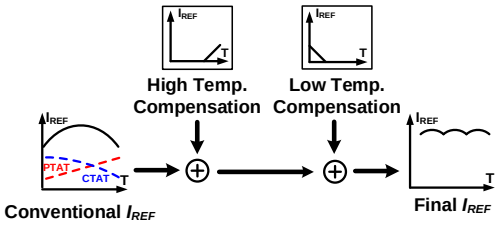



Fig. 4 Principle of Temperature Compensation of BGR

Figure 4 indicates that the BGR utilizes a principle where temperature compensation is achieved by applying both high temperature and low temperature compensation to the basic reference current $I_{REF}$. The BGR provides stable voltage references independent of supply voltage and temperature fluctuations by combining PTAT and CTAT currents through a reference resistor $R_{REF}$. In the BGR core, the base-emitter voltage of BJTs exhibits nonlinear temperature dependence, creating a concave-upward temperature-voltage characteristic curve with performance degradation at extreme temperatures. Second-order piecewise linear compensation effectively addresses this nonlinearity through dual compensation structures that activate separately at low and high temperatures. The superposition of these compensation currents into the $R_{REF}$ maintains voltage stability across an extended temperature range.

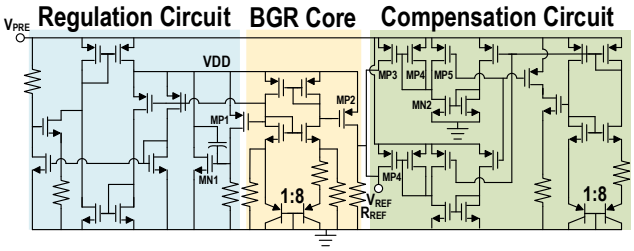



Fig. 5 Schematic of Proposed BGR

The schematic of the proposed BGR is shown in figure 5. The low-temperature compensation circuit comprises transistors MP3, MP4, MP5, and MN2, with PTAT & CTAT generator controlling their gate voltages to establish the current relationship $I_{MN2} = I_{MP5} + I_{MP4}$. During high-temperature operation, MN2 current decreases while MP5 current increases, effectively deactivating MP4. Conversely, at low temperatures, MN2 current increases while MP5 current decreases, enabling substantial current through MP4. This temperature-dependent modulation ensures MP3 conducts only at low temperatures, generating the required compensation current. The high-temperature compensation circuit operates inversely, with MP6 generating its compensation current. Both currents flow through $R_{REF}$, compensating for voltage variations across the operating range to maintain stable BGR output.

Power supply rejection ratio (PSRR) is crucial since pre-regulator voltage sources may demonstrate instability. Conventional BGR architecture exhibits inadequate PSRR due to noise propagation through MP transistors. Implementation of a regulation circuit incorporating negative feedback via transistors MN1 and MP1 effectively attenuates VDD fluctuations in the bandgap core, significantly enhancing PSRR performance.

*B. Current Signal Perturbator*

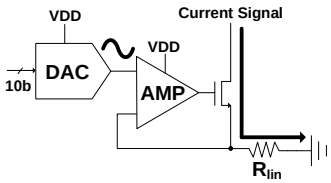



Fig. 6 Schematic of Current Regulator

Figure 6 presents a brief schematic of the current regulator. The current perturbation unit receives digital signals from the MCU and applies well-defined frequency sinusoidal current to the battery. 10-bit CDAC converts digital signals to analog voltage, then transforms voltage to current through negative feedback comprising an op-amp, high-voltage DMOS, and resistor, where $I = V_{DAC}/R$. To mitigate thermal issues, the design implements eight parallel operational amplifier-MOSFET pairs rather than a single MOSFET, with drain of each DMOS transistor connecting directly to the battery to deliver precisely controlled excitation current for impedance measurement.

*C. Voltage Signal Measurement Unit*

The VSM unit consists of an HPF stage, AMUX stage, and IA stage.

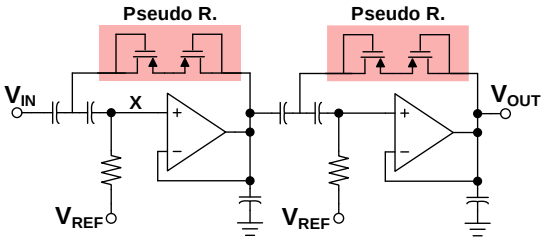



Fig. 7 Schematic of 4th order Sallen-Key HPF

The HPF stage consists of six HPF units, with their schematic presented in figure 7. To achieve effective noise suppression, the system implements an HPF with a cut-off frequency below 0.4Hz. The HPF eliminates DC components to extract impedance from AC signals, with a cutoff frequency set at 0.4Hz to ensure the minimum frequency signal of 1Hz remains undistorted. While conventional RC filter solutions would require impractically large components (>80MΩ resistors and 10nF capacitors) that present significant challenges for IC integration, the design employs a 4th order Sallen-Key topology with pseudo resistors to significantly reduce silicon area requirements while maintaining filtering performance. This approach enables the implementation of extremely low cut-off frequencies in an integrated circuit format without compromising system sensitivity or measurement accuracy.

The AMUX stage is constructed using transmission gates, while the IA adopts a conventional three-stage amplifier structure.

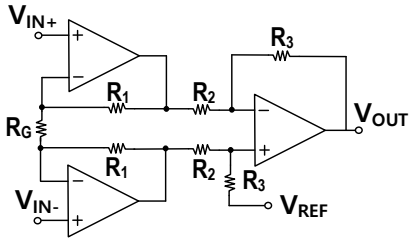



Fig. 8. Schematic of Instrumentation Amplifier

As shown in Figure 8, the IA amplifies battery AC signals following high pass filtering and analog multiplexing. Composed of three amplifiers with resistors RG and R1-R3, the IA maintains high input impedance ensuring signal integrity. Amplification adheres to the relationship $V_{OUT}/V_{IN} = (1+2R_1/R_G)\cdot(R_3/R_2)$. The single output terminal connects to an external ADC for signal digitization and analysis.

## III. RESULTS AND DISCUSSIONS

### *A. Chip Micrograph*

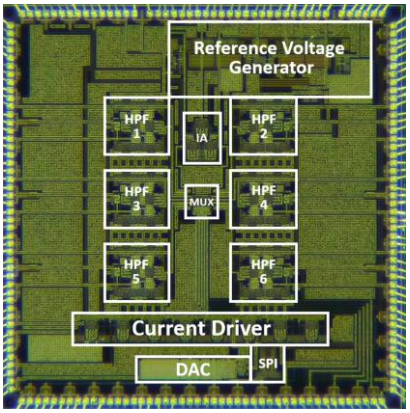
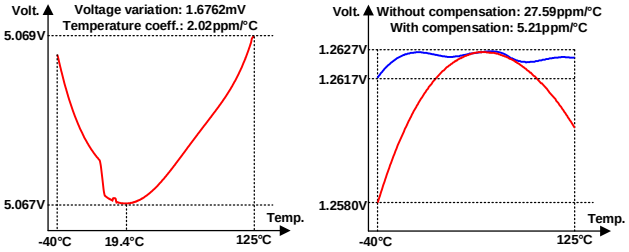



Fig. 9 Chip micrograph

The proposed IC has been implemented using TSMC 180 nm BCD process technology. The total die area measures 5mm by 5mm. As shown in the chip micrograph in figure 9, the EIS IC comprises the RVG, CSP, VSM unit and SPI interface.

### *B. Post-layout Simulations*

Post-layout simulations confirmed the operational stability of key AFE blocks over the AEC-Q100 Grade 1 temperature range. This study focused on the on-chip AFE's circuit design and simulation, demonstrating EIS capabilities including 1Hz low-frequency sweeps. While simulations suggest the potential for accurate impedance extraction, experimental validation of EIS measurement accuracy using fabricated ICs is planned for future work. The main contribution of the paper is the successful design and simulation of a compact, integrated AFE for embedded BMS, covering the critical low-frequency EIS spectrum.




(a) (b)

Fig. 10 (a) Temperature Coefficient of Reference Voltage Generator (b) Comparison of with and without compensation in BGR circuit

Figure 10(a) shows the simulation result of the LDO output of RVG in the temperature range of -40 to 125°C. The reference voltage of 5V exhibits a temperature variation of approximately 1.6762mV, with a temperature coefficient of about 2.02ppm, demonstrating a low variation. The implementation of a compensated BGR circuit enables this voltage regulation across the entire operational temperature range. Figure 10(b) compares the bandgap reference (BGR) performance with and without temperature compensation. Prior to compensation, the BGR exhibited a temperature coefficient of 27.59 ppm/°C, which was significantly reduced to 5.21 ppm/°C after the compensation was applied. Herein, the simulated PSRR was significantly improved from an existing 14.71dB to 85.77dB.

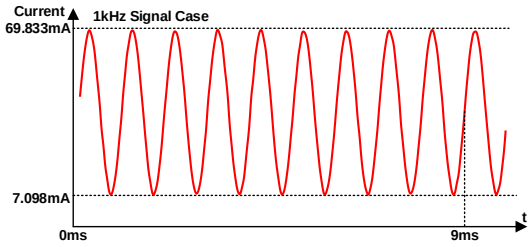
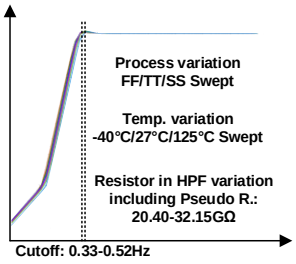
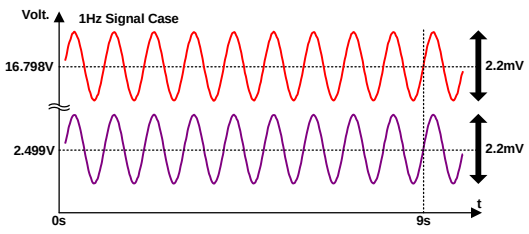



Fig. 11 Waveform of sinusoidal perturbation current




(a)




(b)

Fig. 12. (a) HPF Cut-off Frequency Response, (b) HPF Input and Output Transient Response

Fig. 11 shows the waveform of sinusoidal perturbation current in 1kHz case. The current delivered to the battery and $R_{CAL}$ ranges from 7 to 70mA. Minimizing the excitation current ensures linear-region operation of the battery, reduces thermal issues. The signal applied to the impedance model of a cylindrical cell with a resistance of 35mΩ produced subsequent voltage responses.

Figure 12(a) demonstrates that the HPF cut-off frequency stabilizes at 0.33-0.52Hz when swept across the process and temperature range of -40 to 125°C. The result shows 20.40-32.15GΩ variation in high-pass filter resistance, including the pseudo resistor. This value incorporates all resistors in the 4th-order Sallen-Key HPF. This enables effective elimination of noise in the low frequency band. Figure 12(b) shows the transient response graph of the HPF input and output when a 1Hz signal is applied. With a DC level of 16.8V at the HPF input, the 2.2mV input swing is accurately preserved at the output with a DC level of 2.5V. This confirms effective level shifting of high voltage signals to match the ADC input voltage range.

## IV. CONCLUSION

This paper has presented an integrated circuit design for EIS implementation in embedded BMS. The proposed architecture addresses key challenges of EIS integration through three main functional blocks: a temperature-compensated reference voltage generator with 2.02ppm coefficient, a precision current perturbation unit operating in the 7-70mA range, and a low-frequency voltage sensing circuit with 0.52Hz cut-off frequency.

The system enables frequency sweep control from 1Hz to 1kHz, which facilitates comprehensive Nyquist plots for estimating battery internal state parameters. The design successfully enables high-voltage battery impedance measurements while meeting AEC-Q100 Grade 1 temperature specifications (-40℃ to 125℃).

By minimizing excitation current and implementing area-efficient filtering techniques, the system achieves accurate impedance measurement capabilities within form factors suitable for automotive applications. The demonstrated performance validates the feasibility of integrating EIS functionality into embedded BMS.

## ACKNOWLEDGMENT

The authors would like to thank IDEC to participate HM-2303 MPW process for fabricating the proposed EIS IC. This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT; RS-2023-00278995, and BK21) and Institute of Information & communications Technology Planning & Evaluation (IITP) under the Graduate School of Artificial Intelligence Semiconductor(IITP-2025-RS-2023-00256472) grant funded by the Korea government(MSIT).

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**Byeongho Hwang** received the B.S. degree, in 2022, and the M.S. degree in 2024. He is currently pursuing the Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. His research interest includes power management circuits for battery management system (BMS). Especially, he is currently conducting research on battery monitoring IC (BMIC) design and hardware design in electrochemical impedance spectroscopy (EIS) system.

**Yunchae Lee** received the B.S. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2023. He is currently pursuing the master's degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. His research interest includes

sensing circuits for battery management system (BMS). Especially, he is currently conducting research on battery monitoring IC (BMIC) design and hardware design in electrochemical impedance spectroscopy (EIS) system.

**Uikyoung Lee** received the B.S degree in Electrical and Electronic Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2024. His research interest includes battery management systems (BMS). He is currently conducting research on battery monitoring IC (BMIC) and hardware board development to accurately estimate battery state of charge (SOC) using AI.

**Jihan Shin** received the B.S. degree in electrical engineering from Yonsei University, Seoul, South Korea, in 2024, and is currently conducting his M.S. research at KAIST. His research interest includes analog front-end circuits for battery management systems (BMS), especially battery monitoring IC (BMIC) design, and he is also working on designing Electrochemical Impedance Spectroscopy (EIS) systems to estimate the State of Charge (SOC) and State of Health (SOH) of batteries.

**Kyeongha Kwon** received the Ph.D. degree in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2018. From 2018–2020, she was with the Center for Bio-integrated Electronics (CBIE) at Northwestern University, IL, USA, as a postdoctoral researcher. Since 2020, she has been with the Faculty of Electrical Engineering, KAIST, where she is currently an associate professor. Her research interests span a wide range of topics in wireline communication, bioelectronics, and battery management system. She is an active Technical Program Committee (TPC) Member of IEEE ISSCC and IEEE CICC. She has served as the Country Representative of South Korea for the ISSCC Far-East Region in 2024.