# Four-Phase Always Quadra-Path Hybrid DC-DC Converter with Output Capacitor Free

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***Abstract*** **- This paper presents a four-phase always quadra-path (AQP) DC–DC converter designed to achieve high power density and power conversion efficiency with low output ripple. The proposed architecture consists of one inductor path and three capacitor paths operating in a time-interleaved manner to collectively deliver the output current. This structure reduces the inductor's DC current stress, enabling the use of a compact inductor without sacrificing efficiency or transient performance. The converter supports an output voltage range of 0.3–2.0 V from a 5 V input supply, making it suitable for battery-powered and low-voltage SoC applications. The hybrid current delivery through capacitive and inductive paths improves transient response and ripple suppression. Measurement results show a peak power conversion efficiency (PCE) of 74% and a maximum load current of 2 A. The converter is implemented in a TSMC 180 nm BCD process, occupying a 3 mm × 3 mm (9 mm²) silicon area.**

***Keywords***— **Hybrid DC–DC converter, multi-path, step-down converter.**

## I. INTRODUCTION

Over the past years, Internet of Things (IoT) technologies have been advanced to conduct multiple operations with limited hardware resources. To support the high performance of end nodes in IoT applications, increased memory usage has been introduced recently. This trend requires the power management integrated circuit (PMIC) to provide a fast transient response and minimal ripple with high efficiency.

Single inductor-based Hybrid DC–DC converters have been widely studied because of their wide output voltage range with high efficiency [1], [2], [3], [4], [5], [6], [7], [8]. Although these single-inductor-based Hybrid DC-DC converters require a large area and slow load transient response, the converters achieve a wider range than switched capacitor (SC) converters and LDO regulators. In particular, hybrid converter architectures are suitable for systems that demand both wide voltage programmability and high current delivery capability. Therefore, a Hybrid DC-DC converter with a fast transient response is a key component for implementing the DRAM to have high energy efficiency.

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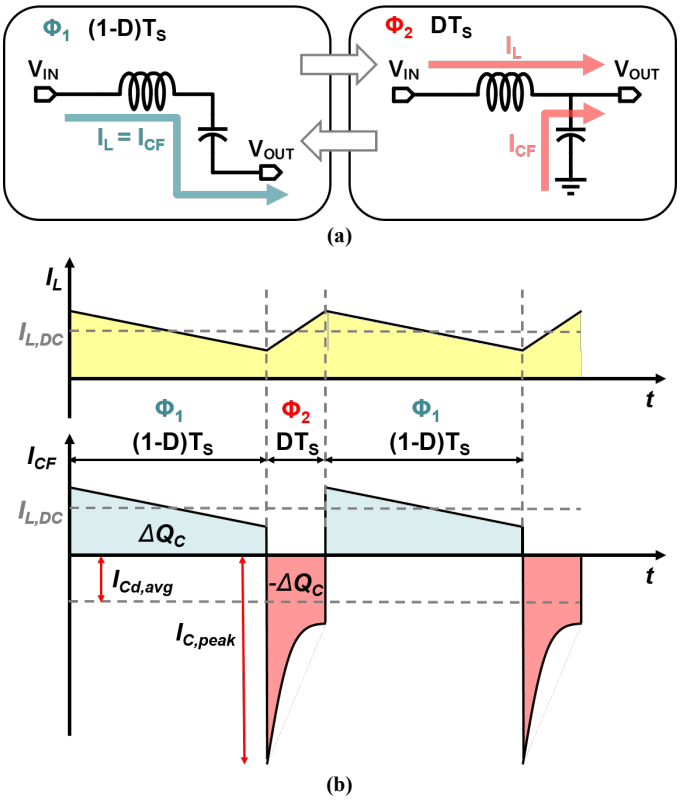



Fig. 1. Dual path Hybrid DC-DC Converter: (a) Operation topology and (b) inductor current and flying capacitor current graph. [8].

## II. EXPERIMENT

### *A. Prior Works*

Recently, for reduced inductor DC resistance (DCR) loss and switch stress, dual-path (DP) (or multi-path)-based hybrid buck converters have attracted great research interests in the applications of compact systems using small-size inductors. Existing topologies often exhibit a fundamental trade-off between the reduction of inductor DC current ($I_{L,DC}$) and the control of the averaged flying capacitor (CF) discharging current ($I_{Cd,avg}$). As shown in Fig. 1, effective $I_{L,DC}$ minimization are achieved through sufficient CF charging duration in DP-based converters. However, a reduced discharging period, particularly when the duty cycle (D) approaches 0 or 1, precipitates a marked increase in $I_{Cd,avg}$ inrush. This surge leads to significant

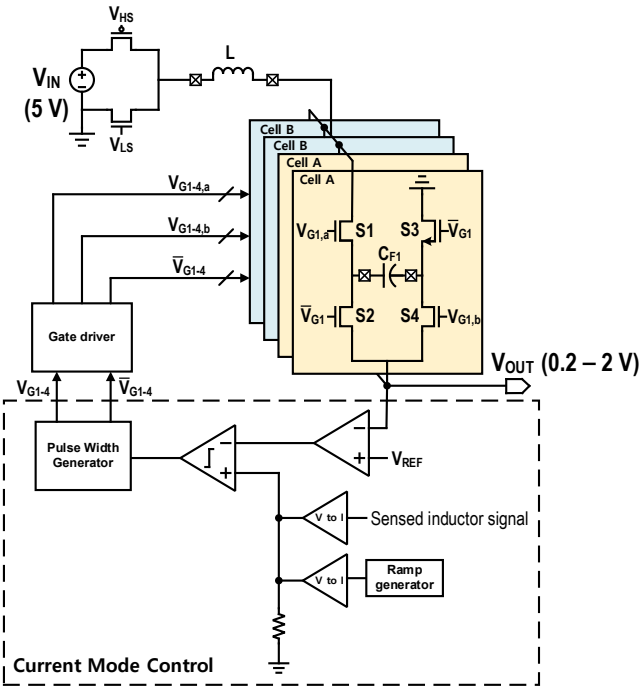



Fig. 2. Proposed AQP Hybrid DC-DC Converter top diagram.

conduction losses, necessitates a higher peak-current handling capability, contributes to substantial output ripple, and exacerbates electromagnetic interference (EMI).

*B. Proposed Work*

Fig. 2 shows the top block diagram of the proposed always quadra path (AQP) DC-DC converter. The proposed converter includes one off-chip inductor and four off-chip capacitors in the power stage. It basically operates in four phases: Φ1, Φ2, Φ3, and Φ4. During the four-phase operation, the output current is delivered through one inductor path and three capacitor paths. To increase CF-assisted energy transfer with its high continuity, the proposed ADP converter charges and discharges the four flying capacitors alternatively during each phase. $C_{F1}$ is charged by the inductor current at $\Phi_1$ and discharged other three phases. And the other three flying capacitors follow the same operation. Accordingly, the inductor is charged with the voltage of $V_{IN} - 2V_{OUT}$ during $\Phi_1$ and $\Phi_3$, and discharged with $2V_{OUT}$ during $\Phi_2$ and $\Phi_4$. Based on the voltage-second balance of the inductor, the voltage conversion ratio (VCR) is given by D/2, where the duty cycle is D. Fig. 3 shows the operation in each phase and the charge and discharge behaviors of the flying capacitors. Accordingly, the inductor current and the three flying capacitor currents are the drive output nodes. For the flying capacitors' charge balancing, this system satisfies the following equation.

$$\Delta Q_{CF1,3} = I_{L,DC} \cdot (1-D)T = I_{CF1,3} \cdot (1+D)T \quad (1)$$

$$\Delta Q_{CF2,4} = I_{L,DC} \cdot DT = I_{CF2,4} \cdot (2-D)T \quad (2)$$

$$\therefore\ I_{L,DC} = \frac{1}{2} I_{out}\ (0 \le D \le 1) \quad (3)$$

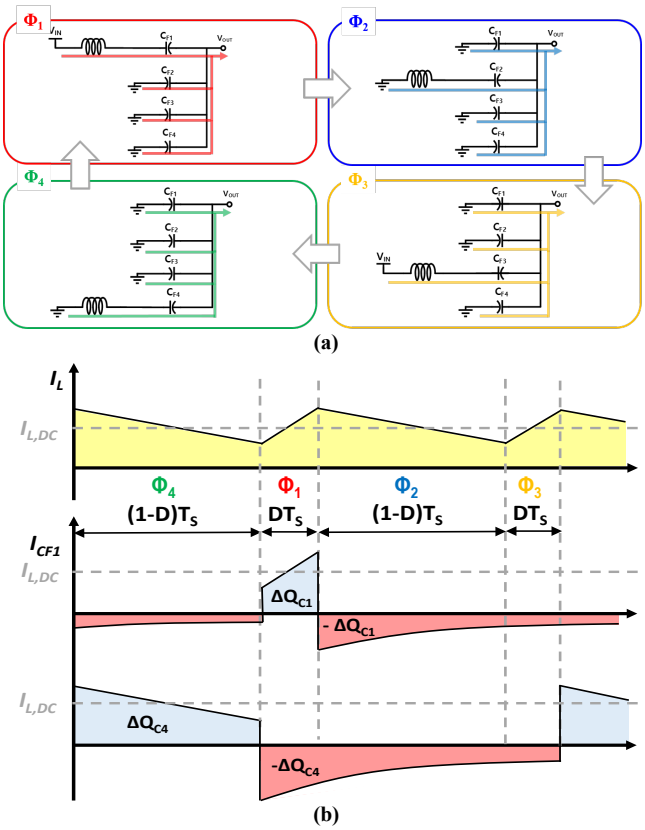



Fig. 3. Proposed AQP Hybrid DC-DC Converter : (a) Operation topology and (b) inductor current and flying capacitor current graph.

Equation (3) shows that $I_{L,DC}$ is always equal to 1/2 $I_{Load}$. When supplying such a heavy $I_{Load}$ into a small $R_{Load}$ (with low VDD), the efficiency degradation in the DC—DC converter is mainly due to conduction loss ($I_{Load}^2 \times R_{Loss}$), where the equivalent $R_{Loss}$ is typically composed of the power switch's $R_{ON}$ and inductor's DCR ($R_{DCR}$). Moreover, the use of chip inductors has a large $R_{DCR}$ (>> $R_{ON}$). It means reducing $I_L$ decreases efficiency loss. In the proposed circuit system, since the average inductor current is less than 1/2 $I_{out}$, it results in a quarter of less energy loss compared to conventional systems.

Moreover, this topology solves prior work issues, which inrush current flowing through the capacitor. Each operates in an interleaved manner with opposite phases, significantly extending the CF discharge intervals from $DT_S$ to $(1+D)T_S$ or from $(1-D)T_S$ to $(2-D)T_S$, while maintaining the inherent charging dynamics of the CF. This adjustment leads to a marked reduction in the $I_{Cd,avg}$, positioning it substantially below the inductor DC current ($I_{L,DC}$) as D approaches zero. This system operation obviates the dependency on extensive power switches and metallization within the conduction pathway, a prevalent issue in DP-based topologies.

From the presentation in Fig. 3(a), it is apparent that the proposed topology offers a significant diminution in $I_{Cd,avg}$ and augments the efficiency of power-stage conduction, particularly as D nears 0 or 1, in stark contrast to extant methodologies. An additional merit of this topology is its capability to facilitate $C_{OUT}$-free functionality across the full spectrum of load conditions. The proposed topology ensures that three flying capacitors are connected to the output node across all phases, and two flying capacitors remain connected even during dead time,

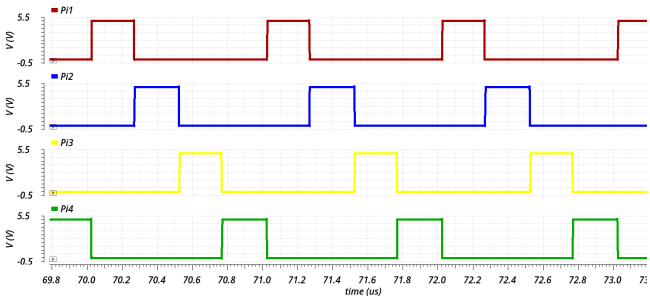
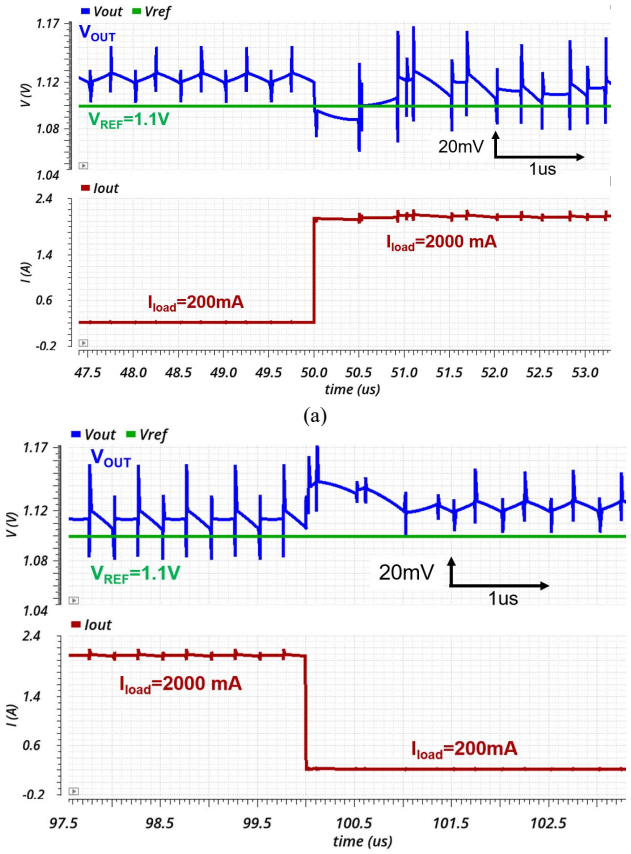



Fig. 4. Simulated waveforms of 4 Phase signal.




(a)




(b)

Fig. 5. Simulated transient response waveforms of load transient (a) light to heavy and (b) heavy to light.

thereby enabling Cout-free.

Fig. 4 Shows simulated waveforms of each four phases signal at $V_{REF}$ =1.1 V. Each phase is arranged sequentially without overlap.

## III. RESULTS AND DISCUSSION

Fig. 5 shows a simulated $V_{OUT}$ and $I_{Load}$ waveform of the load transient. Fig. 5(a) illustrates the transition from light ($I_{Load}$ = 200 mA) to heavy ($I_{Load}$ = 2 A) load, and Fig. 5(b) shows the transition from heavy to light load. The simulation results reveal that the settling time is less than 5 μs in both cases. Furthermore, despite being Cout-free, it is observed that both overshooting and undershooting are significantly small. Three flying capacitors operate similarly to an output capacitor across all phases during the load transient response. The flying capacitor connected to the output node delivers

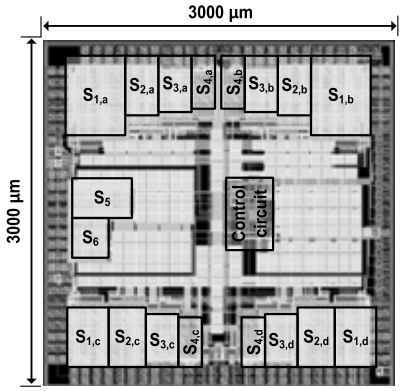



Fig. 6. Chip layout

current to the output until the $I_L$ settles into steady state, enabling fast recovery from the under/overshoot.

Fig. 6 presents the floor plan of the proposed AQP hybrid DC–DC converter. To accommodate high load current, the power switches are designed with a sufficiently large size. These switches are strategically placed along the pad lines to minimize the length of the power delivery metal traces, thereby reducing parasitic resistance and enhancing overall power conversion efficiency.

To achieve an optimal trade-off between conduction loss and switching loss, the dimensions of the power transistors are carefully optimized to minimize total energy loss. The control circuitry is centrally located within the chip layout to shorten the routing paths of control signals toward the power stage, which improves signal integrity and response time. Additionally, the phase generator block, implemented in digital logic, is positioned and designed with attention to timing alignment between the control circuitry and the corresponding switching cells. The total layout area of the implemented design is approximately 9 mm².

## IV. CONCLUSION

TABLE I. Comparison with state-of-the-art multi-path hybrid DC–DC converters

| | TCAS1'22 [5] | TPEL'24 [6] | ISSCC'22 [7] | VLSIC'21 [8] | This work |
|---|---|---|---|---|---|
| Technology [nm] | 65 | 130 | 65 | 180 | 180 |
| Topology | Tri-path | ADPR | CPL | ADP | AQP |
| $V_{IN}$ [V] | 3.3–4 | 2.8–4.2 | 3–4.2 | 3.4–4.5 | 5 |
| $V_{OUT}$ [V] | 0.7–1 | 0.9–1.1 | 0.6–0.8* | 0.3–1.7 | 0.7–1.8 |
| VCR | D/(1+2D) | D/(1+2D) | D/(1+2D)* | D/2 | D/2 |
| $I_{L,DC}/I_{OUT}$ @VCR = 0.2 | 0.5 | 1/(1+2D) | 1/(1+2D) | 0.5 | 0.5 |
| $F_{SW}$ [MHz] | 5 | 1 | 2 | 1 | 1–2 |
| Inductance [μH] | 1 | 4.7 | 0.47 | 4.7 | 1 |
| $C_F$ [μF] | 2×0.47 | 2×4.7 | 2×4.7 | 2×10 | 4×10 |
| $C_{OUT}$ [μF] | 1 | NR | 10 | 10 | - |
| Peak Efficiency [%] | 84 | 95.4 | 92.9 | 91.5 | 74.1 |

* Performance of sub-1/3X mode is included

Table I presents the summarized specifications of the proposed single inductor-based Hybrid DC-DC converter. The power stage is composed of one inductor and four flying capacitors. The proposed AQP reduces the inductor current, so it reduces energy loss. Moreover, this approach ensures

that three flying capacitors are connected to the output node across all phases, and two flying capacitors remain connected even during dead time, thereby enabling $C_{OUT}$-free. As a result, the converter achieves a wide output voltage range and fast load transient.

## ACKNOWLEDGMENT

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