Isolated Multi-Cell Single-Path Battery Management System for Electric Vehicle Batteries

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***Abstract* - A Battery Management System (BMS) is essential for monitoring battery voltage and maintaining balance in high-voltage environments. This study applies an indirect measurement approach using an isolated structure, where LEDs are used for voltage sensing and balancing. In order to monitor the accurate voltage even in the PVT environment, the multiple battery voltages were monitored with a multi-cell single path structure, and an internal reference voltage was generated to ensure the monitoring result compensated for temperature, even with battery temperature changes. BMS executes to get cell monitoring and reference voltages in one output port while performing temperature compensation, and independently, the cell-by-cell register operation method allows simultaneous balancing of multiple cells. As a result of the design, the voltage resolution within +/-5mV from -20 degrees to +80 degrees was secured, and the balancing operation was secured at more than 20mA. This allows the battery voltage monitoring and cell balancing to be stable with the proposed isolated circuit structure in high-voltage environments.**

***Keywords*— Battery management system (BMS), cell monitoring, balancing, isolated structure, photo, resolution.**

I. INTRODUCTION

With the acceleration of electric vehicle (EV) adoption, Battery Management Systems (BMS) have established themselves as key technologies for safety and efficient energy management. BMS monitors the voltage of each battery cell in real time to prevent risks such as overcharging, deep discharge, and thermal runaway, thereby ensuring the battery's lifespan and safety [1], [2], [3], [4], [5], [6], [7]. Importantly, electric vehicle batteries are composed of thousands of cells, and voltage imbalances among these cells can lead to overloading and thermal runaway in some cells, which has been identified as a major cause of EV fires [1]. Traditional BMS operated by directly connecting the battery cells to control circuits to measure voltage, but applying voltage directly to control circuits operating at low voltage (below 5V) in high voltage environments (over 1,000V) poses risks of circuit damage and malfunction [5,6]. Hence, there is a need for indirect measurement technologies that physically isolate the battery cells from low-voltage control boards, and a proposal has been made to implement this via an LED-based optical signal conversion method. However, existing methods using multiple LEDs have resulted in voltage sensing errors per cell (approximately 5mV) due to differences in manufacturing processes and temperature characteristics [2], [3]. In another study, individual battery cell voltages are sequentially selected and monitored by measuring the voltage differences between adjacent analog inputs (e.g., VIN1 − VIN0, VIN2 − VIN1, etc.) via a multiplexer. The ADC driver converts the battery signal, which is input in a single-ended format, into a fully differential signal, ensuring high linearity and low noise performance. Furthermore, by integrating an LDO (Low Dropout Regulator) and a PTAT (Proportional To Absolute Temperature)-based temperature compensation circuit, a stable bandgap reference voltage is generated regardless of temperature variations [8]. In addition, balancing technologies that minimize voltage differences between cells are essential for the stable operation of BMS. Commercially available balancing solutions (such as NXP's BMA7318/BMA7518) offer passive or active balancing, but limitations of direct connection methods result in heat generation and power consumption issues [9]. Previous studies have proposed a method of parallel connection of two semiconductor devices to achieve passive balancing (<8Ω, 80mW) using 14 cells, as well as a design utilizing two MOSFETs to implement normal, bypass, and balancing modes. Moreover, designs employing switches for connecting cells or modules in series, and active balancing structures using inductors and switches, have been proposed, yet issues with high voltage and high current have not been resolved [10], [11], [12], [13]. Recent studies have suggested advanced solutions, such as a Li-ion battery switching charger employing a three-level DC-DC buck converter with a loop-free auto-calibration technique, significantly improving efficiency and reliability [14]. This paper proposes a single-path multi-cell voltage monitoring and balancing system utilizing LED-based indirect measurement techniques and an isolation structure based on the above precedents. The proposed system employs high-resolution reference voltages (REF_V) created by partitioning from 4.2V to 3.2V into 15 steps, compensating for voltage errors due to temperature variations and component imbalances. It also enables safe cell balancing even in high-voltage environments through an isolated balancing circuit and implements safe operation by completely separating high-

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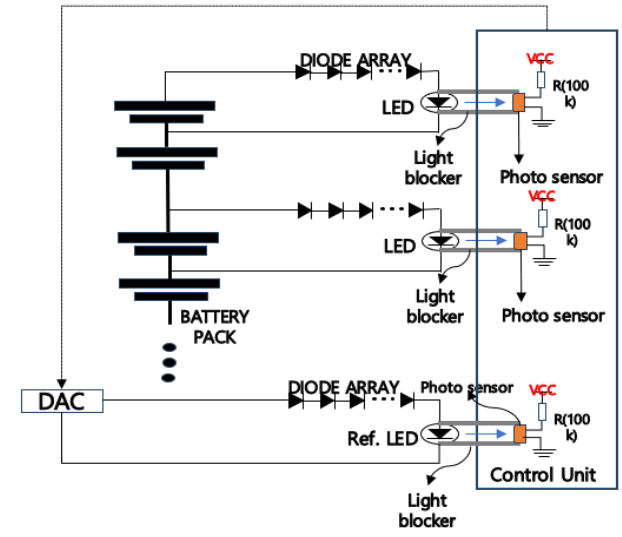
voltage and low-voltage circuits through photodiode-based signal transmission.

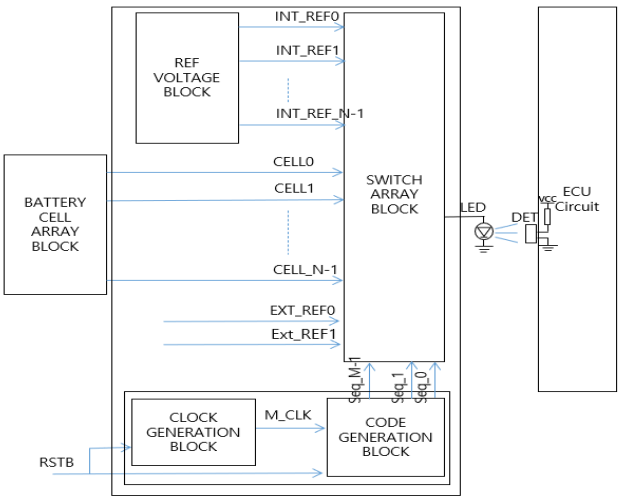
II. DESIGN METHODOLOGY

A. Multi-Cell Single-Path BMS Design

Fig. 1 (a) shows the previous study of measuring each battery cell voltage with each LED using an LED and a photosensor to isolate the high-voltage part and the low-voltage part. The problem in the previous study is that each LED has different characteristics and cannot be accurately measured the voltage when monitoring the voltage. In this study, a structure to monitor the voltage of several battery cells through a single path, shown in Fig. 1 (b), was proposed and designed. This design sequentially selects the voltage values and reference voltages of the battery cells and outputs the selected signals through a single path to reduce errors and enable accurate monitoring. The main components and operating principles are as follows.



(a)



(b)

Fig. 1. Proposed isolation battery voltage monitoring structure; (a) Previous work BMS (b) Proposed BMS (Single-Path Multi Cell)

The reference voltage and the battery cell voltage are input from the ref voltage block and the battery cell array block, respectively. The code generation block controls the selection of a specific battery cell voltage or reference voltage by sequentially generating signals. The selected signal is delivered via a single output path via a switch array block, amplified by an OPAMP, and finally outputted as monitoring data. The proposed design efficiently monitors the voltages of multiple battery cells on a single path and minimizes errors caused by environmental changes through reference voltage and temperature correction algorithms. Ref voltage block generates a reference voltage and compares it with the battery cell voltage during the monitoring process to ensure the accuracy of temperature correction and voltage measurement. The generated reference voltage is divided into 15 stages from 3.2V to 4.2V and entered into the switch array block. This reference voltage plays a key role in correcting monitoring errors caused by external environmental changes. The switch array block receives the voltage signal from the battery cell and sequentially selects and outputs the voltage value based on the signal provided by the code generation block, and the reference voltage input from the ref voltage block is also sequentially selected and transmitted to the monitoring path. This allows multiple voltage comparisons on a single path. The switch array block receives the control signal from the code generation block and selects the battery cell voltage or the reference voltage. The selected signal is amplified through the operational amplifier (OPAMP) and finally transmitted to the output data.

The following Fig. 2 describes the clock generation block and the code generation block.

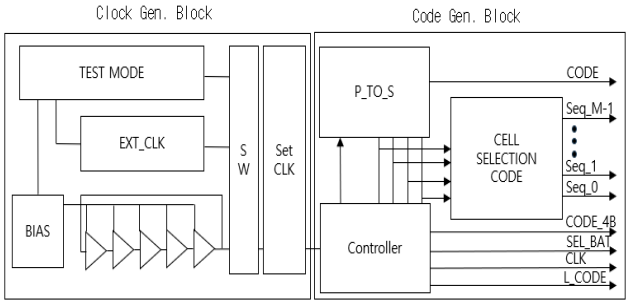


Fig. 2. Control Clock Generation and Battery Code Generation Circuit.

The clock generation block generates an internal clock signal (1 kHz) to coordinate system operations. This clock drives the code generation block and the monitoring system. The code generation block produces control signals to sequentially select the voltages of multiple battery cells. The generated SEL_BAT, CLK, L_CODE, and CODE_4B signals indicate which cell voltage is currently being output. Fig. 3 shows how the switch array block operates based on the Seq_N-1 signal obtained from the code generation block. The signals generated from the code generation block are entered into the ref_voltage switch array block and battery cell switch array block in sequence to select each battery cell voltage and internal reference voltage (voltage for temperature correction) and select either the internal

reference voltage or the battery cell voltage from the selection switch block. For use as a reference signal, 16 reference signals from 3.0V to 4.3V were made internally in 0.08V units for temperature correction. They were output sequentially through the REF Switch array shown in Fig. 3. In addition to sequentially monitoring the battery unit cell voltage, the battery switch array shown in Fig. 3 was configured to be output.

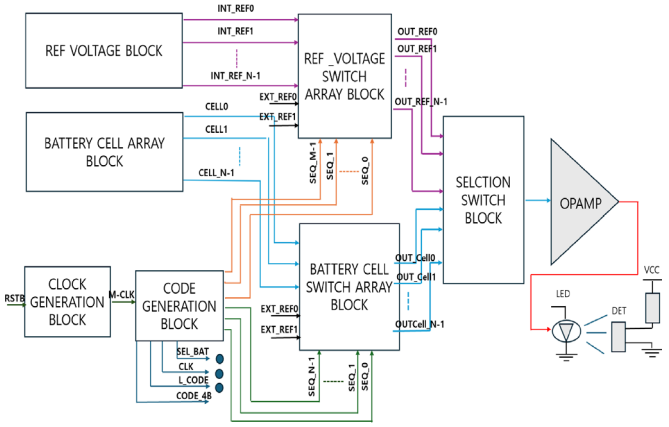


Fig. 3. Design Switch Array Block Circuit Structure.

Fig. 4 shows a timing chart of the signals in which the designed switch array block, clock generation block, and code generation block operate in Fig. 4. In order to output the voltage of the battery multi-cell sequentially in one path, it displays the L_CODE signal, which is the code signal for selecting battery cells, and the OUT signal, which is the battery voltage. The OUT voltage is a signal for outputting REF_V voltage and the voltage of the battery cell, and it can be seen in Fig. 4 that it is output together with the code signal CODE_4B so that a certain REF_V and a certain battery cell voltage can be known. Specifically, if the S_BAT signal is low, the battery voltage value is output, and if the S_BAT signal is high, the reference voltage value is output. When the ECU receives the multi-cell voltage and REF_V, it allows it to receive the voltage value separately from the code.

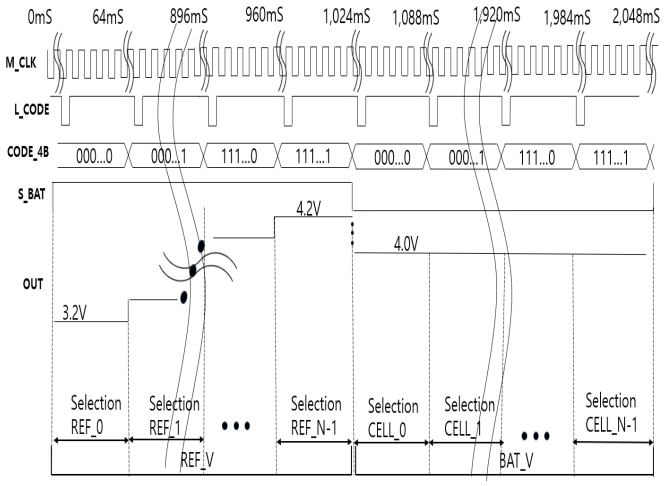


Fig. 4. Monitoring voltage Operation Timing Chart.

B. Isolated Balancing Circuit

The proposed isolated balancing circuit is composed of an isolation interface block and a balancing switch block. The isolation interface block receives control signals from the electronic control unit (ECU) and controls the high-voltage balancing switch block connected to the battery. When controlling the high-voltage balancing switch block, the circuit is designed with a photo diode and a photo detector to ensure electrical isolation between them. This structure enables the low-voltage operation control circuit of the ECU to function safely without being affected by high voltages that can reach thousands of volts. Fig. 5 illustrates the isolated balancing circuit proposed in this paper.

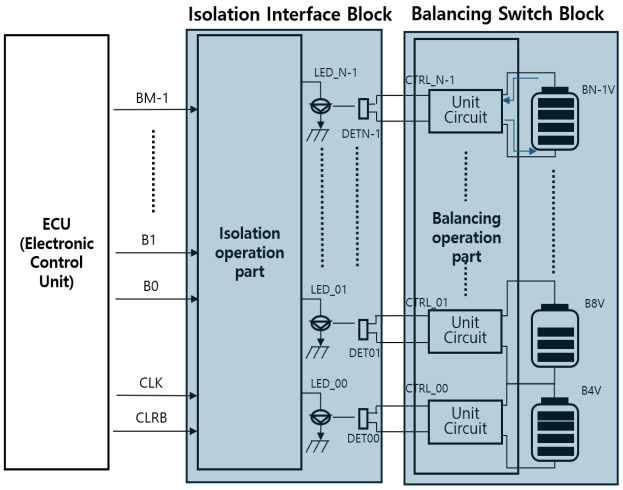


Fig. 5. The proposed isolated balancing circuit.

As shown in Fig. 5, the Isolated Design provides safe electrical Isolation between high-voltage and low-voltage operation control signals. In this indirectly connected structure, each single-cell unit is independently controlled, allowing multiple cells to be balanced simultaneously. For stable operation, M-bit (control signal) commands are synchronized with the CLK (Clock) signal to perform balancing operations. The Isolation Interface Block processes commands from the ECU (Electronic Control Unit) in an Isolated Manner, selects the battery required for discharge, and safely transmits the command to the Balancing Switch Block. This Isolation-Based Design is a key technology that maintains system stability even in high-voltage environments. It enables simultaneous balancing control without issues, not only in single-cell battery modules but also in battery packs composed of multiple battery modules. This design provides flexibility and scalability while ensuring that the high-voltage battery management system operates safely and reliably.

The Isolation Interface Block, which supports control operations, is designed to receive M-bit commands from the ECU, select the battery required for discharge, and perform the balancing operation. The number of battery cells (N) can be infinitely expanded in a series structure depending on the M-bit value. The operation of the insulation is illustrated as a block diagram in Fig. 6.

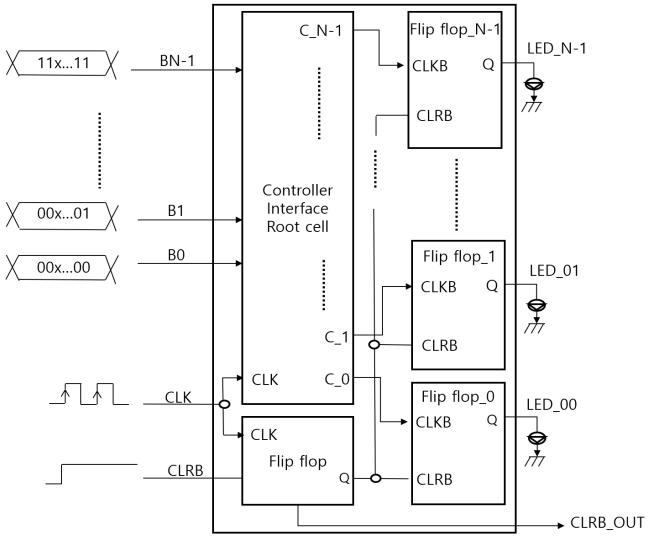


Fig. 6. Isolation Operation Part Circuit Block Diagram.

As shown in Fig. 6, the isolation interface block includes a controller interface root cell and a register corresponding to the battery cell control. At the input unit, the N battery cell values (C_0, C_1, . . . , C_N-1) output from the controller interface root cell output signals (C_0, B1, . . . , BM-1) for selecting cells according to the M bit commands (B0, B1, . . . , BM-1) of the ECU, and are designed to operate in synchronization with the CLK signal in the register. This method is designed so that the flip-flop can operate stably and minimize the noise effect on the input terminal. In addition, the flip-flop can initialize the balancing function using a clear signal (CLRB). The output unit generates a CLRB_OUT signal based on the ON/OFF state of the CLRB and transmits LED signals (LED_00, LED_01, ... , LED_N-1) that control each battery cell. These LED signals control the balancing operation of each battery cell and can safely separate the high voltage and low voltage to ensure the stability and reliability of the system. Through this, the balancing operation can be performed effectively and stably by safely isolating the battery and the control unit in a high-voltage and high-current environment. A detailed description of the operation can be found in Fig. 7.

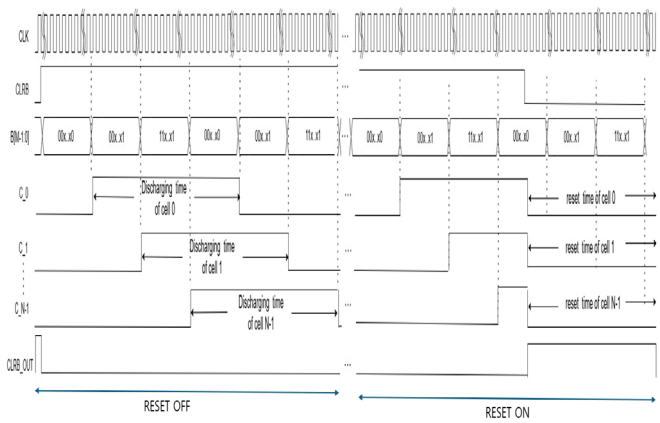


Fig. 7. Controller Interface Root Cell Timing Chart.

Fig. 7 shows a timing chart where the ECU selects a battery cell to be discharged from the N battery cell values (B0, B1, ..., BM-1) and transmits this information to the Controller Interface Root Cell. Each battery cell (C_0, C_1, ..., C_N-1) then performs discharge, balancing, and reset operations while being synchronized with the CLK signal. When the battery cell selection signals B0, B1, ..., BM-1 take the value 00x...x0, battery cell 0 (C_0) is selected, initiating the discharge process in synchronization with the CLK signal. Subsequently, when the same 00x...x0 signal appears again, it indicates that the discharge of battery cell 0 (C_0) has been completed. The bit pattern transitions from 00x...x0 to 11x...x1, sequentially selecting each battery cell for discharge in order. Fig. 7 visually represents this process, showing the sequential progression of the signals. Additionally, since B0, B1, ..., BM-1 are synchronized with CLK, the proposed circuit operates stably by executing the ECU′s CLK command to discharge the selected battery cell when necessary. In the initial state, the CLRB signal monitors all battery cell voltages. If an issue is detected, it resets all battery cell balancing operations. This mechanism uses the flip-flop structure of the CLK signal to control a stable battery balancing operation while preventing errors due to noise. The CLRB signal is also used to generate the CLRB_OUT signal, which provides feedback on the state of the CLRB signal, ensuring that the reset status is clearly indicated. In RESET OFF mode (as shown in Fig. 7), the balancing operation is executed normally. In RESET ON mode, the balancing states of all battery cells are reset.

Fig. 8 illustrates the Photo Diode and Photo Detector, which are the core circuit components of the isolated operation, responsible for generating control signals and executing the balancing operation to indirectly control the balancing process in the Isolated Balancing Circuit. The Photo Diode and Photo Detector circuits are highly sensitive to PVT (Process, Voltage, Temperature Variation) conditions. To ensure stable operation under all environmental conditions, it is necessary to optimize the Rd and Rb values, which define the operational characteristics of the Photo Diode and Photo Detector. These Rd and Rb values were optimized through experimental measurements. Fig. 8 presents a block diagram defining the Rd and Rb values.

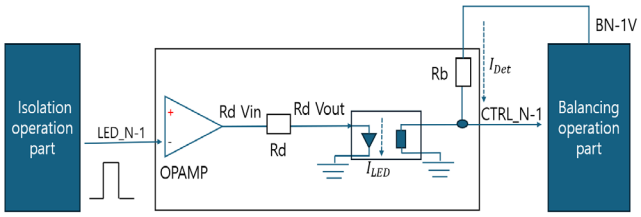
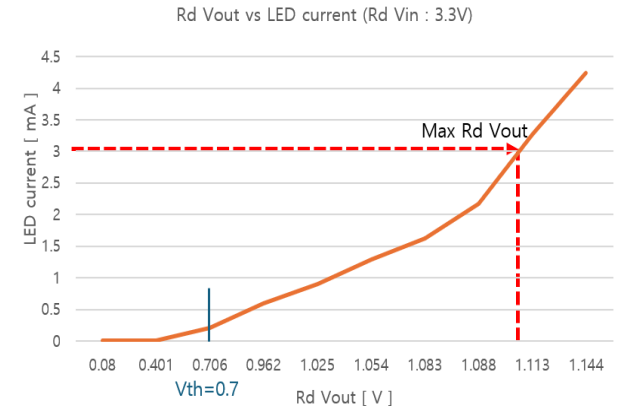


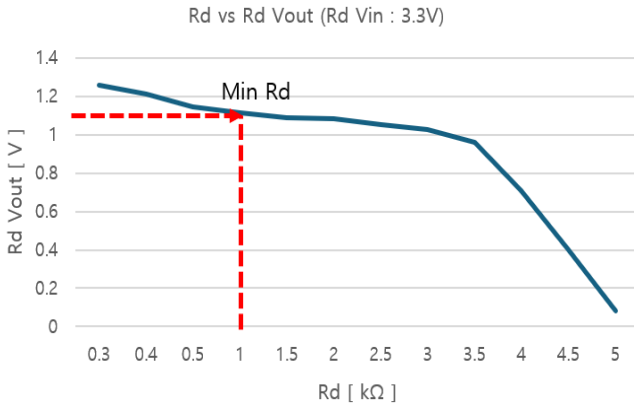
Fig. 8. Test block diagram for defining resistance Rd and Rb values.

Fig. 8 presents the experimental results defining the maximum input voltage (Rd Vout) of the Photo Diode (LED) based on the Rd value in the Isolated Balancing Circuit. The OPAMP, which drives the LED through Rd, operates with a maximum output current limit of 6mA. This output current is determined by both the Rd value and the operating voltage

of the Photo Diode. To ensure stable operation, the design restricts the output current to no more than 3mA, which is half of the OPAMP's maximum drive current. Fig. 9 illustrates the Photo Diode current characteristics as a function of Rd, as well as the maximum input voltage of the LED according to Rd.



(a)



(b)

Fig. 9. Photo diode operating characteristics: (a)Voltage for LED current and (b)Rd value according to voltage.

As a result of measuring the operation characteristics of the Photo Diode in Fig. 9, it was found that the maximum voltage at which the LED current remains below 3mA is 1.113V, with a corresponding resistance value of 1kΩ. Additionally, the threshold voltage (Vth) that initiates the Photo Diode operation was determined to be 0.7V.

Next, as shown in Fig. 10, the balancing current behavior was experimentally examined based on changes in Rb and Rd values, which influence the operation of the Photo Detector. It was observed that larger Rb values cause the balancing operation to begin earlier, and when Rb exceeds 5kΩ, the balancing current increases slightly but maintains similar balancing characteristics. Additionally, when the balancing switch is activated, a larger Rb value requires a higher Rd value. A higher Rd value reduces the operating current of the Photo Diode, thereby lowering the OPAMP load. However, if Rd becomes too large, the Photo Diode enters cutoff, preventing proper operation. To ensure stable operation, Rb was set to at least 5kΩ, and the effect of Rd on the balancing operation was analyzed. Fig. 10 presents a graph showing the variation in balancing current with different Rb values (3kΩ, 4kΩ, 5kΩ, 6kΩ) and Rd values. The results indicate that by appropriately adjusting Rb, the optimal operating conditions of the balancing circuit can be determined based on Rd values.

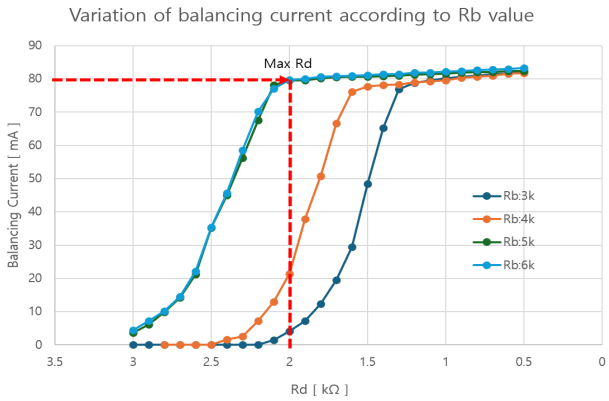


Fig. 10. Variation of balancing current according to Rb value.

The results obtained from the above graph indicate that when Rb is 5kΩ or higher, there is no significant variation in the balancing current curve. Additionally, when Rb is set to 5kΩ, the maximum Rd value is determined to be 2kΩ. If Rd exceeds 2kΩ, the balancing current decreases significantly or may not flow at all. To ensure optimal operation, Rb was set to 5kΩ, and Rd was designed as 1.5kΩ, which is the midpoint between the maximum value (2kΩ) and the minimum value (1kΩ).

C. Temperature Compensation

The indirect measurement circuit proposed in this paper also consumes a different amount of current depending on the temperature. On the other hand, LEDs are devices that change the intensity of light depending on the intensity of current consumed, so the value of Brightness changes depending on the temperature. Fig. 11 shows the change in Brightness according to the temperature.

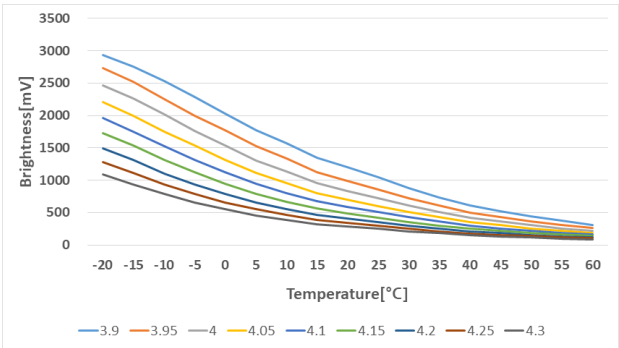


Fig. 11. Brightness changes according to the temperature change of the LED.

In the graph of Fig. 11, it can be seen that there is a tendency for the difference in brightness to be large at low temperatures and low voltages at the same battery voltage. Therefore, an appropriate temperature compensation circuit is required. In this paper, a circuit, such as an indirect measurement circuit, is connected to a regulator to measure the corresponding brightness, thereby measuring the temperature corresponding to the brightness, and an offset is

given to the brightness of each LED to implement a temperature compensation circuit. Fig. 12 shows the flowchart of the temperature correction algorithm. Temperature compensation is performed by sequentially determining the battery voltage by comparing it with the already known REF voltage value. The battery cell voltage is temperature-compensated based on the internal REF voltage, but the battery cell voltage can also be temperature-compensated based on the external REF voltage. In order to accurately obtain the internal REF voltage value, the values from 3.0 V to 4.3 V are divided into 16, and the REF values can be obtained sequentially. One step value of the internal REF voltage is 0.08 V, and a close value is set as the battery voltage value so that the accurate battery voltage can be known. In addition to defining the battery voltage value as a value close to each step, it was finally corrected through the equation of the internal REF to obtain an accurate battery voltage value. In conventional systems, temperature compensation was performed by defining a LUT based on discrete temperature values measured by sensors. However, this method has a fundamental limitation in resolution: it cannot compensate for temperatures that fall between the predefined points, and as device aging progresses, LUTs may become inaccurate. In contrast, the proposed method applies real-time interpolation using LED brightness and REF voltage, allowing continuous compensation over the entire –20 °C to 80 °C range with a measured error of less than ±5 mV. Moreover, by using a single LED path, our approach eliminates the need for separate temperature LUTs for multiple LEDs, thereby improving system consistency and long-term reliability. The temperature compensation algorithm in Fig. 13 is executed by first selecting the 0th battery cell and sequentially applying internal REF voltages from REF_00 to REF_N–1. This allows the system to match each measured battery voltage to its corresponding REF level, apply the compensation model, and repeat the process across all battery cells in sequence.

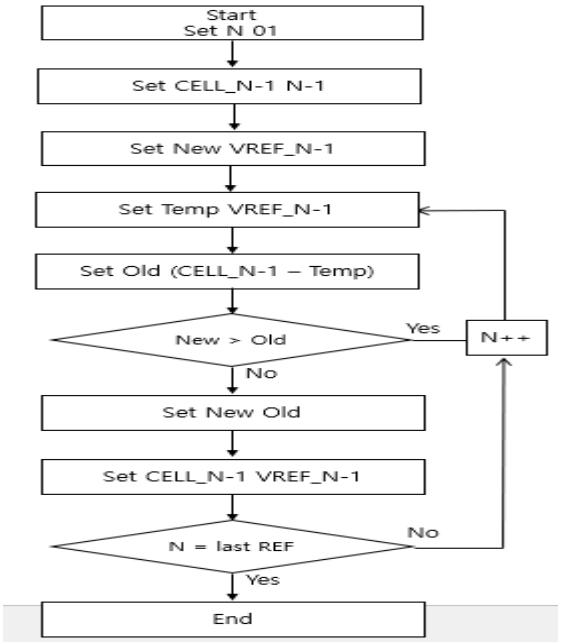


Fig. 12. Temperature Compensation Algorithm Flowchart.

III. RESULTS

Fig. 13 shows the semiconductor and the PCB results driving the semiconductor based on the above design contents, and an operation experiment was conducted based on this.

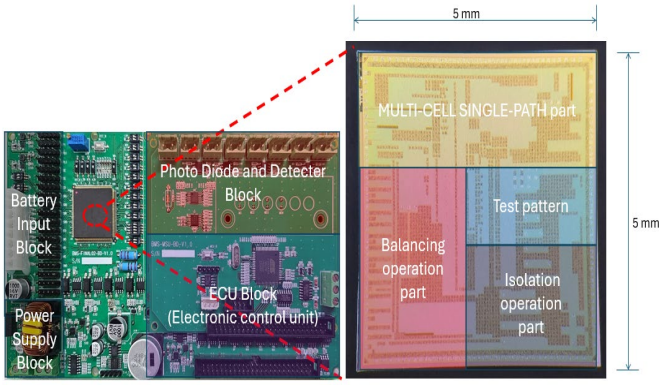


Fig. 13. Board manufacturing and Semiconductor chip manufacturing results,

The left figure in Fig. 13 shows the PCB results applied and driven by the designed semiconductor package, and the right figure shows the semiconductor chip designed inside the semiconductor package. The semiconductor chip consists of a multi-cell single-pass part and a balancing operation part, an isolation operation part, and a test pattern. The chip size is designed to be 5mm X 5mm. And the PCB is designed as a power supply block to drive the semiconductor chip, a photodiode and detector block, an ECU block to perform balancing control, and a battery input block to connect to the battery. Fig. 14 is the monitoring measurement result obtained by operating an external clock.

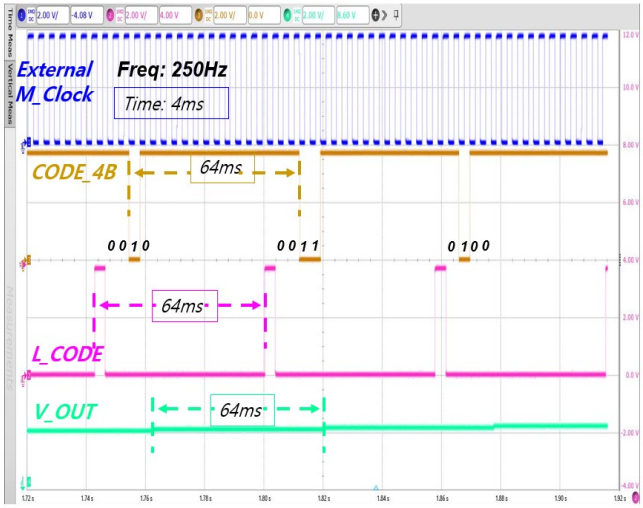


Fig. 14. Monitoring results measured by external clock.

The external clock measurement results in Fig. 14 confirm that the external M_Clock operates with a period of 250 Hz, that is, about 4ms. This external clock signal is the timing reference used throughout the system and is used to process 16 battery cell signals and 16 reference voltage signals (32 signals in total) sequentially. The measurement showed that

the total time to process 32 signals was about 2.048 seconds, which is consistent with the simulation. In addition, the external clock signals operate in conjunction with L_CODE, 4B_CODE, and V_OUT, similar to the internal clock signals, and the timing stability of the entire system is ensured by maintaining a constant temporal correlation between these signals. This confirmed the reliability and synchronization performance of the external clock measurement results.

The system takes approximately 2seconds to read 16 cells through this process. A battery pack consisting of 16 cells operates as a slave, and a single master can manage up to 256 slaves, forming a master/slave structured BMS. Since each cell typically has a 2P configuration (two cells in parallel), the master can manage up to 8,192 cells (=16 cells × 256 slaves × 2P) every 2 seconds through the controller. In addition, the designed circuit is configured to operate not only with an internal clock but also with an external 2.5 MHz clock, enabling all 16 cells to be read within approximately 200µsec

Fig. 15 shows the balancing circuit test results for the balancing current result according to the battery input voltage (Vin) and compared with the PVT simulation results.

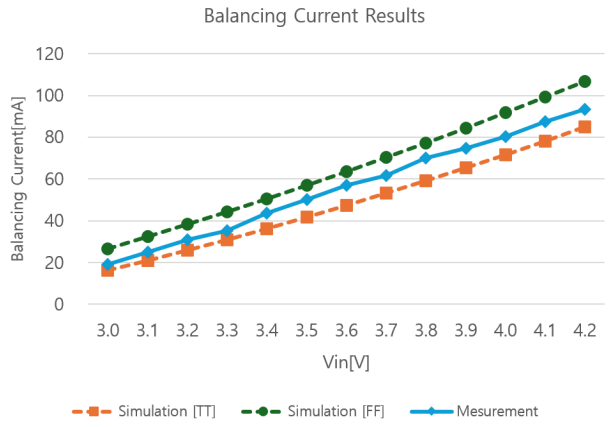


Fig. 15. PVT Balancing Simulation and measurement result.

In the graph, the actual measured values were found to lie between the TT (Typical-Typical) and FF (Fast-Fast) values of the simulation. Here, TT (Typical-Typical) represents a state where both NMOS and PMOS exhibit typical characteristics, reflecting the average process performance, which is commonly used as a reference point in circuit design. Conversely, FF (Fast-Fast) refers to a state where both NMOS and PMOS have fast characteristics, meaning that device mobility increases, enhancing current driving capability but potentially increasing power consumption. During the balancing operation, it was confirmed that at an input voltage of 3V, a current of at least 20mA flows, while at 4.2V, the balancing current exceeds 87mA. The measured results were found to be between TT and FF, indicating that the process characteristics fall within this range. Table I below compares the performance of the existing technology and the results of this study.

TABLE I. Comparison table with existing technology

Specification	This Work	TRAN II (2019) [10]	PEDES (2022) [11]	ECCE (2023) [12]	DISCOVER (2024) [13]
Architecture	Single-path, Single LED	Parallel LED	Series sensing	Series sensing	Series sensing
Isolation Method	Optical (Photodiode)	None	Current-controlled	None	None
Voltage Resolution	±5mV	±10mV	±20mV	±10mV	±10mV
Vref Granularity	16 steps (3.0–4.3V)	LUT-based	Fixed Vref	Fixed Vref	Fixed Vref
Temperature Compensation	Ref-based auto-correction	LUT-based	External sensor	None	None
Power Consumption	180µW (Core block)	5W	300mW	400mW	400mW
Monitoring Channels	16 cells (scalable, Master/slave)	7 cells	14 cells	16 cells	16 cells
Scalability	Scalable	Low	Moderate	Limited	Limited
technology	0.18µm	0.35µm	0.25µm	0.5µm	0.5µm

Unlike the existing technology that measures by being directly connected to the high voltage, this technology is an isolated technology that can stably balance the battery cells even at high voltage without affecting the controller circuit operating at the low voltage.

IV. CONCLUSION

This paper proposed a single-path multi-cell battery management system (BMS) utilizing an LED-based indirect measurement technique and a photodiode-based isolation structure to achieve accurate voltage monitoring and safe cell balancing in high-voltage battery environments. The proposed design efficiently processes and monitors 32 signals (16 battery cells and 16 reference voltages) through a single path, significantly reducing complexity and enhancing reliability. Experimental results demonstrated stable voltage measurement with a resolution within ±5mV from -20°C to 80°C. Additionally, the isolated balancing circuit, optimized by adjusting resistors Rd and Rb, maintained robust cell balancing currents ranging from 20mA at 3V to over 87mA at 4.2V, effectively mitigating power consumption and ensuring stable operation. Consequently, the proposed isolation-based BMS design provides significant advantages in high-voltage battery systems by offering improved safety, reliability, and scalability.

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