A 5-GHz Multi-Modulus Divider with Duty Cycle Extension Re-Timer on 65-nm CMOS Technology

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***Abstract* – In this paper, a multi-modulus divider (MMD) operating at 5 GHz has been designed using a 65-nm CMOS process. The MMD core is composed of cascaded DIV2/3 cells. The first three stages were composed of TSPC D-flipflop, and the last stage was composed of static D-flipflop. We propose a re-timer that extends the duty cycle by generating an asynchronous reset through digital logic gates. This not only removes accumulated circuit noise, but also generates a duty cycle from at least 43% to 53% depending on the division ratio. Based on the output frequency of 200MHz, when N is 25, the total power consumption is 0.9mW, and the circuit size is 75µm*30.5µm.**

***Keywords*—Phase locked loop, divider, re-timer, MMD, duty-cycle.**

I. INTRODUCTION

Phase-locked loops (PLLs) are widely utilized for frequency synthesis in various applications, including analog-to-digital converters (ADCs) and radio frequency (RF) circuits. Traditionally, analog PLLs have been predominantly used; however, they exhibit several disadvantages: (1) an increase in spurious tones due to current mismatch in the charge pump, which worsens as the supply voltage decreases with process scaling, (2) the requirement for a large chip area due to the use of a passive loop filter, and (3) challenges in implementing digital calibration [1], [2]. To address these issues, digital PLLs have become the preferred choice in recent years [3], [4], [5].

The architecture of a fractional-N bang-bang digital PLL is illustrated in Fig. 1. This structure comprises a bang-bang phase detector (BBPD), a digital loop filter (DLF), a digitally controlled oscillator (DCO), a multi-modulus divider (MMD), a delta-sigma modulator (DSM), and a digital time converter (DTC). The BBPD, which is a 1-bit time-to-digital converter (TDC), serves as an alternative to conventional TDC implementations [6]. The adoption of this architecture offers the following advantages: (1) utilizing a DTC enables fine resolution with lower power consumption compared to a conventional TDC, and (2) issues related to TDC resolution and linearity can be mitigated [7].

In Fig. 1, the phase difference between *REF* and *FB* is converted into a digital code through the BBPD. This digital code is then processed by the digital loop filter, which adjusts the frequency of the DCO, thereby controlling the output frequency.

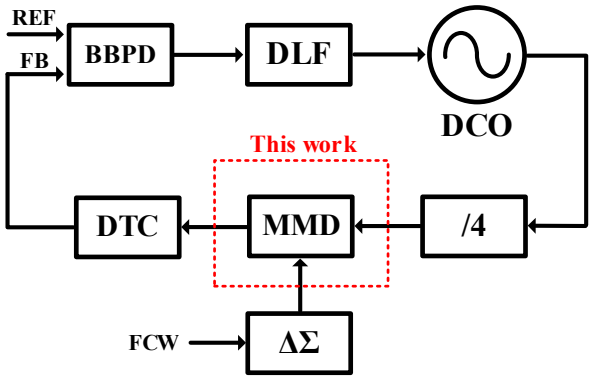

Fig. 1. Structure of fractional-N bang-bang digital PLL.

In an integer-N PLL, the frequency control word (FCW) is an integer, and thus the output frequency is limited to an integer multiple of the reference frequency, i.e., f_{OUT}=Nf_{REF}. This can be implemented using a single fixed division ratio without the need for a multi-modulus divider (MMD). However, such a structure cannot support the fine channel spacing of several kilohertz required by modern communication systems [8]. To overcome this limitation, a fractional-N PLL is required to enable finer frequency resolution. This is accomplished by dynamically adjusting the division ratio between N / N+1 using the output of a delta-sigma modulator (DSM), which serves as the digital control signal for the MMD. Consequently, the effective division ratio of the PLL can be expressed as N + α, where α is the fractional part of the *FCW*, having a value between 0 and 1. This value represents the average division ratio resulting from toggling between N / N+1.

However, conventional MMDs suffer from an insufficient output duty cycle depending on the division ratio [9]. This issue affects the pre-charge and reset operations of the digital time converter (DTC) in subsequent stages, leading to the degradation of its integral nonlinearity (INL), which in turn deteriorates the fractional spur performance of the PLL. To mitigate these challenges, a re-timer incorporating an inherent duty cycle extension technique is proposed,

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ensuring that the duty cycle of the multi-modulus divider (MMD) output remains within the range of 43% to 53%, depending on the division ratio N.

The remainder of this paper is organized as follows: Section II details the structure of the core multi-modulus divider (MMD) and the proposed re-timer. Section III discusses the simulation results. Finally, Section IV concludes the paper.

II. PROPOSED MMD WITH DUTY-CYCLE EXTENSION RE-TIMER

A. MMD Core Structure

Fig. 2 illustrates the multi-modulus divider (MMD) architecture proposed in [9], which employs a cascaded DIV2/3 structure to dynamically adjust the division ratio based on the selected MODE. When the MODE signal is set to ‘0’, the circuit operates as a DIV2, whereas for MODE = ‘1’, it functions as a DIV3. With an input frequency of 5 GHz, the division ratio N ranges from 16 to 31 using four cascaded DIV2/3 cells, resulting in an output frequency spanning from 161.29 MHz (N=31) to 312.5 MHz (N=16).

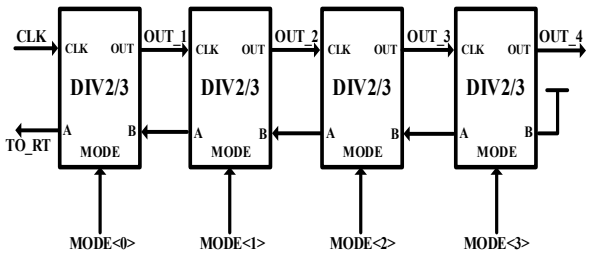


Fig. 2. Structure of MMD.

To enhance performance, the MMD design incorporates multiple types of latch and flip-flop structures. A true-single-phase-clock (TSPC) D-latch and flip-flop are utilized in the first three stages to minimize propagation delay and reduce power consumption. To further improve robustness, additional back-to-back inverters are included in the second and third TSPC stages. In contrast, the final stage employs a transmission-gate-based D flip-flop, where the operating frequency is relatively lower and stable operation at low speed.

Fig. 3 presents the detailed circuit implementation of the DIV2/3 cell. To mitigate propagation delays in the AND gates and latch circuits, an optimized design approach was adopted. In the first three stages, AND-latch structure was integrated into the TSPC-based circuit, as seen in instances such as *I1* and *I2*, to minimize delay and enhance overall performance [10]. Furthermore, the D flip-flop in *I3* was also optimized, as described above.

During DIV2 operation, when the MODE signal is set to '0', the output of *I2* remains consistently at logic '1', activating only *I3* and *I4*. In contrast, during DIV3 operation, when the MODE signal is set to '1', all cells from *I1* to *I4* are engaged, ensuring the intended frequency division. The dividing operation is triggered at each rising edge of the input clock to the DIV2/3 block. For DIV2, the output periodically follows (1,0), while for DIV3, it follows (1,0,0).

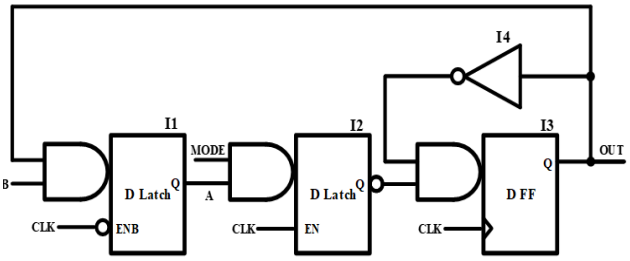


Fig. 3. Unit DIV2/3 circuit.

B. Duty-Cycle Extension Re-timer

Fig. 4 illustrates the proposed re-timer, which enhances the design methodology presented in [11]. In [11], retiming is achieved using *TO_RT*, as shown in Fig. 2, and its proper operation depends on the satisfaction of two key conditions: (1) *TO_RT* is generated from a transparent D-latch *I1* when the *CLK* input is ′0,′ as shown in Fig. 3. Since *I5* is a rising edge triggered D flip-flop, T_CLK/2 must be sufficiently larger than the flip-flop′s setup time. (2) The sum of the clock-to-Q delays of *I5* and *I6* must be significantly smaller than T_CLK to prevent timing violations and ensure reliable retiming. If these conditions are satisfied, the re-timer effectively suppresses MMD noise.

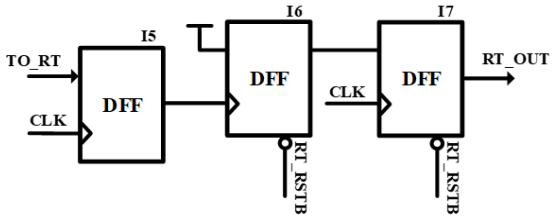


Fig. 4. Re-timer.

Despite its effectiveness in noise suppression, the re-timer in [11] has a notable drawback—insufficient duty cycle. The duty cycle varies significantly depending on the division ratio, which directly affects the reset and pre-charge operations of the subsequent DTC. To overcome this limitation, we propose a duty-cycle extension technique utilizing simple combinational logic.

Unlike the conventional approach in [11] , where *RT_RSTB* employs fixed reset logic regardless of the division ratio, the proposed re-timer dynamically adjusts its logic configuration based on the division ratio (e.g., *MODE*). The logic is shown in Fig. 5. When (*MODE*<3>, *MODE*<2>) = (0,0) or (1,0), the circuit uses a combinational logic gate. For (*MODE*<3>, *MODE*<2>) = (0,1), the logic implementation remains the same as in [11]. Finally, for (*MODE*<3>, *MODE*<2>) = (1,1), only an inverter is used. As a result, the overall division ratio ranges from 16 to 31, and is partitioned into four groups: logic 1 for 16~19, logic 2 for 20~23, logic 3 for 24~27, and logic 4 for 28~31. Depending on the operating mode, one of these logic blocks is selected via a multiplexer (MUX). This adaptive logic configuration effectively minimizes duty cycle variation and mitigates MMD-induced noise with minimal hardware overhead.

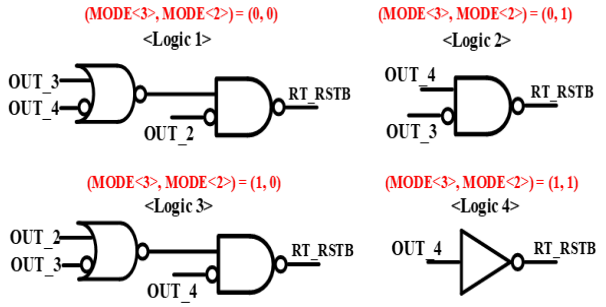


Fig. 5. Proposed asynchronous reset generator.

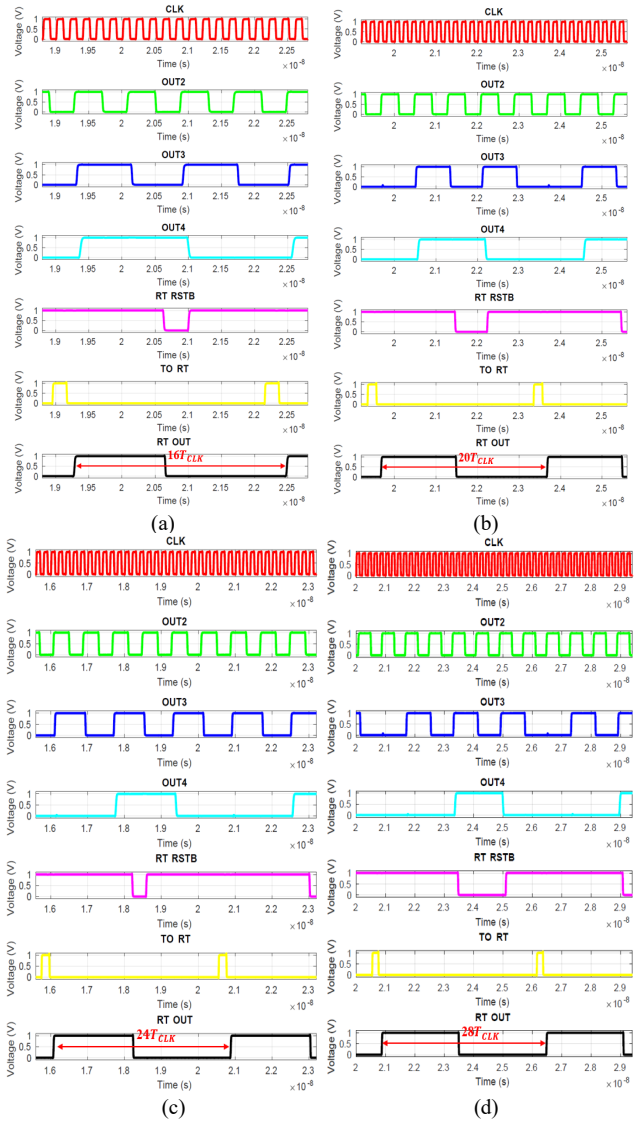


Fig. 6. Proposed asynchronous reset generator and re-timer transient plot: (a) Logic 1 (N=16), (b)Logic 2 (N=20), (c)Logic 3 (N=24), and (d)Logic 4 (N=28).

Fig. 6 shows representative transient plots for *RT_RSTB* generation, each corresponding to a specific division ratio selected from the ranges of 16 to 19, 20 to 23, 24 to 27, and 28 to 31. In Fig. 6(a), the waveform corresponds to a division ratio of 16, where *RT_RSTB* is generated through a NOR operation between the inverted *OUT4* and *OUT3*, followed by a NAND operation with the inverted *OUT2*. Fig. 6(b) illustrates the case of a division ratio of 20, where *RT_RSTB* is formed by inverting *OUT3* and performing a NAND operation with the inverted *OUT2*. In Fig. 6(c), corresponding to a division ratio of 24, *RT_RSTB* is generated through a NOR operation between the inverted *OUT3* and *OUT2*, followed by a NAND operation with the inverted *OUT4*. This logic structure is functionally equivalent to that of Fig. 6(a). Fig. 6(d) shows the case of a division ratio of 28, where *RT_RSTB* is generated using only inverters. All *RT_RSTB* signals are designed to be generated between two consecutive *TO_RT* pulses to ensure robust operation of the re-timer.

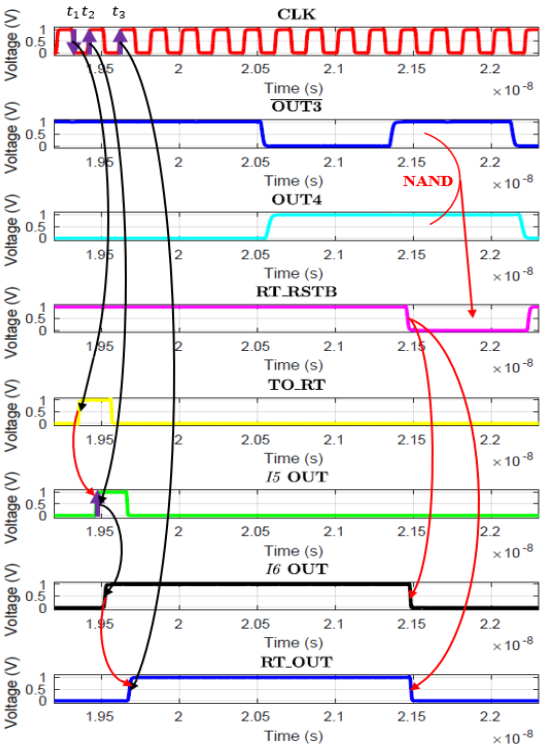


Fig. 7. Proposed asynchronous reset generator and re-timer timing diagram when using logic 2 (N=20).

Fig. 7 illustrates a detailed view of a section of Fig. 6(b). The *RT_RSTB* signal is generated using *OUT3* and *OUT4*. As shown in Figs 2 and 3, the *TO_RT* signal, which serves as an input to the re-timer shown in Fig. 4, is triggered by the falling edge of the *CLK* at time t_1 in the timing diagram. At t_2, *TO_RT* is sampled at *I5* in Fig. 4 on the rising edge of the *CLK*. *I6* is triggered by the rising edge of the output from *I5* and consistently outputs a logic "HIGH". Finally, *RT_OUT* is generated at t_3 by *I7*. The outputs of *I6* and *I7* are observed to be asynchronously reset by the *RT_RSTB* signal.

III. SIMULATION RESULTS

The proposed MMD was designed in a 65-nm CMOS process, occupying an area of 75 μm × 30.5 μm, as shown in Fig. 8. With an input frequency of 5 GHz and a four-stage cascaded structure, the division ratio ranges from 16 to 31, resulting in an output frequency range of 161.3 MHz to 312.5 MHz.

Fig. 9 presents the duty cycle of the MMD output, comparing the proposed design with that in [11]. The duty

cycle in [11] exhibits a variation of 34%, ranging from approximately 30% to 64%. In contrast, the proposed MMD, incorporating a re-timer, reduces this variation to only 10%, maintaining a duty cycle between 43% and 53%. These results demonstrate the effectiveness of the proposed method in minimizing duty cycle variation.

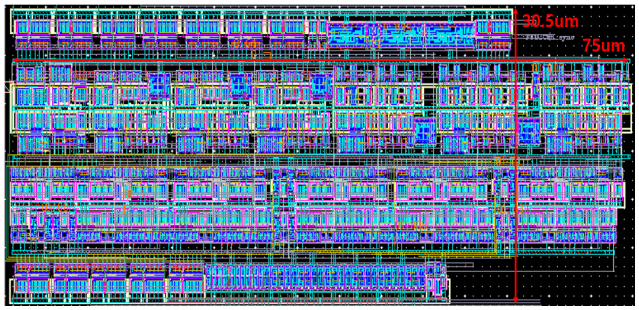


Fig. 8. Layout of MMD with proposed re-timer.

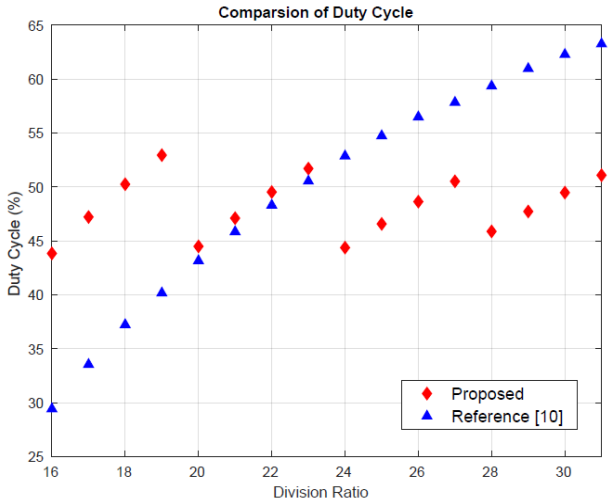


Fig. 9. Comparison of duty cycle.

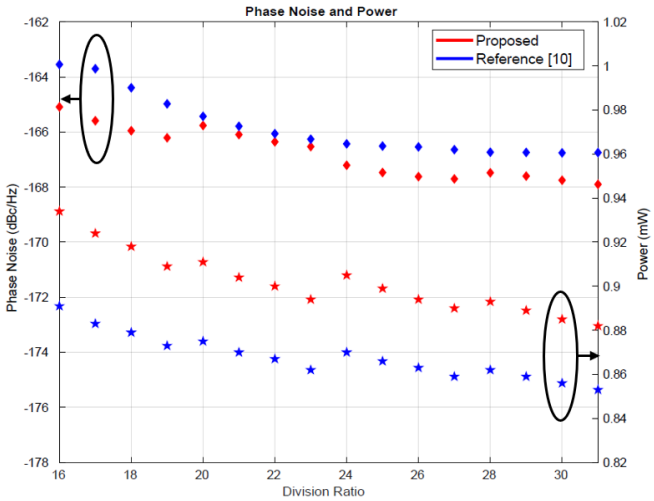
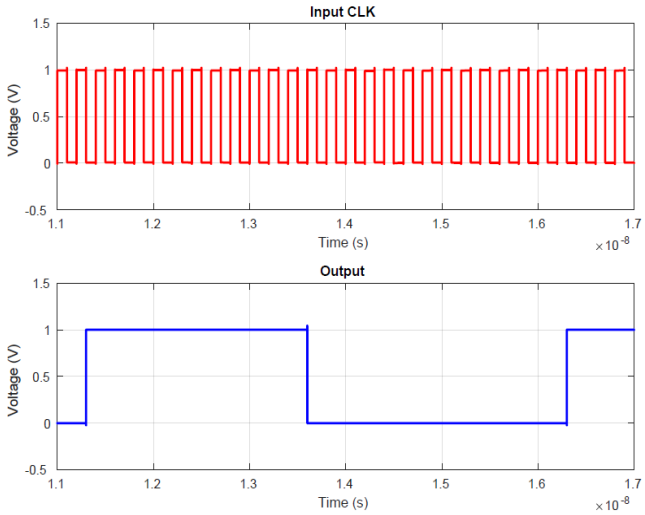


Fig. 10. Comparison of phase noise and power.

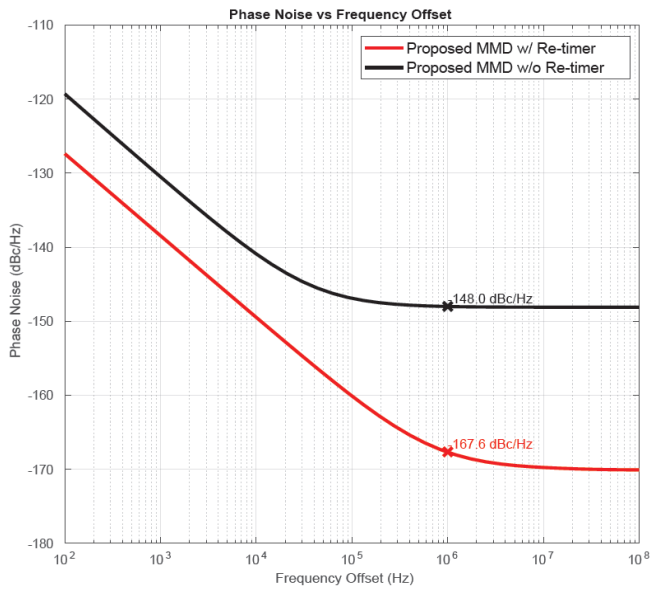
The phase noise performance and power at other division ratios are presented in Fig. 10 to further validate the robustness of the proposed MMD across various division ratios. The proposed MMD exhibits phase noise performance similar to that in [11] but consumes 30uA ~ 40uA more current due to additional circuitry shown in Fig. 5.

Fig. 11(a) illustrates the transient waveform of the proposed MMD with a 5 GHz input signal. The output waveform at 200 MHz, corresponding to a division ratio of 25, demonstrates stable frequency division operation. The output frequency is set to 200MHz to match the reference clock (*REF*) frequency shown in Fig. 1, which operates at 200MHz.

Fig. 11(b) illustrates a comparative analysis of the phase noise performance before and after the implementation of the proposed re-timer. The results show that incorporating the re-timer improves phase noise by 19 dB, effectively reducing jitter and enhancing signal purity. These findings confirm that the proposed re-timer not only mitigates duty cycle variation but also reduces noise induced by the MMD through its re-timing operation, thereby enhancing overall MMD performance.



(a)



(b)

Fig. 11. (a) Proposed MMD input CLK and output transient waveform (division ratio: 25); (b) MMD phase noise comparison before and after applying the proposed re-timer (division ratio: 25).

TABLE I. Comparison of [11] and proposed MMD.

	Reference [11]	Proposed MMD
Duty-Cycle [%]	30 ~ 64	43 ~ 53
Phase-Noise [dBc/Hz]	-166.74 ~ -163.54	-167.9 ~ -165.59
Power [mW]	0.853 ~ 0.891	0.882 ~ 0.934

IV. CONCLUSION

In this paper, a re-timer with an inherent duty cycle extension technique is proposed. By utilizing this technique, the duty cycle variation is reduced to 10% at a 5 GHz input frequency. Furthermore, as demonstrated in the simulation results, the proposed re-timer effectively suppresses noise, similar to the previous re-time design.

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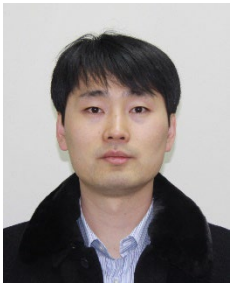

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