Impedance Measurement Integrated Circuit for Wireless Sensor Readout

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***Abstract* – This chip detects the resonant frequency of an inductor-capacitor (LC) wireless sensor by analyzing its impedance characteristics. When wireless coupling occurs between the transmitter (TX) resonator and the receiver (RX) sensor, the impedance of the TX coil varies with the RX sensor's frequency response. By analyzing the voltage variation across the TX resonator, the TX coil's impedance can be determined, achieving resonant frequency detection of the RX sensor. Existing portable sensor readout systems using commercial ICs suffer from high complexity and power consumption. To address these issues, an impedance measurement IC is designed. The proposed IC extracts voltage characteristics at both ends of the TX resonator using a single-to-differential converter, mixer, level shifter, and low-pass filter. Therefore, the impedance of the TX coil is derived by dividing the two output DC voltages. Post-layout simulations with varying the TX coil resistance confirm that the measured values match the initial set values. The IC is designed using the TSMC 180nm RF CMOS process.**

***Keywords* — LC Sensor, Impedance measurement, Resonant frequency detection, Wireless sensor readout**

I. INTRODUCTION

The resonant LC wireless sensor consists of an RX coil and a capacitive sensor, and operates by changing the gap between capacitor plates in response to the external environment variation, such as pressure changes, altering the resonant frequency of the LC circuit. To measure the resonant frequency of the RX sensor, the TX module sweeps RF signals to find a certain frequency that matches the resonant frequency of the RX sensor. At the sensor's resonant frequency, electromagnetic wave reflection from the RX sensor is minimized relative to the electromagnetic waves emitted from the TX coil, at which point maximum power is transferred.

Traditionally, a readout system comprising a vector network analyzer (VNA) and a TX coil has been primarily used to measure the resonant frequency of the RX sensor [1]. The resonant frequency and pressure variation can be detected by finding the minimum point of the reflection coefficient (S_{11}) measured by the VNA. However, VNAs are typically bulky, complex, and costly. To overcome these disadvantages, recent developments have focused on portable systems using a method that detects changes in the impedance of the TX coil when TX-RX coupling occurs [2] [3]. The voltage at both ends of the TX (V_{in}, V_{out}) is identified and used to extract the impedance characteristics of the RX sensor, as shown in Fig. 1.

However, using commercial ICs instead of custom ICs still leaves constraints regarding power consumption, performance optimization, and system area. The proposed IC simplifies the measurement process with a compact and power-efficient system.

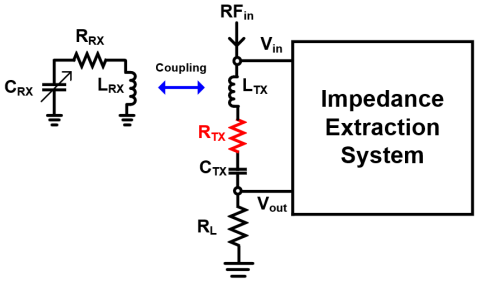

Fig. 1. Wireless Sensor Readout System with Impedance Extraction.

II. DESIGN METHODOLOGY

A. Proposed Impedance Measurement IC

As shown in Fig. 2, the proposed impedance measurement IC consists of a Single-to-Differential Converter (S to D), a double-balanced mixer, a level shifter (LS), and an active low-pass filter (LPF), configured with two channels. The current reference and bias generation circuit adjusts LPF, mixer, and LS biasing voltages and common mode voltages (V_{b_lpf}, V_{cm-}, V_{cm+}, V_{b_mixer}, V_{b_LS}).

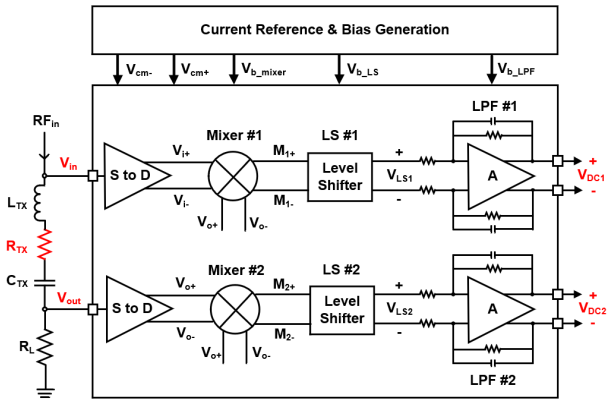

Fig. 2. Proposed Impedance Measurement IC Block Diagram.

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Manuscript Received Feb. 11, 2025, Revised Apr. 23, 2025, Accepted Apr. 24, 2025

The S to D circuit converts a single-ended input into a differential output and acts as a voltage buffer, enabling the use of a double-balanced mixer with differential inputs. The double-balanced mixer, implemented using a Gilbert cell, determines the multiplied peak node voltages and the phase difference between two nodes [4]. The LS circuit adjusts the mixer's output DC level to match the LPF's input DC operating point. The LPF circuit removes harmonic components from the mixer, extracting and amplifying only the DC components that contain phase difference information.

The voltages at both ends of the TX resonator (V_{in}, V_{out}) are applied through each channel, resulting in the output voltages (V_{DC1}, V_{DC2}) as follows:

$$V_{DC1} = V_{in}V_{out}cos\varphi \qquad V_{DC2} = {V_{out}}^2 cos\varphi \qquad (1)$$

By calculating the ratio of V_{DC1} to V_{DC2}, it is possible to derive the parasitic resistance of the TX coil.

$$\mathrm{Re}(Z_{TX}) \propto \frac{V_{DC1}}{V_{DC2}} \qquad (2)$$

At the resonant frequency of the RX sensor, $\mathrm{Re}(Z_{TX})$ reaches its maximum with wireless coupling. Therefore, by measuring the resistive component of the TX coil, it is possible to detect the RX sensor.

B. *Current Reference & Bias Generation Circuit*

As shown in Fig. 3, the current reference utilizes a constant-g_m biasing circuit structure (MP_2, MP_3, MN_4, MN_5) and includes a start-up circuit (MP_1, MN_1 to MN_3). Through the biasing circuit, the gate voltage (V_{b_LPF}) for MN_4 and MN_5 is obtained. Additionally, a biasing circuit using an additional current mirror and diode-connected MOS generates V_{b_LS} and V_{b_mixer} for operating the LS and mixer. These nodes are connected to the tail current source of the LPF, LS, and mixer. Also, the circuit generates supplementary voltages (V_{cm-}, V_{cm+}) to adjust the output common mode voltage of S to D, ensuring proper operating conditions for the subsequent double-balanced mixer stage.

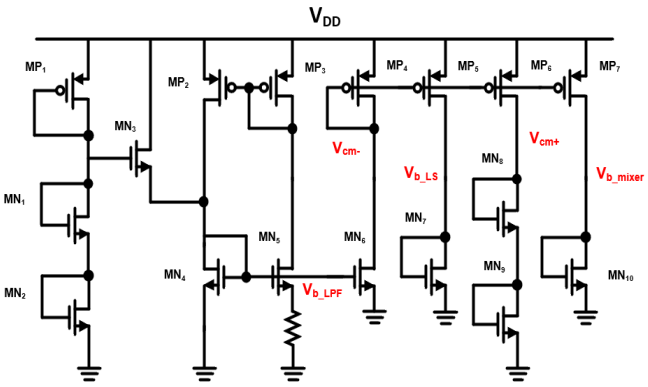

Fig. 3. Schematic of the Reference Generation Circuit.

C. *Single to Differential Converter (S to D)*

The S to D circuit consists of a common-source (CS) stage with a drain resistor and a source follower (SF) stage with a source degeneration resistor. It receives input at the NMOS gate to exhibit high input impedance. The V_{o-} terminal operates as a CS amplifier, while the V_{o+} terminal functions as a source follower. When the two resistors are matched, the conversion gain shows identical but with an inverted phase, enabling the acquisition of a differential input stage for the subsequent mixer stage.

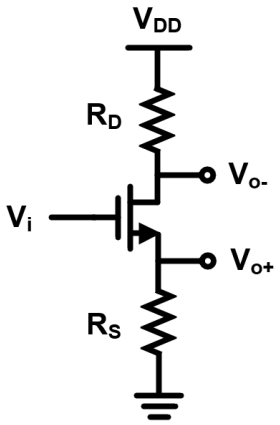

Fig. 4. Schematic of the Single to Differential Converter (S to D).

The voltage gains of the CS and SF stages in S to D circuit in Fig. 4 follow these equations:

$$A_{V1} = -\frac{R_D}{\frac{1}{g_m}+R_S} \qquad A_{V2} = \frac{R_S}{\frac{1}{g_m}+R_S} \qquad (3)$$

Here, A_{v1} and A_{v2} represent the voltage gains of the CS and SF stages, respectively, while g_m denotes the transconductance of the NMOS. To minimize signal distortion and gain mismatch, the circuit sets $R_S = R_D = 500\Omega$. The common mode voltages of both V_{O-} and V_{O+} are adjusted through DC coupling capacitors, either V_{cm-} or V_{cm+}, from the bias generation circuit. Therefore, the input common mode voltage requirements of the subsequent double-balanced mixer stage are verified. Furthermore, the input impedance of the mixer receiving signals through the NMOS gate exceeds the output impedance of the CS and SF stages.

D. *Double-balanced Mixer with Level Shifter (LS)*

As shown in Fig. 5, the double-balanced mixer acts as a voltage multiplier for two differential inputs (V_{in1}, V_{in2}). Through this multiplication, it generates DC components that include the phase difference between the two inputs, along with unnecessary harmonic components of the excitation frequency. To implement the mixer, a Gilbert cell structure was chosen [4], consisting of a current source (M_{N1}) biased by the reference generation circuit (V_{b_mixer}) in Fig. 3, a transconductance stage (M_{N2}, M_{N3}), and a switching stage (M_{N4}–M_{N7}) with output drain resistors. The differential output node (V_{M+}, V_{M-}), which contains both DC and harmonic components, is connected to the level shifter.

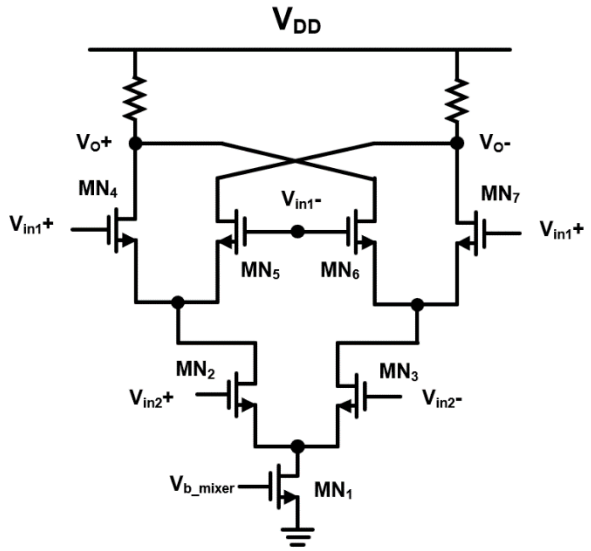

Fig. 5. Schematic of the Double-balanced Mixer.

Also, the LS circuit in Fig. 6 decreases the output common-mode voltage of the double-balanced mixer. It is configured as a source follower using an NMOS load, which lowers the DC voltage by the amount of V_{b_LS} generated from the reference circuit in Fig. 3, adjusting the input common mode voltage suitable for the operation region of the active LPF. Additionally, it acts as a buffer, preventing additional loading on the mixer's load drain resistor with the feedback resistor of the LPF stage. To minimize mismatch, the active LPF and LS are symmetrically positioned around the reference generation circuit in the IC layout.

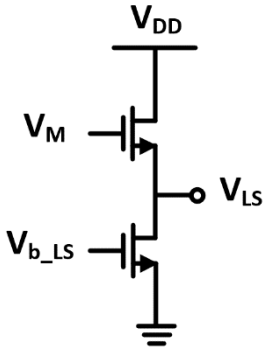

Fig. 6. Schematic of the Level Shifter (LS).

E. DC-gain Active Low Pass Filter (LPF)

The DC-gain LPF removes unwanted harmonic components from the mixer output while amplifying the DC component that contains the phase difference. As shown in Fig. 7, the output voltage from the level shifter is amplified through a feedback network consisting of 10kΩ on-chip resistors and an operational amplifier (op-amp). The feedback resistance and capacitor allow for external adjustment of the LPF's gain and bandwidth. The output common mode voltage of the Active LPF is adjusted to ensure operation in the saturation region by trimming V_{b1}, V_{b2}, V_{b3}, and the aspect ratio of the NMOS and PMOS. More practical topologies, such as CMFB, will be addressed in future work.

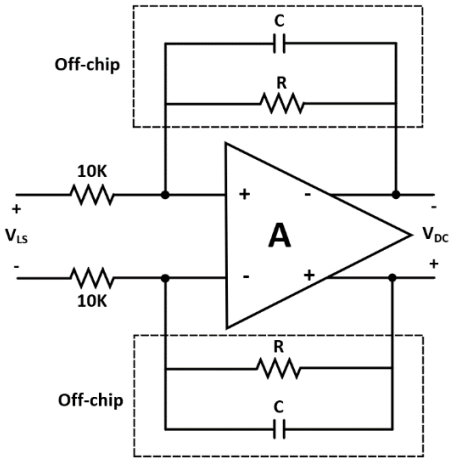

Fig. 7. Overall Diagram of the DC-gain Active LPF.

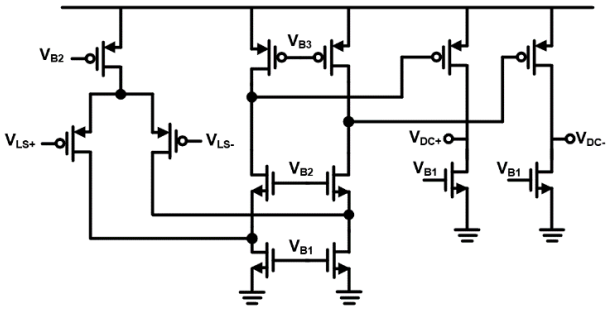

Fig. 8. Schematic of an Op-amp for the Active LPF.

The differential input to differential output op-amp is configured as shown in Fig. 8 and consists of a 2-stage amplifier with a PMOS folded cascode amplifier and with CS amplifier. The bias circuit is structured as depicted in Fig. 9, which receives V_{b_LPF} voltage from the reference circuit in Fig. 2 and provides bias voltage to the op-amp's bias nodes (V_{B1}, V_{B2}, V_{B3}) through current mirrors. The simulated op-amp's open-loop gain is 81.7dB, and for stability, load capacitors added to the V_{DC+} and V_{DC-} nodes adjust the phase margin to 42.3 degrees (C_L = 5nF).

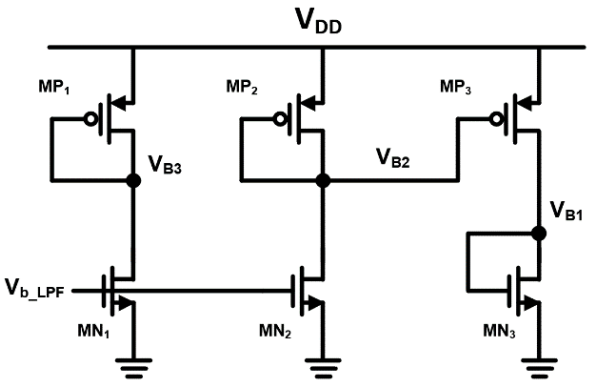

Fig. 9. Schematic of the Biasing Circuit for Op-amp.

III. RESULTS AND DISCUSSIONS

A. Proposed IC Layout

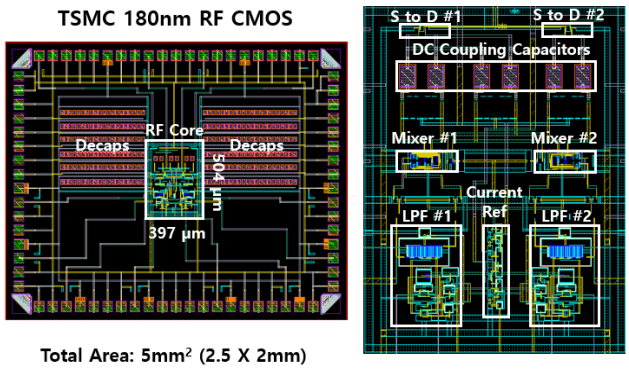

Fig. 10. Proposed IC Layout.

The proposed IC has been implemented using the TSMC 180nm RF CMOS process. As shown in Fig. 10, the total area of the IC is 2.5mm by 2mm, with the active area containing only the RF core being 504 µm by 397 µm. As depicted from the block diagram in Fig. 1, the RF core is comprised of two channels of S to D, mixers, and LPF. Also, additional DC coupling capacitors are used for adjusting the common-mode voltage to the mixer inputs.

B. Post-Layout Simulations

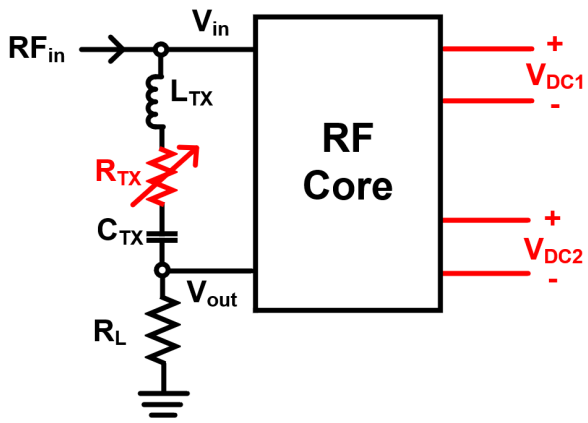

Fig. 11. Post-layout Simulation Testbench.

When TX and RX are coupled, the resistive component seen at TX (R_{TX}) reaches maximum at the resonant frequency of the RX sensor. Therefore, as shown in Fig. 11, a testbench is configured with the RLC circuit and proposed IC (RF Core). The R_{TX} values are adjusted while measuring V_{DC1} and V_{DC2}. These values are then converted into the $Re(Z_{TX})$ from the equation below to check the similarity between the calculated values and the initial set values. In this testbench, V_{DD} = 1.8V, L_{TX} = 3µH, C_{TX} = 9.4pF, and R_L = 50Ω.

Figs. 12, 13, and 14 display the output DC voltage of the proposed RF core IC as the R_{TX} (resistive component seen at TX) varies. Taking Fig. 10 as an example, the graph at the top shows the voltages at all four output nodes of the active LPF, while the voltage at the bottom shows the voltage difference at the output nodes of the LPF (V_{DC1}, V_{DC2}). The DC voltage is measured when these voltages have settled, and then substituted into the equations to calculate R_{TX} and compare it with the set values.

$$\mathrm{Re}(Z_{TX}) = \left(\frac{V_{DC1}}{V_{DC2}} - 1\right)R_L \tag{4}$$

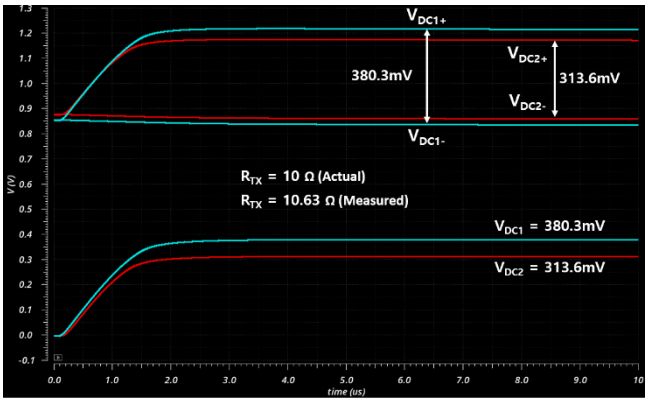

Fig. 12. Post-layout Simulation at R_{TX} = 10 ohms.

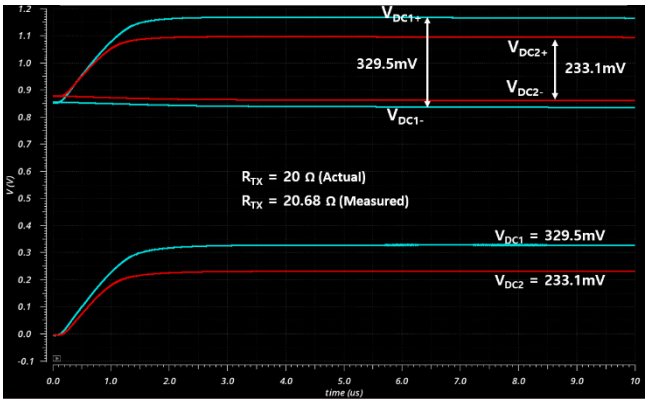

Fig. 13. Post-layout Simulation at R_{TX} = 20 ohms.

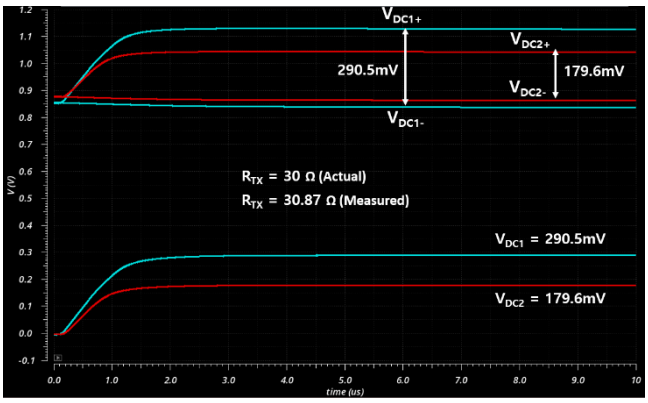

Fig. 14. Post-layout Simulation at R_{TX} = 30 ohms.

TABLE I. Measurement Accuracy of the Proposed IC.

Actual R_{TX}	Measured R_{TX}	Measurement Error	Accuracy (%)
10 Ω	10.63 Ω	0.63 Ω	93.7
20 Ω	20.68 Ω	0.68 Ω	96.6
30 Ω	30.87 Ω	0.87 Ω	97.1

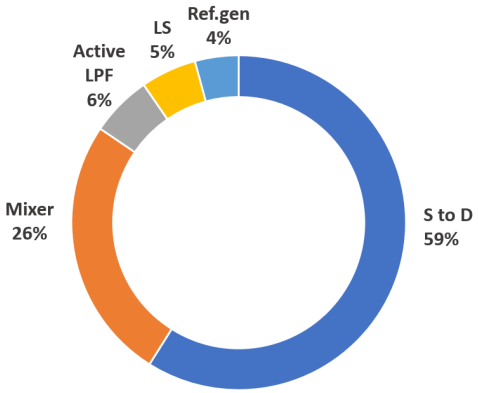

Fig. 15. Block-by-Block Power breakdown of the proposed IC

Table I shows the measurement accuracy of the proposed system with varying R_{TX}. The resonant frequency was set at 30 MHz, and the R_{TX} values were measured at 10.63 ohms when the setting value was 10 ohms, 20.68 ohms when set to 20 ohms, and 30.87 ohms when set to 30 ohms, demonstrating an accuracy of over 93.7%. Therefore, using this proposed IC simplifies the measurement process.

Fig. 15 illustrates the power consumption ratio of each block in the proposed IC. The circuit consumes 3.083mA of current at V_{DD} = 1.8V, resulting in a total power consumption of 5.55mW. S to D accounts for the majority of the overall power consumption (59%), followed by mixer (24%), active LPF (6%), LS (5%), and reference generator (4%).

C. Performance Comparison

TABLE II. Performance Comparison.

Performance	This work	[2]	[3]
System Topology	Mixer + LPF (ASIC)	Mixer + LPF (Commercial)	Buffer + Peak Detector (Commercial)
Supply	1.8V	-	5.5V
Power Consumption	5.55mW	1010mW	24.2mW
Chip Area	5mm^2	100mm^2	20mm^2
Frequency Range	10 - 50MHz	1 - 100MHz	1 - 10MHz
Relative Difference	< 6.3%*	< 0.33%**	< 3.8%**

* $Re(Z_{TX})$ measurement.
** Resonant frequency measurement.

Table II compares the key performance metrics between this work and previous works that could be utilized for similar applications. The core commercial ICs of each work are listed ([2]: mixer, AD831, [3]: buffer, ADA4891-1). The proposed IC demonstrates significantly lower power consumption (up to 184 times improvement) and system area (20 times reduction) compared to previous works, despite its lower measurement accuracy. The measurement accuracy is expected to improve with additional calibration processes in future work.

IV. CONCLUSION

The proposed RF core IC for use in a portable RF readout system was designed with TSMC 180nm RF CMOS. The proposed IC comprises two channels, including S to D, mixers, level shifters, and an active LPF, capable of sampling voltages at both ends of the TX resonator to measure gain and phase. The circuit's operation and measurement accuracy were validated through post-layout simulation, and it is expected to reduce the computation complexity of impedance measurement.

ACKNOWLEDGMENT

The authors would like to thank IDEC for participating HM-2303 MPW process for fabricating the proposed RF core IC. This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIT) (No. RS-2020-NR047144). This work was supported by the BK21 FOUR program (Connected AI Education & Research Program for Industry and Society Innovation, KAIST EE, No. 4120200113769). K. Kwon acknowledges support from Institute of Information & communications Technology Planning & Evaluation (IITP) under the Graduate School of Artificial Intelligence Semiconductor(IITP-2025-RS-2023-00256472) grant funded by the Korea government(MSIT).

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