Neural Recording with Auto Noise Calibration to Reduce Multichannel Variation

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Abstract **- Recording neural signals and transmitting measurement data wirelessly is crucial for implementing closed-loop neural stimulation systems. This work achieves a dynamic range of over 90 dB by employing delta-sigma and auto-ranging structures in an integrated circuit (IC) chip. Traditional wireless data transmission methods such as Bluetooth, inductive coil, and RF communication pose challenges including large spatial requirements, movement restrictions, and low data transmission rates relative to power consumption. To address these limitations, this research adopts optical communication techniques for wireless data transmission from freely moving multiple experimental animals. Additionally, noise calibration logic is designed to reduce channel mismatches. The IC chip, fabricated in a standard 65nm CMOS process, has a size of 1 mm² and consists of 8 channels.**

Keywords **- Closed-loop neural recording, Wireless communication, Noise calibration, Delta sigma ADC**

I. INTRODUCTION

Significant efforts have been made to develop multi-channel neural recording devices to research brain disorders such as epilepsy, Alzheimer's, and Parkinson's diseases, as well as to explore brain mechanisms [1-4]. To assess brain connectivity and functional aspects more effectively, it is necessary to enhance spatial resolution by utilizing a greater number of electrodes to measure more brain regions. Thus, the devices capable of measuring neural signals with over 10,000 channels are under investigation [5]. However, performance issues due to process-voltage-temperature (PVT) variations and mismatches in gain, common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR) are challenges.

Traditional approaches to improving gain accuracy, such as using passive components [6], trimming techniques with external reference resistors [7], or group chopping methods, are impractical for large-scale multi-channel systems [8]. However, the use of external reference resistors for calibration becomes impractical as the number of channels scales to thousands. Similarly, the chopping method for gain averaging is unsuitable for designing a multi-channel neural recording IC, as it introduces significant structural complexity that grows with the increasing number of channels.

To address these challenges, this study proposes the design of a digital unit integrated within the chip for noise and gain calibration. In this system, the initial noise level was measured to adjust the current of each channel, aiming to equalize the noise levels across channels. Unlike previous studies [5-7], this method offers the advantage of being processed in the digital domain, eliminating the need for additional processing even when the number of channels increases to thousands, while also efficiently reducing channel variations through periodic calibration instead of requiring continuous maintenance over time.

The ultimate goal of this study is to develop a neural recording system capable of monitoring electrocorticogram (ECoG) signals in real time over the life cycle of freely moving experimental animals. This paper presents a system capable of neural recording and stimulation, enabling multiple experimental animals to move freely during experiments. The recording module is designed specifically for ECoG signals, targeting a frequency band of 0–500 Hz. Additionally, the system incorporates wireless transmission of neural signal data from multiple subjects.

Key components of the system, including the high-dynamic-range neural recording module, LED-based communication circuit, and noise calibration logic, are detailed in Section II. Simulation and experimental results related to the circuit are discussed in Section III.

II. DESIGN METHODOLOGY

A. Circuit Design Implementation

Fig. 1 illustrates the overall conceptual framework of this study. The aim is to enable real-time monitoring of ECoG data from freely moving experimental animals using a miniaturized, modular neural signal monitoring system throughout their entire life cycle. An IC chip implanted in the animals measures neural signals, which are encoded and wirelessly transmitted to an external device via an LED-based communication module. This system establishes a novel experimental environment and provides a foundation for long-term observations in neuroscience research. The power system for this design will employ a setup capable of

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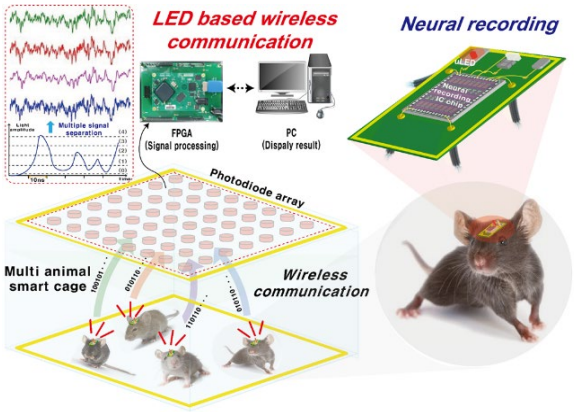
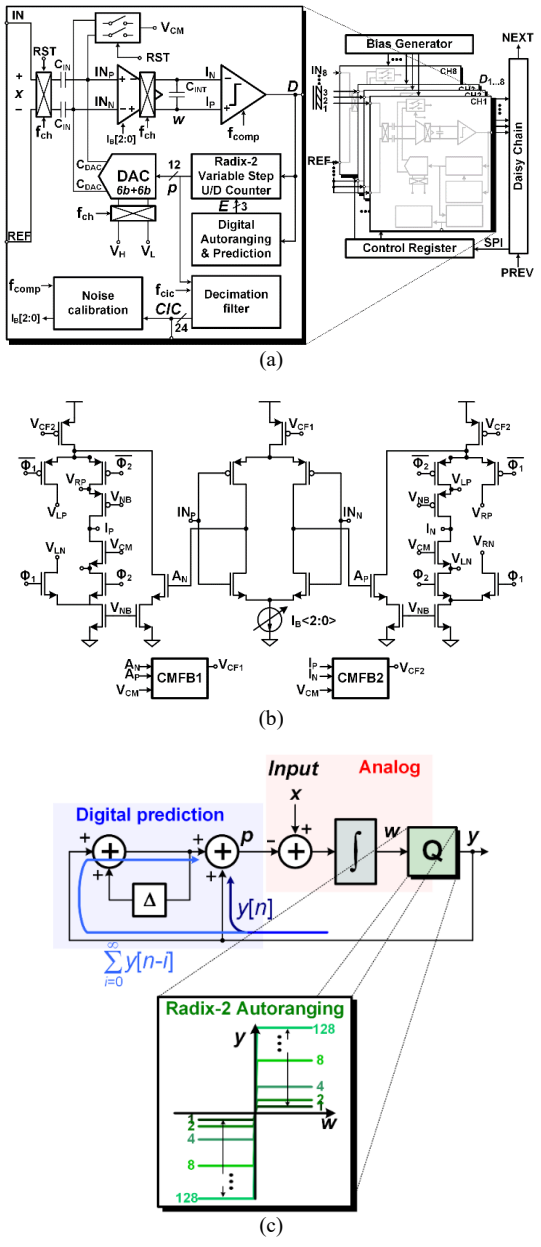


Fig. 1. Proposed neural monitoring system for freely moving animals.



(a)

(b)

(c)

Fig. 2. Overall ADC structure for ECoG recording: (a) an 8-channel ADC with CIC filter and noise calibration logic, (b) noise-dependent current-tunable integrator, and (c) auto-ranging digital prediction structure employed to track rapid large artifact inputs.

delivering power into the circuit within the cage [9]. However, this paper focuses primarily on describing the recording system.

The overall system structure is shown in Fig. 2. (a). To minimize channel-to-channel variations, the system measures the noise level generated by the chip at the start of operation. The designed IC utilizes a delta-sigma (ΔΣ) ADC architecture. With oversampling, the ΔΣ ADC shapes quantization noise into higher frequencies through noise shaping. As a result, the ADC's noise performance in the low-frequency band (relevant for ECoG) is determined primarily by the thermal noise of the integrator.

To ensure consistent noise levels across channels, the system incorporates noise calibration logic, which adjusts the current in the integrator, as illustrated in Fig. 2. (b). The amplifier used in the first stage employs a current reuse architecture. As previously mentioned, minimizing the integrator's noise is critical for improving the overall ADC performance. Therefore, to achieve a high gm/Id, the first stage was designed using this architecture.

The level of thermal noise was designed to be comparable to the shifted quantization noise (Qnoise). Considering the system gain, the input-referred Qnoise of a 12-bit system is calculated to be 34.8 μV_{rms}. With a second-order delta-sigma modulator (DSM) and an oversampling ratio (OSR) of 64, noise shaping reduces the Qnoise in the 0–500 Hz band to 544 nV_{rms}. This value is based on the assumption of an ideal integrator; however, in practical implementations, perfect noise shaping is not achievable, leading to a higher actual Qnoise. Accordingly, the integrator used in this design was configured to have an input-referred noise of 603 nV_{rms}, slightly higher than the ideal case. This design choice was validated through Cadence simulations, which confirmed that further reducing the thermal noise would have a negligible impact on overall performance.

For the first stage's common-mode feedback (CMFB), a transconductance-based CMFB structure was implemented to regulate the common-mode voltage. This configuration was chosen due to its high linearity, which is particularly advantageous in the first stage, where the gain is relatively low. In the second stage, a folded cascode architecture was adopted to accommodate the required gain of over 90 dB, ensuring a wide output swing range. Additionally, due to this wide swing requirement, a resistor-based CMFB utilizing a pseudo resistor was employed instead of the transconductance-based CMFB used in the first stage. Since the circuit is implemented using a resistor-based CMFB, it can be sensitive to mismatch, which may cause the common-mode voltage to shift from 500mV to 510mV or 480mV. However, the second-stage output is fed into the differential comparator, and while this may affect the output range of the integrator, it does not critically impact the overall operation. This was verified through simulations by varying the common-mode voltage before implementation. The design allows for the external configuration of the integrator's capacitor with values of 400f or 800f, and accordingly, the dominant pole can be set to 1k or 1.8k.

The system employs an auto-ranging digital prediction

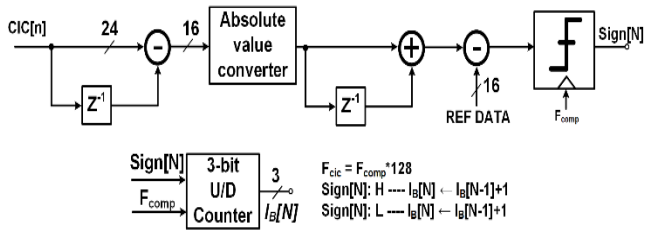


Fig. 3. The logic utilizes the continuous absolute difference of the CIC output values to estimate the level of noise. During calibration, this information is used to determine the amount of current for the integrator.

feature to enable rapid detection of transient neural signal changes, as shown in Fig. 2. (c) [10]. This feature dynamically adjusts the quantizing range based on the signal's characteristics. The prediction algorithm (PDA) monitors the sign of the signal output changes (sign(Δ Out[n])). When the input signal exhibits large variations, the output sign remains consistent. The system increases the quantizing range if the output sign remains constant for at least four iterations. Conversely, if the range exceeds the actual signal variation, causing the output sign to alternate more than three times, the logic reduces the quantizing range. This adaptive adjustment, distinct from conventional ADCs, allows the system to more rapidly and accurately capture momentary neural signal changes.

The sampling frequency of the recorded data is increased through oversampling at a rate that is a multiple of the Nyquist sampling rate, referred to as the oversampling rate (OSR), to reduce quantization noise. However, to improve efficiency, the oversampled data is not directly transmitted externally. Instead, it undergoes down-sampling, where the oversampled frequency is divided by the down-sampling rate (D). During down-sampling, shaped high-frequency noise is aliased into lower frequencies, which can degrade signal quality. To mitigate this, a low-pass filter (LPF) is applied before down-sampling to remove high-frequency noise.

The combination of the LPF and the down-sampling process is known as a decimation filter. One commonly used structure for decimation filters is the cascade integrator-comb (CIC) filter. A CIC filter consists of integrators, a down-sampler, and differentiators, with the number of stages determining the filter's order. The CIC filter is particularly advantageous due to its hardware-efficient design, as it eliminates the need for multipliers or memory [11]. Consequently, we adopted the CIC filter for the decimation process. The frequency response of the CIC filter exhibits a low-pass filter characteristic, attenuating signals at a rate of 40 dB per decade. This feature effectively reduces aliasing noise during the down-sampling process, ensuring high-quality signal processing.

The data processed through the CIC filter is transmitted to the external environment via optical communication using LEDs. To facilitate the reception of data from multiple animals, each recorded dataset is encoded before being transmitted to the LED driver integrated into the chip. With the ADC OSR set to 64, the operating frequency of the CIC filter is 1 kHz. The CIC filter outputs 24-bit data, which is encoded into a 32-bit format for each of the 8 channels. This serialized data is then transmitted to the LED at a frequency of 6.144 MHz. The selection of a 6.144 MHz operating frequency in this system was based on the design requirements of a 1 kHz CIC filter. Since the system needs to decode 8-channel, 24-bit CIC data using a 32-bit Gold code, LED communication was implemented at 6.144 MHz to accommodate these constraints efficiently. In this study, the CODE of the LED used is set to a 50:50 ratio of 0s and 1s, allowing the efficiency to be calculated as half of the LED that remains continuously lit. For the target micro LED (TCE14-660), which consumes 11mW, it is estimated that the power consumed by the LED communication will be within 6mW. The BLE 5.0 (nRF52840), known for its low power consumption, is capable of transmitting up to 2Mbps, requiring approximately 30mW of power for this operation. Therefore, the proposed system can transmit more than three times the data volume of conventional BLE while consuming only one-third of the power.

The LED's optical output is captured by a photodiode positioned above it, as depicted in Fig. 1. The photodiode signal is digitized by an external ADC, and the decoded data is reconstructed by an FPGA to recover the original information.

To reduce channel mismatch, several techniques can be employed, including designing the circuit to allow external control of the gain using passive components or utilizing a resistor degeneration method to minimize variations in transconductance [12]. Another effective approach is the application of Dynamic element matching (DEM) to reduce gain errors. In current-feedback instrumentation amplifiers (CIFA), the mismatch between the transconductance in the signal path and the transconductance in the feedback path determines the system's overall gain errors. To address this, the DEM technique is employed by swapping the transconductance of the feedback and signal paths, effectively mitigating the mismatch between the transconductances [13]. For multi-channel circuits, a common method to minimize inter-channel variations is to average the gain across all channels. By employing a group chopping technique, the circuit is designed such that all amplifiers in each channel are processed within a single clock cycle. As a result, the output of each sample is defined as the average gain of all channels.

While the aforementioned studies demonstrate the feasibility of reducing mismatch in circuits with a small number of channels, this approach becomes increasingly challenging when scaling to systems with thousands of channels. Utilizing the average gain of all amplifiers in such large-scale systems is impractical due to the increased complexity and resource requirements.

The structure of the noise calibration logic is detailed in Fig. 3. Initially, the input is shorted to VCM, and the logic calculates the ADC noise by summing the absolute differences between consecutive CIC output values. After computing the noise level, it is compared to a predefined reference value from simulations. Based on this comparison, the system adjusts the integrator current to either increase or decrease it. This design ensures consistent noise levels across all channels in the system, reducing variability and enhancing reliability.

III. RESULTS AND DISCUSSION

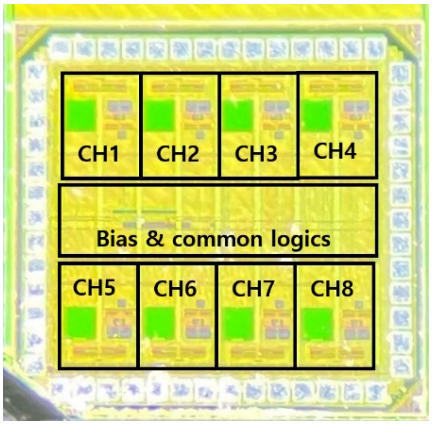
A. Measurements

Fig. 4. (a) represents the chip diagram. A 65-nm CMOS process was employed, and the total area occupied is 1mm^2. Each channel consists of an ADC, a noise calibration block, and a CIC filter. Fig. 4. (b) illustrates the experimental setup for the overall ADC performance test. To minimize external noise, a Faraday shield was fabricated and used during the ADC experiments. The master clock and output data from the chip were managed using an FPGA (XEM6310). The chip's input signal was generated using APX526. The previous chip faced operational issues due to the recording system's loop operating as positive rather than negative feedback. In the case of this new chip, improvements were made to ensure that the ADC operates properly by addressing and rectifying this issue.

When a 10Hz 1mV$_{rms}$ sine wave signal was input, the ADC output before the CIC filter and the CIC output are shown in Fig. 5. (a). The CIC output represents the result after decoding each coded data. As evident from the figure, both the CIC output and the ADC output show minimal differences, indicating successful signal restoration. Fig. 5. (b) depicts the FFT results, demonstrating the characteristics of the CIC filter where the sinc function is observed due to the filtering process. When using a PDA, allows for faster tracking of rapidly changing inputs by adjusting the quantizer's step size. Fig. 6. illustrates the ADC output values with and without the use of PDA when the square pulse input is set to 10Hz with a 5mV$_{pp}$ amplitude. As depicted in the figure, it can be observed that without the use of a PDA, the system tends to follow the input more slowly compared to when a PDA is utilized. Fig. 7 illustrates the Signal-to-Noise and Distortion Ratio (SNDR) of the ADC output before the CIC and after passing through the CIC filter for various input signals.

B. Discussion

Fig. 8 illustrates the noise output with varying integrator bias current for different sampling frequencies. If the overall system noise were determined by the thermal noise of the integrator, an increase in the bias current would be expected to reduce the overall noise. However, as observed in the figure, noise is present regardless of the bias current. Additionally, an overall improvement in noise performance with an increasing sampling rate. If the system were dependent on the thermal noise of the integrator, an increase in the sampling rate should not affect the noise performance. Therefore, it is hypothesized that the system is not dominated by the integrator's noise but rather by Quantization noise or issues related to the differential non-linearity (DNL) of the bridge cap DAC used during the design. The bridge cap DAC, due to its non-integer values in the connected capacitor, may result in performance degradation under PVT variations. However, the narrower fluctuation with higher sampling rates might suggest that the impact of DNL-induced noise performance degradation is less pronounced at higher sampling rates compared to lower rates. To address this, future designs will consider using a DAC in a form other than the bridge DAC.



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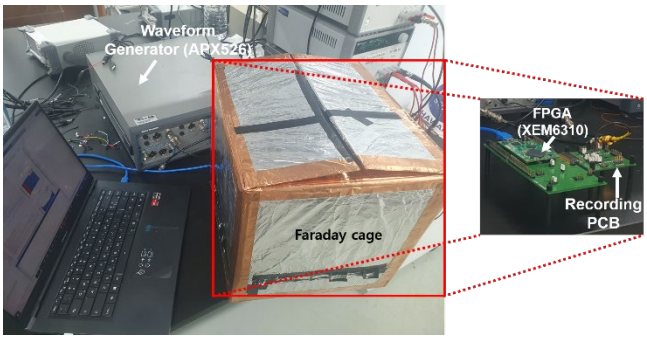
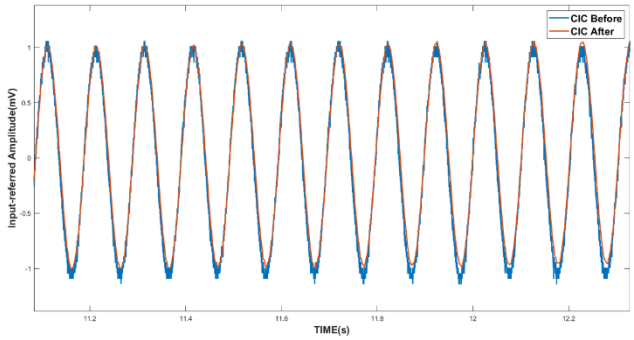


(b)

Fig. 4. (a) 8CH neural recording IC micrograph, and (b) Measurement setup for the performance test.



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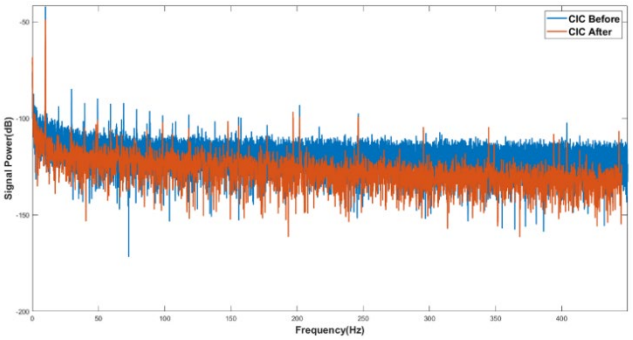


(b)

Fig. 5. ADC test output when a 10Hz sine wave with 1mV$_{rms}$ amplitude is applied to the input. (a) Reconstructed ADC output before and after CIC filter (b) FFT output of each data.

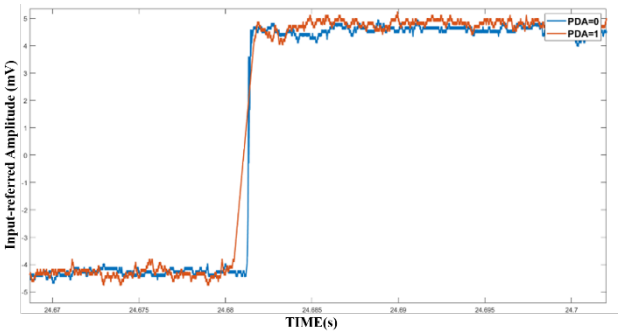


Fig. 6. Comparison of output depending on whether PDA is used or not.

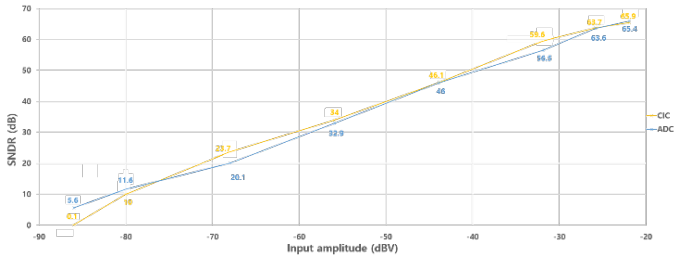


Fig. 7. Comparison of the output values SNDR according to various input signal sizes.

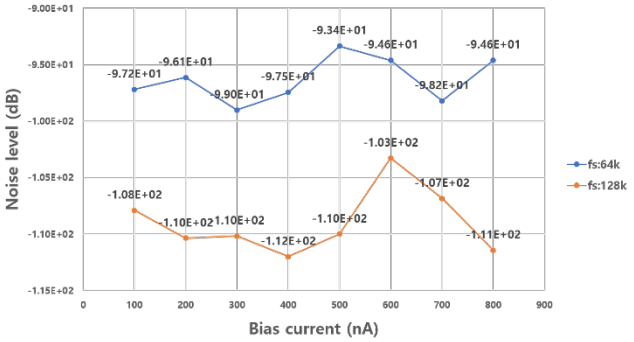
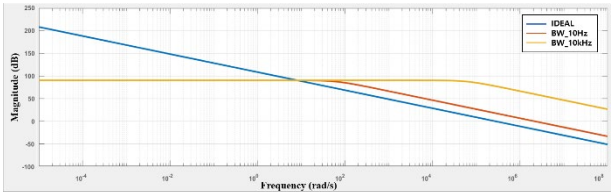
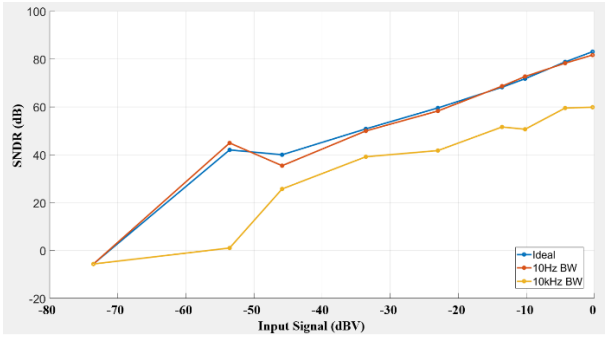


Fig. 8. Comparison of noise measurement results according to bias current.



(a)



(b)

Fig. 9. ADC Comparison of first-order DDSM performance based on the type of integrator: (a) frequency characteristics of the integrator used in MATLAB Simulink, and (b) SNDR variation with input signal for different integrators when the input signal frequency is 500 Hz.

Another factor considered in this study is the bandwidth of the integrator used. In the case of a leaky integrator, achieving performance similar to that of an ideal integrator requires designing the integrator corner frequency to be significantly lower than $\frac{f_{bw}}{\sqrt{3}}$ [14]. Substituting the required f_{bw} into the previously mentioned equation, the integrator should have a corner frequency significantly lower than 288 Hz. A 1st order delta-delta sigma modulator (DDSM) was implemented in MATLAB Simulink. To represent the leaky integrator, the integrator's corner frequency was designed differently, as shown in Fig. 9. (a). When input signals with various frequencies around 500 Hz were applied, the signal-to-noise-and-distortion ratio (SNDR) was observed to vary depending on the type of integrator as illustrated in Fig.9. (b).

In the proposed design integrator, the corner frequency of the integrator was set at 1.6 kHz, which is significantly higher than the required corner frequency mentioned earlier. Consequently, in the designed ADC, quantization noise was not effectively shaped toward high frequencies, leading to performance degradation. This is believed to be a key reason why the designed ADC failed to exhibit optimal performance during noise testing.

IV. CONCLUSION

The designed IC chip, fabricated using a standard 65 nm CMOS process, occupies an area of 1 mm² and includes 8 channels. By employing delta-sigma (ΔΣ) structures and auto-ranging algorithms, the chip is capable of measuring neural signals even in the presence of large stimulation artifact signals, a significant improvement over amplifier-based structures. The measured data is transmitted externally via an LED-based communication system. However, the designed noise calibration logic did not function as intended due to increased noise flow, attributed to issues such as DAC mismatch or bandwidth of integrator. Moving forward, we plan to address these challenges and proceed with a redesign to ensure the proper functionality of the calibration logic.

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