A Fast Adaptive and Fine Stabilizer Based Digital LDO

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***Abstract* - In this brief, a fully integrated digital low-dropout regulator (DLDO) is proposed to address the trade-offs between transient response and power efficiency in dynamic load conditions. The design features a fast-adaptive glitch-driven coarse loop controller, which rapidly adjusts PMOS switches using precisely generated pulses, minimizing transient recovery time (T_{REC}) even during large load current (I_{LOAD}) changes. Additionally, a fine voltage stabilizer ensures steady-state voltage stability by employing high-resolution PMOS control. The DLDO is fabricated in a 65-nm CMOS process, the proposed DLDO supports an input voltage range of 0.6 V to 1.2 V and achieves a regulated output voltage from 0.55 V to 1.15 V. Simulation results demonstrate a 264 mV voltage droop recovery within 19.11 ns for a 26 mA load step, achieving a figure-of-merit of 0.225 ns² and a peak current efficiency of 99.32%. The low quiescent current of 157 µA makes it highly suitable for power-efficient SoC applications requiring both fast transient response and precise voltage regulation.**

***Keywords*— digital low-dropout regulator (DLDO), Fine voltage stabilizer, fast transient, Glitch-driven control**

I. INTRODUCTION

Low-dropout regulators (LDOs) are indispensable components in modern power management systems, ensuring stable power delivery for sensitive electronic applications [1]. They play a critical role in system-on-chip (SoC) platforms, which demand efficient point-of-load power delivery while adhering to strict integration and performance requirements. To meet these demands, LDOs must provide fast transient responses, maintain steady-state voltage stability, and operate within compact form factors compatible with advanced CMOS technologies. While conventional analog LDOs have served these purposes, their limitations in scalability and power efficiency under dynamic conditions have prompted a shift towards fully integrated digital LDOs (DLDOs) [2].

DLDOs offer several advantages over their analog counterparts, such as design simplicity, scalability, and compatibility with CMOS scaling trends. These attributes make them particularly attractive for applications ranging from microampere to sub-ampere load currents in both consumer electronics and industrial systems [3]. However, existing DLDO architectures face significant challenges when deployed in dynamic load conditions. One of the primary issues is the trade-off between transient response and power efficiency [4], [5]. Conventional DLDO architectures, as illustrated in Fig. 1, rely heavily on clocked comparators and fixed-frequency controllers to regulate the output voltage, which introduces delays in transient response and increases quiescent current (I_Q), especially during low-power operation modes. These limitations make conventional designs unsuitable for advanced SoC platforms that demand both high performance and low energy consumption [6]–[8].

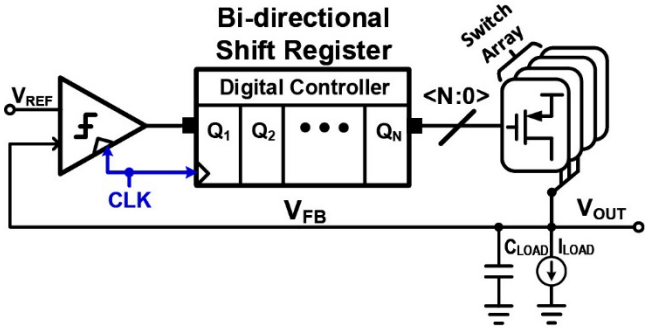

Fig. 1. Block diagram of the first implementation of a digital Low-Dropout Regulator (LDO)

Several innovative approaches have been proposed to overcome these challenges. For example, Kang et al. introduced an event-driven DLDO architecture that eliminates clock dependencies, resulting in faster transient responses. However, this approach requires sophisticated event-detection mechanisms, which significantly increase circuit complexity and power overhead [9]. Similarly, Nasir et al. proposed a dual-loop control strategy consisting of a high-speed coarse loop to handle large load changes and a slower fine loop for steady-state adjustments. While effective, this method still depends on clocked control systems, which limit its responsiveness to highly dynamic load conditions [10]–[14]. These prior works highlight the critical need for DLDO designs that balance transient performance, power efficiency, and circuit simplicity.

In response to these challenges, this study proposes a glitch-driven coarse loop controller for coarse regulation in DLDOs. By leveraging precise glitch pulses generated from changes in the lock signal of the Voltage Range Detector, the proposed controller rapidly adjusts the state of PMOS switches.

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Manuscript Received Jan. 24, 2025, Revised Mar. 7, 2025, Accepted Mar. 11, 2025

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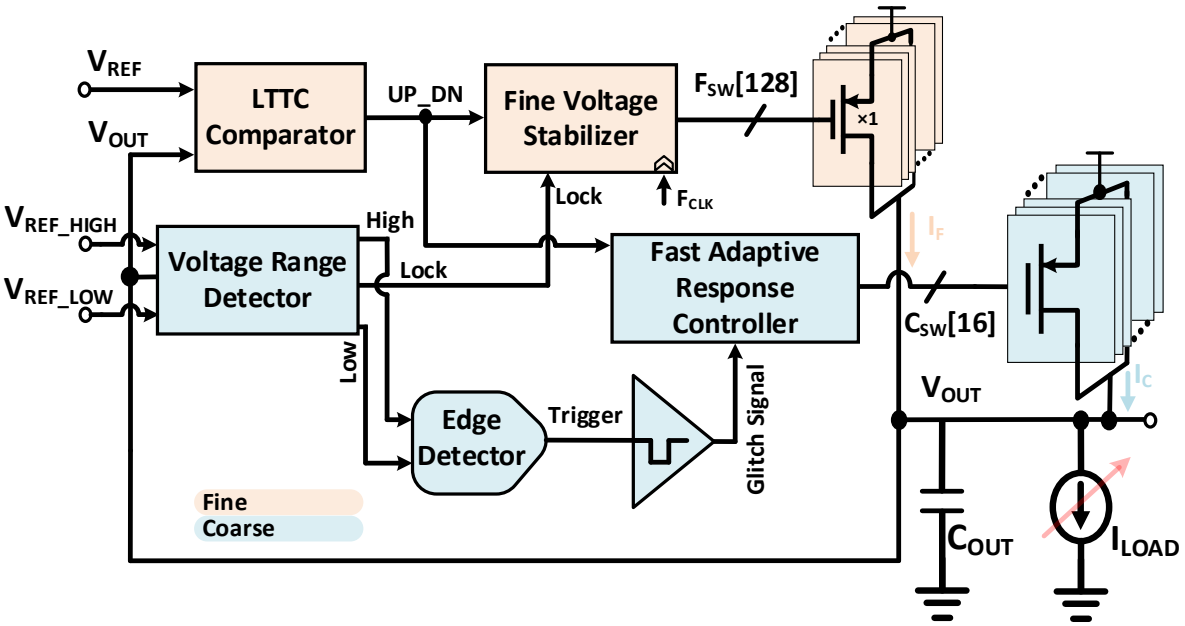

Fig. 2. Block diagram of the overall proposed digital LDO.

This mechanism significantly reduces the transient recovery time (T_{REC}) of (V_{Droop}), even during large (I_{LOAD}) transients, and addresses the limitations of conventional clocked designs. Additionally, the integration of a dual-loop system, consisting of a coarse loop for rapid voltage adjustments and a fine-tuned loop for precise regulation, enables improved load transient response and recovery time.

The remainder of this article is structured as follows. Section II introduces the proposed digital low-dropout regulator (DLDO) architecture, detailing its overall block diagram and the functionality of the proposed blocks. Section III presents the simulation results, offering a detailed analysis of the key performance metrics, including transient recovery time, line regulation, and load transient response. Section IV concludes the paper by summarizing the key contributions of the proposed DLDO design and discussing its potential impact on power management for modern SoCs.

II. DESIGN METHODOLOGY

A. Overall Block Diagram

The proposed Digital Low-Dropout Regulator (DLDO) system, illustrated in Fig. 2, is designed to address dynamic voltage regulation challenges through an integrated framework of advanced control methodologies and circuit components. The architecture comprises a Logic Threshold Trigger Comparator (LTTC), Voltage Range Detector, Edge Detector, Glitch Generation Block, Fast-Adaptive Response Controller for coarse regulation, and a Fine Voltage Stabilizer. Each block is meticulously engineered to ensure a fast-transient response and precise voltage regulation, collectively contributing to a robust and energy-efficient power management solution.

The operation of the DLDO system is best understood through the accompanying timing diagram, which captures the transient response following a sudden change in load current ($I_{_LOAD}$). When (V_{OUT}) drops below the lower reference threshold (V_{REF_LOW}) due to an increased load, a voltage droop (V_{DROOP}) occurs. The LTTC detects this deviation and generates a UP_DN signal to indicate the need for corrective action. Simultaneously, the Voltage Range Detector identifies whether (V_{OUT}) has crossed the predefined reference voltage range, triggering the Edge Detector, which subsequently generates a Trigger signal.

In response, the Glitch Generation Block produces precisely timed glitch pulses that activate the Fast-Adaptive Response Controller, initiating the coarse regulation loop. This loop dynamically engages multiple PMOS switches to restore (V_{OUT}) to the desired level. As depicted in the Fig. 3, timing diagram, a sequence of glitch pulses is generated during the transient state, expediting the voltage correction process. Once (V_{OUT}) stabilizes within the acceptable range, the system transitions to steady-state operation, where the Fine Voltage Stabilizer takes over, performing high-precision adjustments to maintain (V_{OUT}) equal to the (V_{REF}).

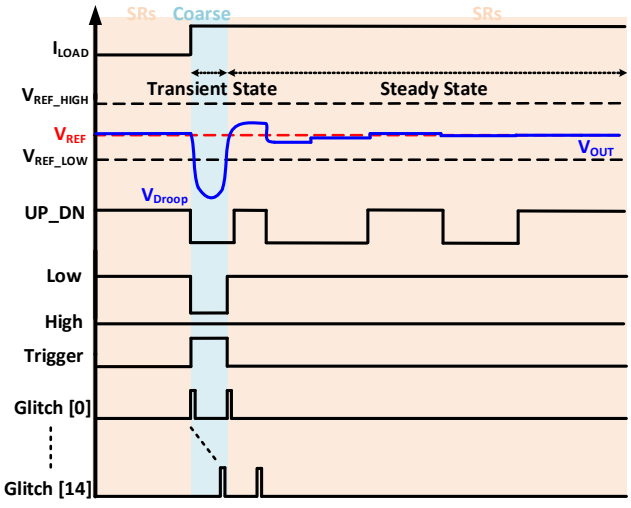

Fig. 3. Operational waveform of the proposed digital LDO.

B. LTTC Comparator

The Logic Threshold Trigger Comparator (LTTC) functions as the primary sensing mechanism, continuously comparing the output voltage (V_{OUT}) with the reference voltage (V_{REF}). The comparator generates a UP_DN signal, providing directional guidance for voltage adjustments. This real-time feedback is pivotal for maintaining system stability and mitigating transient deviations as shown in Fig. 4.

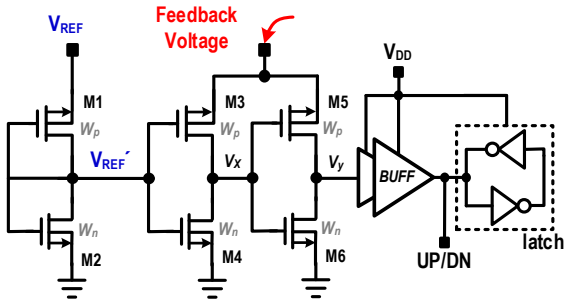

Fig. 4. Schematic of the LTTC-based comparator.

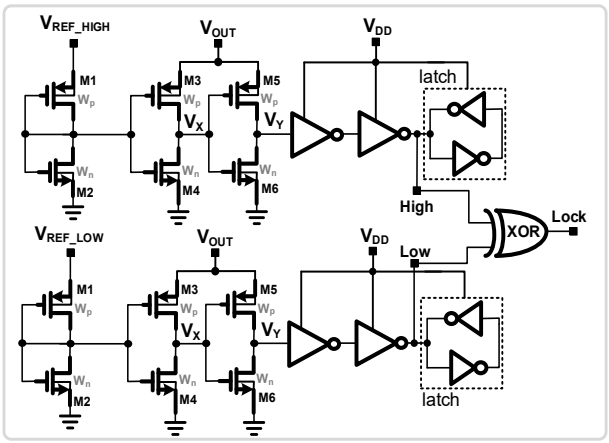

Fig. 5. Schematic of the LTTC-based comparator.

C. Voltage Range Detector

The Voltage Range Detector extends the monitoring capabilities by comparing (VOUT) against predefined thresholds voltage, (VREF_High) and (VREF_Low). This comparison generates three critical signals: (High), (Low), and (Lock), as shown in Fig. 5, which collectively indicate whether (VOUT) is within the desired operational range. The lock signal serves as a central control indicator, guiding the activation of appropriate control loops to enable both rapid corrective action and fine-tuned voltage adjustments.

D. Edge Detector

The Edge Detector is responsible for identifying transitions in the High and Low signals, which indicate variations in V_{OUT} due to dynamic load conditions. It continuously monitors these signals and detects state changes, whether from high to low or low to high.
Upon recognizing such transitions, the Edge Detector generates a Trigger signal, which serves as an essential input to the Glitch signal block. By accurately capturing these transitions, the Edge Detector ensures that the system responds promptly to fluctuations in V_{OUT}, enabling precise activation of the voltage regulation mechanism.

E. Dynamic Control System for Fast and Stable Voltage Regulation

The proposed digital LDO features a dual-loop control system consisting of a Fast-Adaptive Response Controller and a Fine Voltage Stabilizer controller. These subsystems work in tandem to effectively manage dynamic voltage scaling, providing both fast transient response and precise steady-state voltage regulation. This collaboration enables the LDO to handle substantial load variations while ensuring the stability of the output voltage (V_{OUT}) with high accuracy. The architecture of the Fast-Adaptive Response Controller is depicted in Fig. 7. The Fast-Adaptive Response Controller is responsible for coarse voltage adjustments during transient events where (V_{OUT}) deviates significantly from the reference voltage range. When (V_{OUT}) falls outside this range, a trigger is activated by the voltage range detector comparator, which identifies whether (V_{OUT}) is too high or too low. Based on this, the edge detector turns the Fast-Adaptive Response Controller on or off, by generating a precise glitch pulse. These signals are fed into the controller's asynchronous logic, driven by a glitch generator that produces a clockless short pulse with a fixed pulse width to trigger a series of D flip-flops (DFFs) in the control path. Each D flip-flop (DFF) controls a segment of the PMOS driver circuit, enabling or disabling individual PMOS switches in the segmented array. The PMOS driver ensures that the PMOS switches remain OFF during startup, preventing unintended activation and excessive power dissipation. Once the system transitions from startup to active regulation, the PMOS driver responds to control signals from the adaptive controller, selectively activating the appropriate number of PMOS switches to regulate (V_{OUT}) efficiently. This controlled activation mechanism prevents sudden voltage spikes and enhances the overall stability of the DLDO system. The segmented PMOS array is a critical component of the coarse control mechanism. It consists of

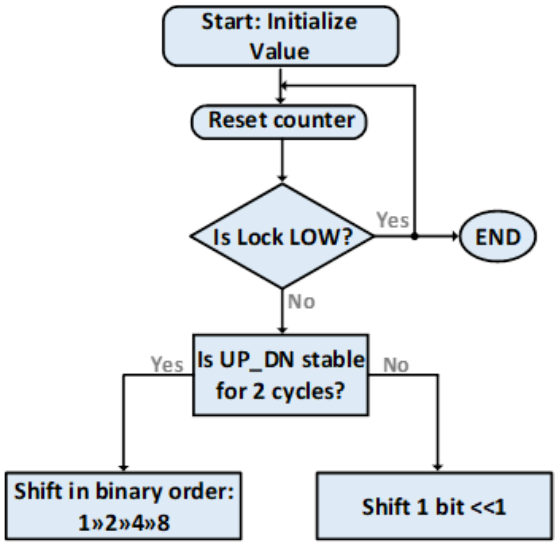

Fig. 6. Flowchart of the proposed fine stabilizer controller.

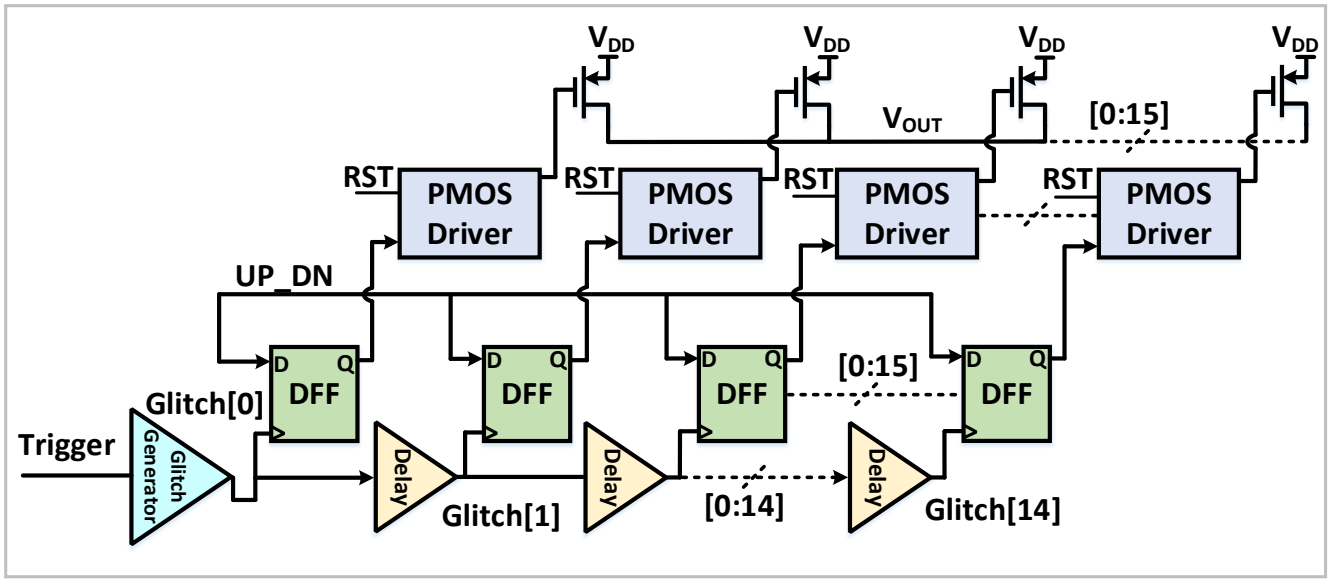

Fig. 7. Schematic diagram of the proposed fast adaptive response controller.

16 PMOS switches, each responsible for supplying a specific amount of current based on which segment is activated. During a transient event, such as a sudden increase in load current (I_{LOAD}), the controller activates multiple PMOS switches simultaneously, allowing substantial current to flow and quickly restore (V_{OUT}) to the desired level. Once the transient is addressed and (V_{OUT}) stabilizes near the reference voltage range, the controller transitions to fine control, which.is managed by the Fine Voltage Stabilizer to maintain precise stability. The flowchart for the Fine Voltage Stabilizer, as depicted in Fig. 6, demonstrates a structured approach for achieving precise voltage adjustments during steady-state operation. The fine stabilizer controller follows a structured sequence to regulate (V_{OUT}) effectively. First, the controller initializes, preparing the system for voltage regulation. Following this, the reset counter is activated, clearing any previous values to ensure a fresh start for the control process. This reset step is essential for maintaining accuracy in subsequent voltage adjustments. After resetting, the system evaluates the Lock signal, which determines whether (V_{OUT}) is within the acceptable range. If the Lock signal is (LOW), it signifies that no further voltage correction is needed, and the process is terminated. However, if Lock remains (HIGH), indicating a deviation from V_{REF}, the controller proceeds to analyze the behavior of the (UP_DN) signal over two clock cycles to decide the appropriate adjustment mode. The fine stabilizer operates in two distinct modes, depending on the stability of the (UP_DN) signal. If (UP_DN) remains constant for two consecutive clock cycles, it indicates that (V_{OUT}) is significantly above or below (V_{REF}), suggesting a large deviation that requires a rapid correction. In this case, the system applies binary order shifting, where the adjustment step size increases progressively, following the sequence (e.g., 1 → 2 → 4 → 8). This approach enables a faster response to significant voltage deviations, expediting the recovery process. On the other hand, if (UP_DN) fluctuates within two clock cycles, it suggests that (V_{OUT}) is approaching (V_{REF}) and requires more precise control to avoid excessive correction. In this scenario, the system applies a 1-bit-at-a-time shift, ensuring finer voltage regulation and preventing overshoot.

III. RESULTS AND DISCUSSION

The proposed Fast Adaptive Response-based digital LDO was designed in a 65 nm CMOS process, occupying an active area of 0.098 mm², as shown in Fig. 8. This design achieves regulated output voltage (V_{OUT}) in the range of 0.55 V–1.15 V with a dropout voltage (V_{DO}) as low as 50 mV, demonstrating excellent performance metrics in both steady-state and transient response. The load current (I_{LOAD}) is regulated over a wide range from 500µA to 22mA, while maintaining a compact design and competitive performance across key parameters, including recovery time, voltage ripple, and line regulation.

The line regulation performance of the proposed Fast Adaptive Response-based digital LDO is depicted in Fig. 9. The simulation evaluates the ability of the output voltage (V_{OUT}) to maintain stability in response to variations in the

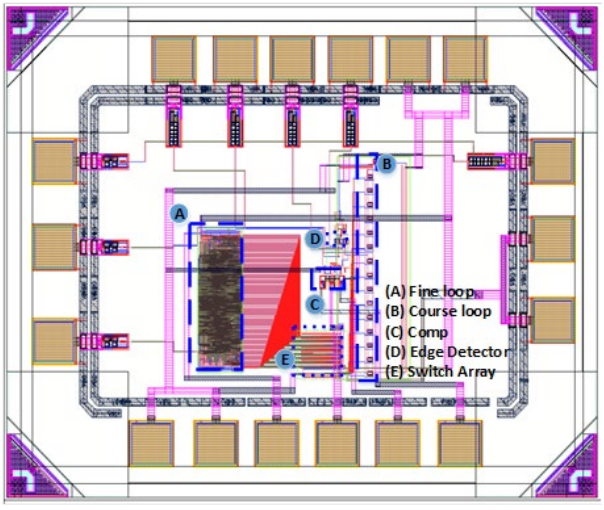

Fig. 8. Chip layout of the proposed adaptive response digital LDO.

supply voltage (V_{DD}) while the reference voltage (V_{REF}) is held constant at 1.05 V. During the test, (V_{DD}) is varied from 1.1 V to 1.2 V and then back to 1.1 V. The results show that (V_{OUT}) remains closely aligned with (V_{REF}), with only minimal deviations observed during the transition.

The calculated line regulation is approximately 0.70 mV/V, indicating a strong ability of the proposed design to suppress supply voltage disturbances. This performance is achieved through the integration of the fast-adaptive response controller and fine voltage stabilizer, which dynamically adjust the PMOS switches to counteract any variations in (V_{DD}). The smooth response of (V_{OUT}) with negligible ripple further demonstrates the robustness of the proposed architecture.

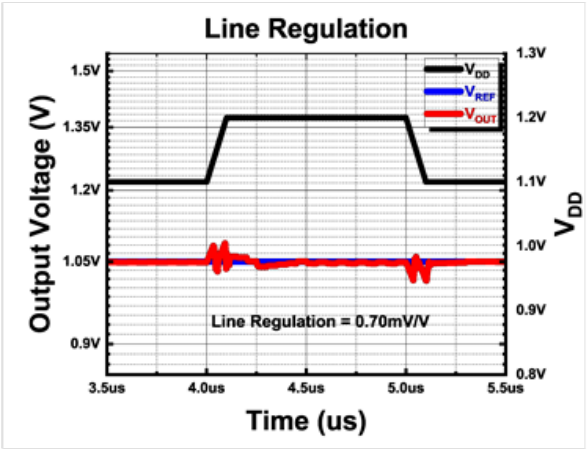

Fig. 9. Simulated line regulation of the proposed digital LDO.

This superior line regulation highlights the capability of the proposed digital LDO to provide consistent output voltage across a wide range of supply voltage variations. Such performance is essential for power management systems in SoCs, ensuring reliable operation even under fluctuating power supply conditions.

The load transient response of the proposed Fast Adaptive Response-based digital LDO is demonstrated in Fig. 10. This simulation evaluates the output voltage (V_{OUT}) behavior under a step load current (I_{LOAD}) transition from 0 mA to 24 mA. At the onset of the load step, (V_{OUT}) experiences a

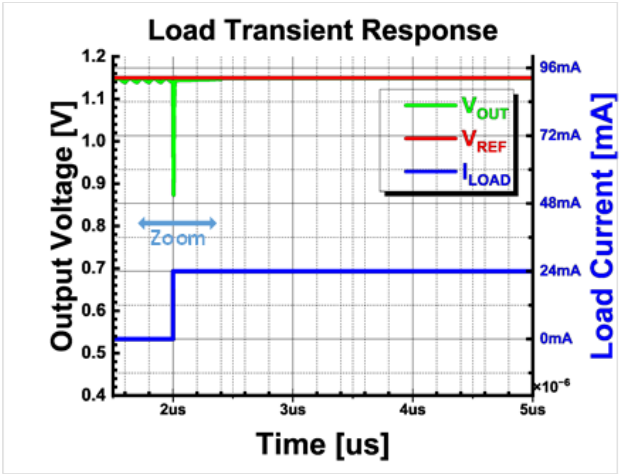

Fig. 10. Simulated load transient response of the proposed digital LDO.

temporary undershoot of 275 mV due to the rapid increase in (I_{LOAD}). However, the proposed architecture ensures a fast recovery, with (V_{OUT}) stabilizing to the reference voltage (V_{REF}) within a transient recovery time of 19.1 ns. This rapid recovery is attributed to the Fast-Adaptive Controller, which dynamically adjusts the PMOS switches to counteract the voltage dip effectively. In the broader context depicted in Fig. 11, (V_{OUT}) remains stable and closely tracks (V_{REF}) after the transient state, maintaining output regulation despite the significant load current variation. The steady-state performance demonstrates the robustness of the proposed

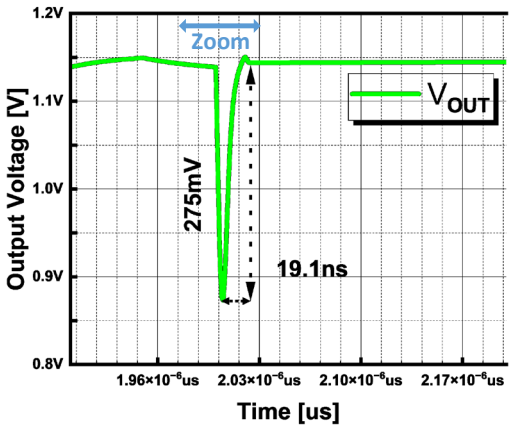

Fig. 11. Simulated zoom part of the load transient response.

design in mitigating ripple and ensuring minimal deviation from (V_{REF}).

These results underscore the superior transient response capability of the proposed LDO, achieving both minimal undershoot and fast recovery, which are critical for modern power management ICs in dynamic operating environments.

The performance of the proposed fast-adaptive response-based digital LDO is compared with recent state-of-the-art digital LDOs as shown in Table I, unlike conventional designs, the proposed LDO demonstrates substantial improvements in key performance metrics while maintaining a minimal output capacitance of 0.1 nF.

The evaluation is based on two critical figures of merit (FOM_1 and FOM_2), highlighting the superiority of the proposed approach. The proposed design achieves a transient recovery time (T_{REC}) of 19.11 ns for a voltage undershoot of 264 mV during a load current step of 22.4 mA, significantly outperforming the designs in [15], [16], and [17]. Additionally, the FOM_2 of the proposed design is remarkably low at 0.225 ns^2, which is substantially better than the values reported in [15], [16], [17] and [18]. This demonstrates the efficiency of the adaptive search controller in delivering faster recovery times with minimized energy costs. Despite its compact size, with an active area of just 0.098 mm^2, the proposed LDO achieves high performance across all metrics, making it a suitable choice for modern system-on-chip (SoC) applications. The comparative analysis underscores the balance achieved by the proposed design in minimizing recovery time, reducing undershooting, and maintaining high efficiency, establishing it as a leading solution among state-of-the-art digital LDOs. remarkably

TABLE I. Performance Comparison of the Proposed Fast-Adaptive Response-Based Digital LDO with State-of-the-Art Designs.

	This Work	[15]	[16]	[17]	[18]
Process [nm]	65	3 GAAFET	65	65	65
Topology	Adaptive + SRs	TEC Distributed	Adaptive Sampling	PID	AS+CEA
V_{DD} [V]	0.6–1.2	0.55–1.1	0.6–1.2	0.7–1.3	0.6–1.2
V_{OUT} [V]	0.55–1.15	0.5–1.05	0.5–1.1	0.65–1.25	0.55–1.15
$I_{LOAD,\ MAX}$ [mA]	23	10000	62	80	26
C_{OUT} [nF]	0.1	320	0.1	0.0095	0.01
V_{OUT}[mV]@ ΔI_{LOAD}[mA]	264@22.4	94@6500	145@31.6	275@28	140@26
T_{REC}[ns]@ ΔV_{OUT} [mV]	19.11@264	200*@94	600*@145	60*@275	95@140
$\Delta I_{LOAD}T_{EDGE}$ [ns]	1	1	48	0.1	20
I_Q [uA]	157	18170	17.4	1050	167
Current Eff. [%]	99.32	99.82	99.99	99.75	99.6
FOM_1 [ps]	11.8	14.3	13.5	5.37	39.4
FOM_2 [ns²]	0.225	2.87	8.08	0.322	3.74
Active Area [mm ²]	0.098	0.038	0.0670	0.0925	0.075

* Estimated from measurement

$$FOM_1 = \frac{C_{LOAD} \times \Delta V_{OUT} \times I_Q}{\Delta I_{LOAD}^2} + \frac{T_{EDGE} \times I_Q}{2\Delta I_{LOAD}}$$

$$FOM_2 = FOM_1 \times T_{REC}$$

low at 0.225 ns², which is substantially better than the values reported in [15], [16], [17] and [18]. This demonstrates the efficiency of the adaptive search controller in delivering faster recovery times with minimized energy costs. Despite its compact size, with an active area of just 0.098 mm², the proposed LDO achieves high performance across all metrics, making it a suitable choice for modern system-on-chip (SoC) applications. The comparative analysis underscores the balance achieved by the proposed design in minimizing recovery time, reducing undershooting, and maintaining high efficiency, establishing it as a leading solution among state-of-the-art digital LDOs.

IV. CONCLUSION

Efficient power management in System-on-Chip (SoC) platforms faces increasing challenges due to aggressive device scaling and dynamic load conditions. This study presents a fast-adaptive digital Low-Dropout Regulator (DLDO) architecture that addresses these challenges with a clockless Logic Threshold Triggered Comparator (LTTC) for asynchronous feedback. The dual-loop control strategy combines a coarse loop for rapid voltage correction during transients and a fine stabilizer for precise steady-state regulation, significantly improving transient recovery time (T_{REC}) and minimizing output ripple while maintaining low quiescent current (I_Q). By eliminating clock dependencies and incorporating a glitch-driven control mechanism, the proposed DLDO demonstrates robust, energy-efficient performance across dynamic load conditions, making it highly suitable for next-generation SoC applications.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

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