A Resolution-Configurable Charge-Domain Capacitance-to-Digital Converter

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***Abstract* – This paper presents a semi-digital capacitance-to-digital converter (CDC) with an extended input capacitance range of up to 1 nF, leveraging a configurable charge subtraction capacitor and a current mirror-based discharger to maintain high resolution. The proposed CDC employs a single-slope discharge mirror technique to achieve energy-efficient operation while eliminating complex analog circuits such as operational transconductance amplifiers (OTAs). The current mirror-based discharger with a charging flag mechanism enables precise charge sensing by dynamically controlling the charging and discharging processes, ensuring accurate capacitance. Additionally, this structure reduces circuit complexity while maintaining measurement accuracy and extending the supported input capacitance range. The configurable charge subtraction capacitor array further enhances flexibility, making the design suitable for various capacitive sensing applications, including pressure, humidity, and touch sensing. Post-layout simulations in a 180 nm CMOS process demonstrate a consistent conversion time across a wide capacitance range while maintaining low power consumption. Measurement results confirm a minimum resolution of 10 fF for a 1 nF input capacitance with single slope regulation.**

***Keywords*—Capacitance-to-Digital Converter(CDC), Semi-Digital CDC, Capacitive Sensing System**

I. INTRODUCTION

Capacitive sensors are widely used to measure physical quantities such as pressure, humidity, proximity, position, and displacement by detecting changes in capacitance [1]. Traditionally, the analog output of these sensors is processed by front-end electronics and an external analog-to-digital converter (ADC). Recently, capacitance-to-digital converters (CDCs) have been adopted to eliminate the need for dedicated analog front ends, thereby reducing system complexity and power consumption [2]. A low-power CDC is particularly advantageous for batteries or energy-harvesting sensor applications. Furthermore, a CDC with a broad input capacitance range, spanning from small to large capacitances can be applied across a wide range of sensor applications.

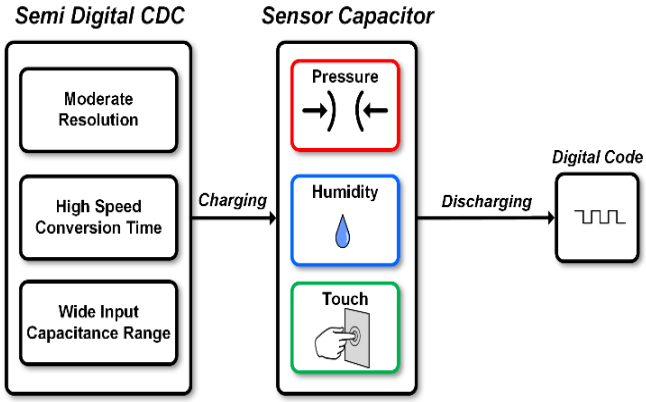

Fig. 1. Concept of semi-digital CDC of the capacitive sensing system.

Additionally, achieving high resolution and linearity is essential for accurately detecting small capacitance variations. Several main CDC architectures have been extensively researched, including the successive approximation register (SAR) CDC, the Δ-Σ(Delta-Sigma) CDC, and the Zoom CDC. The SAR CDC estimates the target capacitance through a successive approximation process. It converts the sensed voltage into a digital binary value and iteratively compares it to the input signal to determine each subsequent bit, ultimately generating the final digital code. SAR CDCs offer high energy efficiency for medium-resolution applications and benefit from a relatively simple design. However, they can suffer from thermal noise due to passive charge sharing between the sensor capacitor and the internal CDAC (Capacitive DAC). While an OTA-based active charge transfer method can mitigate this noise, it inevitably increases power consumption. Moreover, achieving higher resolution requires a low-noise comparator, which operates at each bit comparison, further reducing power efficiency.

The Δ-Σ CDC oversamples the input signal and employs a feedback loop to suppress noise, thereby achieving high resolution and enabling the detection of very small capacitance variations. After sampling, the data is converted into a digital signal and processed through a low-pass filter to reconstruct the original signal. While Δ-Σ CDCs are known for high resolution and low noise, they often rely on an OTA-based integrator in the loop filter, which consumes static current and limits energy efficiency. Furthermore, in typical single-bit loop designs, the required oversampling

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Manuscript Received Jan. 10, 2025, Revised Mar. 20, 2025, Accepted Mar. 25, 2025

ratio can be excessively high.

A Zoom CDC integrates aspects of both SAR and Δ-Σ CDCs by first using a SAR CDC to obtain an initial measurement, followed by a Δ-Σ approach to refine the result [3]. This enables fast conversion while leveraging noise shaping, thereby simultaneously achieving high resolution, low noise, quick conversion, and relatively low power consumption. However, by integrating both SAR and Δ-Σ, zoom CDCs inherit the complexities and drawbacks of each, often resulting in increased design complexity and power consumption.

Conventional CDC architectures have achieved high resolution and SNR in the unit of [aF], but they do not have a wide input range, restricting applicability across different sensor systems. SAR CDC can sense up to about 75 pF, Δ-Σ CDCs around 1 pF, and Zoom CDCs up to 5 pF of capacitance range.

To address the need for high-resolution over a wider input range, recent research has introduced a semi-digital CDC design (Fig. 1). This CDC approach first fully charges both the sensor and subtraction capacitors, then discharges them while measuring the discharge time or the number of discharge cycles, which is then converted into a digital code. Although this method may have slightly reduced resolution and longer conversion times, the predominantly digital circuit structure facilitates low-power operation. Additionally, allowing the capacitor to fully charge before starting the conversion helps extend the input capacitance range.

This paper presents a single-slope regulation CDC architecture featuring a configurable charge subtraction capacitor array, enabling an improved semi-digital CDC design with an extended input range. Section II describes the proposed architecture and its operational principles. Section III provides post-layout simulation results and a performance comparison with existing works. Finally, Section IV concludes the paper by summarizing the key findings and contributions.

II. PROPOSED ARCHITECTURE

A. Proposed Design

The overall block diagram of the proposed capacitance-to-digital converter is shown in Fig. 2. The proposed CDC is based on a self-sensing mechanism, allowing the selection between an external sensing capacitor and an internal capacitor.

The detailed circuit implementation of the proposed CDC is illustrated in Fig. 3. The sensor capacitor is charged through a PMOS switch, and the stored charge is subsequently evaluated using a discharge capacitor and a comparator inside the CDC. The comparator consists of a preamplifier and a strong-arm latch, ensuring precise voltage comparison between the charged sensor capacitor and the selected discharge capacitor. Furthermore, as shown in Fig. 3, the proposed CDC can also function as a test vehicle for verifying chip functionality and performance by connecting the internal capacitor.

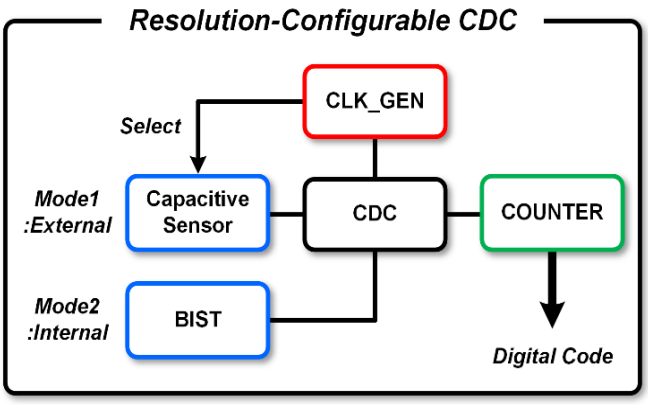

Fig. 2. Top block diagram of the proposed CDC.

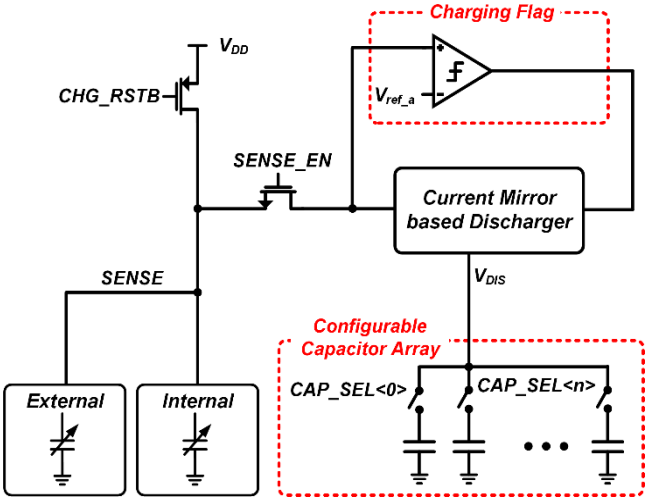

Fig. 3. Overall circuit implementation of the proposed CDC.

The key features of the proposed CDC include a current mirror-based discharger structure with a charging flag and a configurable charge subtraction capacitor array, implemented within a single-slope regulation framework. This architecture enables efficient charge redistribution while maintaining high resolution and a wide input capacitance range.

B. Single-Slope CDC with Configurable Subtraction Capacitor Array

The single-slope CDC is a traditional capacitive architecture. In this design, the sensor capacitor is first charged based on the sensed capacitance value. Then, using a binary-weighted discharge capacitor, the charge is subtracted step by step, converting the capacitance into a digital output [4].

In the proposed design, a configurable discharge capacitor selection mechanism is implemented. A control signal determines which discharge capacitor inside the CDC will be utilized. The sensor capacitor is charged to V_{dd} via a source follower, ensuring that the discharge current remains stable, as regulated by the previously introduced current

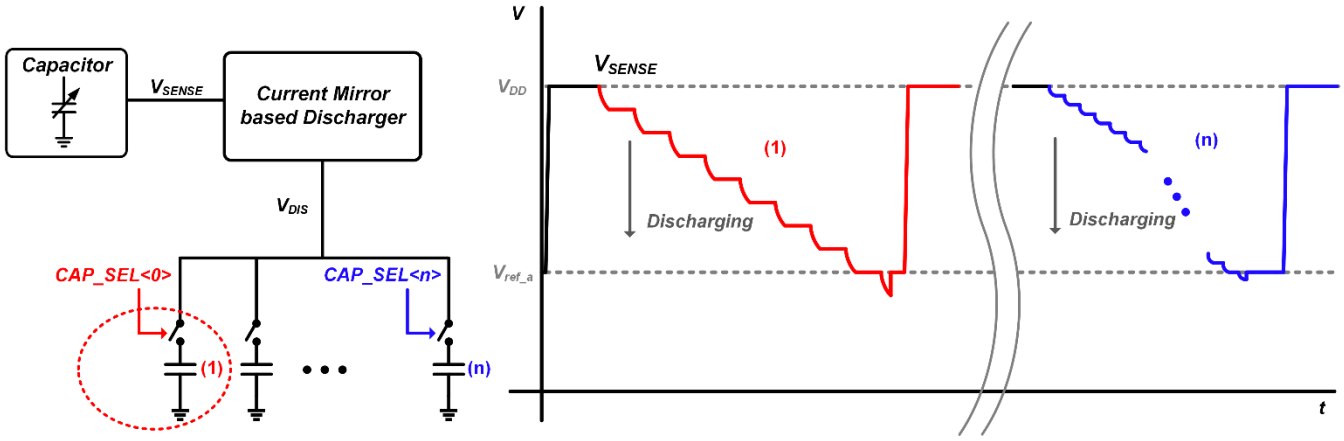

Fig. 5. Discharge operation for each selected configurable capacitor.

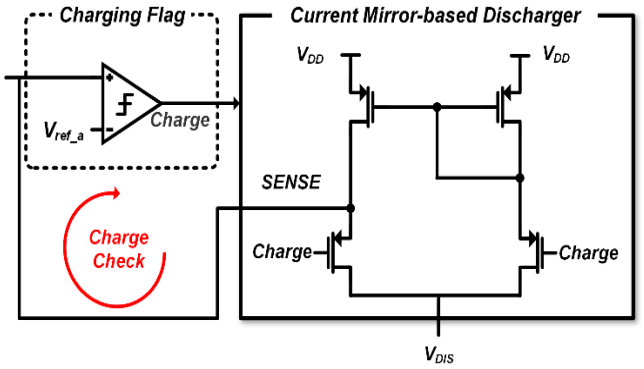

Fig. 4. Overall circuit implementation of the current mirror-based discharger.

mirror-based discharger structure. The stored charge in the sensor capacitor is subsequently discharged through the OTA and source follower. The number of discharge cycles required to reach a predefined voltage threshold is counted, and this count is used to digitally represent the sensor capacitance.

This structure is particularly well-suited for implantable sensor systems, as it maintains high resolution compared to conventional CDC architectures. Additionally, by selecting an appropriate discharge capacitor, the input capacitance range can be dynamically adjusted, making the CDC adaptable for various sensing applications.

Fig. 4 illustrates the detailed operation of the configurable charge subtraction capacitor. After the sense node capacitor is fully charged to V_{dd}, it is discharged through the current mirror-based discharger into the selected subtraction capacitor. The effective capacitance that can be measured at the sense node varies based on the selected subtraction capacitor, affecting both the number of discharge cycles and the voltage step size.

For instance, as shown in Fig. 4, suppose a 1 nF sensor capacitor is connected to the sense node, and the 128 pF subtraction capacitor called case (1) is selected. In this case, the capacitor discharges as depicted by the red waveform in Fig. 4. The discharge count is recorded by the digital circuit, allowing the sensor capacitance to be estimated. Conversely, if a smaller subtraction capacitor, such as the 128 pF called case (4), is selected instead, the discharge follows the blue waveform in Fig. 4. The number of discharge cycles decreases as the subtraction capacitor's capacitance increases, whereas the voltage step per discharge event becomes larger. Moreover, increasing the subtraction capacitor capacitance results in a shorter conversion time. Therefore, the proposed CDC provides a flexible and configurable subtraction capacitor selection mechanism, allowing it to be adapted to different sensor systems based on application-specific requirements. Additionally, as the selected subtraction capacitor increases in capacitance, the maximum measurable sensor capacitance at the sense node also increases, which is further validated in the simulation results section.

C. Current Mirror-based Discharger with Charging Flag

A current mirror-based discharger with a charging flag comprises a current mirror and a comparator. The sense node voltage is continuously compared to a reference voltage, and a charging flag is used for control. When the sense node voltage drops below the reference voltage level, the charge signal is asserted to reset the discharge process and restore the capacitor to its initial charged state. An end signal is generated, followed by a reset signal, allowing the sensor capacitor to recharge.

As illustrated in Fig. 5, this structure enables a repetitive discharge process. In each cycle, the discharge time is measured and converted into a digital value to estimate the sensor capacitance until the charging flag is triggered. Moreover, because the capacitor is fully charged at the start of every conversion cycle, the proposed method supports a wider input capacitance range while maintaining measurement accuracy.

III. SIMULATION RESULTS

Fig. 6 and 7 present the simulation results of the proposed CDC. The digital code in the simulation results represents the

TABLE I. COMPARISON TABLE AND SUMMARY OF THE STATE OF THE ART

	This Work	ISSCC'14 [1]	JSSC'13 [2]	JSSC'17 [3]	NEWCAS'20 [4]	ISSCC'15 [5]
Type	Single Slope	SAR	ΔΣM	SAR + VCO-ΔΣM	Single Slope	Iterative Delay-Chain
Process	180 nm	180 nm	160 nm	40 nm	180 nm	40 nm
Cap Range [pF]	1,000	2.5~75.3	0.54~1.06	5	0.5~8.5	0.7~10,000
Conv. Time [μs]	500	4 ms	800	1	192	19.06
Min. Resolution [fF]	10	6	0.07	1.1	6.84	12.3
Power [μW]	135.72	0.16	10.3	0.075	2.75	1.84

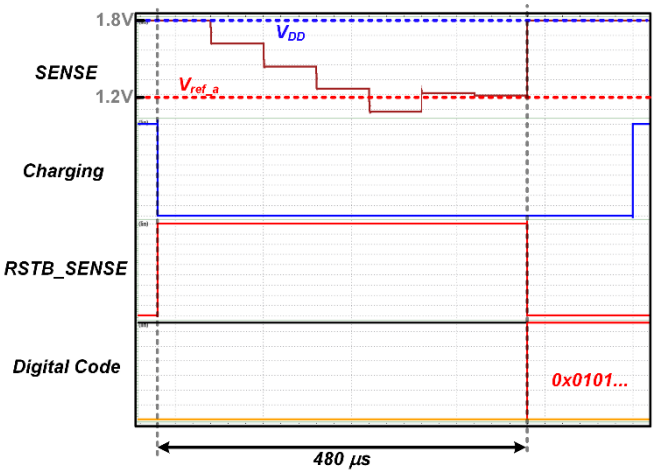

Fig. 6. Simulation results of the proposed CDC with large capacitor at 400 pF.

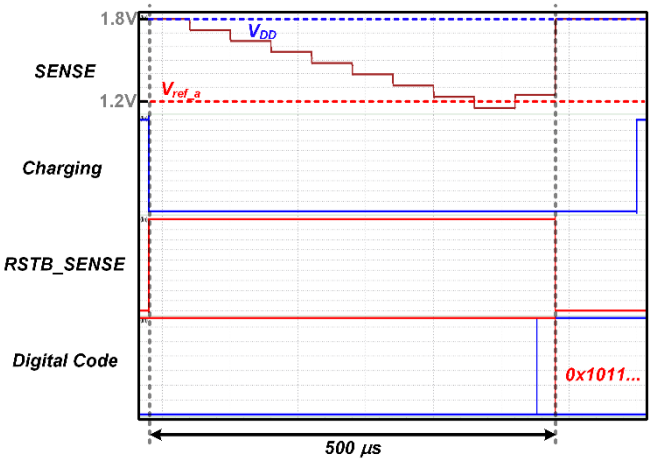

Fig. 7. Simulation results of the proposed CDC with a small capacitor at 400 pF.

number of discharge events contributed by the discharge capacitor. By counting the number of discharge cycles at each bit, the total capacitance value is converted into a digital code.

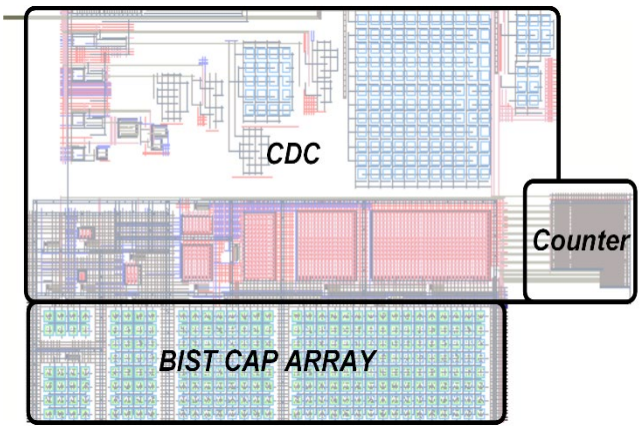

Fig. 8. Layout of the proposed CDC.

Fig. 6 and 7 illustrate the scenario in which a 400 pF sensor capacitor is connected to the sense node. As observed from the comparison between the two figures, increasing the capacitance of the selected discharge capacitor results in a shorter conversion time, fewer discharge cycles, and a larger discharge voltage step. Furthermore, the digital code values obtained from the simulation results show a discrepancy between those in Fig. 6 and 7. Additionally, increasing the capacitance of the discharge capacitor allows for a greater measurable sensor capacitance.

Additionally, the simulation results confirm that the proposed CDC can successfully convert capacitances up to 1 nF into digital values within 500 μs. The minimum resolution remains consistent across different capacitance ranges, making the CDC highly adaptable to various sensor systems. The layout of the proposed circuit is shown in Fig. 8. Furthermore, as demonstrated in Table I, which compares the post-layout simulation results with those of previously published works, the proposed CDC achieves a wider capacitance coverage of 1 nF and a minimum resolution of 10 fF with a power consumption of 135.72 μW. These results highlight the high resolution achieved within a wide capacitance range, demonstrating the effectiveness of the proposed design.

IV. CONCLUSION

In this paper, we propose a semi-digital CDC architecture that utilizes a configurable charge subtraction capacitor and a current mirror-based discharge structure to support an expanded input capacitance range of up to 1 nF while maintaining high resolution. The semi-digital CDC operates by charging the target capacitance and counting the number of discharge cycles to convert it into a digital value. This method eliminates the need for OTAs or complex analog circuitry, which are typically required in conventional CDCs, thereby reducing design complexity and cost. The proposed design employs a single-slope discharge mirror to ensure high resolution over a wider input capacitance range. Additionally, the configurable charge subtraction capacitor enables the system to accommodate a wide range of input capacitances up to 1 nF, making it highly adaptable for various capacitive sensing applications. The simulation results validate that the proposed CDC achieves a minimum resolution of 10 fF for an input capacitance of 1 nF. This demonstrates high accuracy over a wide capacitance range. Furthermore, these results confirm the feasibility of implementing the proposed architecture in high-precision capacitive sensing systems with a wide input range.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

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